4
Semiconductor:Polymer Blend OFETs

Performance of the OFETs is highly dependent on the quality of dielectric-semiconductor interface. A superior quality of this interface leads to higher performance in devices. In a device, where semiconductor is directly deposited over the inorganic dielectric layer, this interface suffers from various defects, which act as charge trapping locations. In order to improve quality of dielectric-semiconductor interface and hence the device performance, a thin buffer layer of polymeric insulator can be incorporated in between the organic semiconductor and the inorganic dielectric layer. However, subsequent solution processing over this polymeric buffer layer remains a challenge. Another promising way to enable solution processing of polymers and organic semiconductors together is through their blends, which causes development of a very uniform interface in comparison to most of the other processing schemes, which in turn materializes in form of much better device performance. In this chapter, improved device performance and stability of semiconductor:polymer blend OFETs due to process of vertical phase separation have been discussed and compared with neat semiconductor OFETs. Results discussed in this chapter have been recently published [Bharti and Tiwari, 2016].

4.1 INTRODUCTION

In OFETs, it is the quality of dielectric-semiconductor interface, which largely affects the carrier mobility and electrical stability. A superior quality of the above interface is highly desirable for obtaining high performance in the devices. However, improving the quality of dielectric-semiconductor interface in the case of solution processed OFETs is quite challenging due to various intricate reasons which are related with material properties of dielectric and semiconductor and film processing conditions. Use of a polymeric gate dielectric has been confirmed as one of the simple ways to form a high quality semiconductor-dielectric interface leading to an excellent device performance [Faraji *et al.*, 2015, Sheida *et al.*, 2016]. An appropriate polymeric dielectric material may also conceal the surface defects of the inorganic dielectric layer and acts as a barrier for the moisture to reach the surface of the inorganic dielectric [Kalb *et al.*, 2007], ultimately resulting in superior electrical performance and electrical stability in OFETs [Tiwari *et al.*, 2009]. The advantages incurring due to use of a polymeric dielectric can further be strengthened if the dielectric-semiconductor interface is developed uniformly from proper phase separation in the blends of polymer and organic semiconductor [Jin Lee *et al.*, 2015, Shin *et al.*, 2013]. A surface energy driven vertical phase stratification in the blends of polymer and organic semiconductor causes formation of a high quality of dielectric-semiconductor interface [Naden *et al.*, 2014], directing the way for superior performance and stability in OFETs [Lee *et al.*, 2015, Lee *et al.*, 2009, Niazi *et al.*, 2015].

Various polymeric materials including poly(α-methylstyrene) (P-αMS), poly(triarylamine) (PTAA), polystyrene (PS), and poly(methylmethacrylate) (PMMA), have been investigated with many small molecule organic semiconductors. However, reports with mobility values higher than 1.0 $cm^2 V^{-1} s^{-1}$ are still scarce. In addition, reports on high mobility blend OFETs based on TIPS-pentacene are rare with maximum reported mobility of 2.8 $cm^2 V^{-1} s^{-1}$ [Hwang *et al.*, 2012]. Moreover, the procedure used to deposit thin films from the blends of organic semiconductor-polymer blend is widely spin coating [Hwang *et al.*, 2012, Faraji *et al.*,

2015, Smith *et al.*, 2012], however, this method does not provide substantial degree of crystallinity in the active layer due to insufficient time available for molecular rearrangement. While depositing films using semiconductor-polymer blend solutions, incorporation of a scheme like drop casting [Bharti and Tiwari, 2016, Kim *et al.*, 2014], where ample amount of time is available for molecular settlement due to slower evaporation rate of solvent, a high carrier mobility is expected due to merits of high degree of crystallinity and articulate phase separation leading to high quality semiconductor-dielectric interface. This aspect has not been given its due attention lately and high mobility OFETs fabricated using drop cast scheme with these blend solutions are not yet fully explored for their performance and electrical stability.

In this chapter, TIPS-pentacene:polystyrene blend and neat TIPS-pentacene OFETs have been fabricated by a facile drop cast method on rigid Si/SiO_2 substrates and have been systematically explored for their performance and stability. A uniform phase separation between organic semiconductor and polymer in the blend films was confirmed using scanning electron microscopy (SEM). Improved crystallinity of the active semiconductor layer and a high quality of dielectric-semiconductor interface developed because of vertical phase separation resulted in to a maximum mobility of 2.6 $cm^2\ V^{-1}\ s^{-1}$ in TIPS-pentacene:PS blend OFETs. Complete recovery of electrical characteristics in blend devices from the degrading effects of gate bias-stress further supported the assertion of improved interfacial conditions. Electrical repeatability study also verified consistent and stable device operation for polymer blend OFETs in comparison to those with SiO_2 gate dielectric [Bharti and Tiwari, 2016].

4.2 PHASE SEPARATION IN SEMICONDUCTOR:POLYMER BLENDS

One of the main challenges associated with solution processing of small molecule organic semiconductor is their tendency to dewet during solvent evaporation [Kang *et. al.*, 2008] [Chung *et al.*, 2011], which causes a discontinuous film formation and poor or no device behavior. Even slightest of the deviation in the drying condition can alter film growth and its crystallinity [Zhao *et al.*, 2016]. An excellent film formation requires crystallization to be initiated from the solid–liquid interface [Li *et al.*, 2013]. Dewetting of the small molecule based organic semiconductor can be largely avoided by blending it with a polymer, which is a popular technique to improve processability, reproducibility, and stability of small molecule OFETs [Kang *et al.*, 2008, Ohe *et al.*, 2008, Madec *et al.*, 2008, Smith *et al.*, 2008]. This method derives its beneficial features from the ability of the organic semiconductor and polymer to phase separate themselves into layered structure while maintaining the general attribute of the organic semiconductor [Kang *et al.*, 2008, Ohe *et al.*, 2008]. It is a complex phenomenon, which in ideal cases, should result into the formation of large, and inter-connected crystalline domains of continuous and stratified layers of highly crystalline small molecule OSC [Lee and Park, 2014]. Phase separation in blends takes place either via the nucleation and growth or by the spontaneous (spinodal) route [Budkowski, 1999] and it is dependent on the free energy of the system [Smith *et al.*, 2010]. There are several types of factors which affect the process of vertical phase separation including molecular (i.e., miscibility and concentration of the components, molecular weight and solvent), thermodynamic (i.e., composition, temperature, and pressure) and processing (i.e., substrates, film deposition method) [Lee and Park, 2014]. Miscibility is commonly determined by using the Flory-Huggins interaction parameter (χ) [Bawendi and Freed, 1988]. A high χ value indicates a strong probability of phase separation. The choice of solvent determines the solvent evaporation rate, surface tension and viscosity. A solvent with higher boiling point will have a lower evaporation rate and thus will take more time for phase separation and vice versa. Solubility of organic semiconductor and polymer in the solvent also governs the pattern of the phase separated layers, as the solute with lower solubility solidifies first from the solution. The surface energy of the substrate is another important parameter regulating the pattern of phase separation. The component having least surface energy mismatch with that of the substrate, will acquire the substrate-film interface, with segregation of the other component on the air-film interface [Lee and Park, 2014].

Several studies have discussed the critical role of above mentioned parameters in the process of vertical phase separation and resultant film structure. For example, the formation of a polycrystalline diF-TES-ADT layer on top of PMMA or severe dewetting was shown to be dependent on the solvent evaporation rate [Lee *et al.*, 2012]. TIPS–pentacene segregation at both interfaces (air-film and film-substrate) with a poly(α-methyl styrene) (PαMS) layer in the middle was reported by Ohe *et al.*, which remained largely intact with thermal annealing [Ohe *et al.*, 2008]. Similar structure of the phase separated TIPS-pentacene was reported in another study [Cho *et al.*, 2013]. The crystallinity of the polymer also affects the process of vertical phase separation. When TIPS–pentacene was blended with a semicrystalline isotactic polystyrene (i-PS), stratification occurred at both interaces with a polymeric layer in the middle, whereas when the blend was made with semicrystalline syndiotactic polystyrene (s-PS), the segregation and crystallization of TIPS-pentacene was hindered [Madec *et al.*, 2008]. Smith *et al.* reported that amorphous semiconducting polymer can aid in the conduction process across the grain boundaries of diF-TES-ADT rich regions when the diF-TES-ADT is blended with poly(triarylamine) (PTAA) or poly(dialkyl-fluorene-co-dimethyl-triarylamine) (PF-TAA) [Smith *et al.*, 2012, Hamilton *et al.*, 2009]. These fundamental aspects of vertical phase separation should be given adequate attention, when objective is to use the film obtained from the blend solution as the active layer for OFET applications.

4.3 FABRICATION OF DEVICES

Devices were fabricated on highly doped n-type Si wafers with 300 nm thermally grown SiO_2 layer. Semiconductor and polymer materials were purchased from Sigma-Aldrich and used as received without purification. Si/SiO_2 substrates were thoroughly cleaned in heated solvents of 2-propanol, trichloroethylene, and methanol and copious amount of deionized water respectively, and then dried by a N_2 blow. Solutions of 1.0 wt.% each of TIPS-pentacene and polystyrene (M_W ~ 280,000) were prepared in toluene and stirred at 70° C for 3 hours. Blend solutions were prepared by mixing TIPS-pentacene and PS stock solutions in 3:1 ratio by volume, followed by a vigorous shaking. Neat TIPS-pentacene and TIPS-pentacene:PS blend solutions were drop casted on substrates inclined at small angle (~5°) and the films were allowed to dry overnight in a solvent rich environment by covering with a glass petri dish. Subsequently, annealing at 70 °C for 30 minutes was done to evaporate any residual solvent in the films. To form Source-Drain contacts, a 200 nm thick Au layer was deposited through shadow masks by thermal evaporation under a high vacuum of 10^{-6} Torr. Three type of device structures are shown in Figure 4.1. All the processing was done in dark and ambient conditions. Capacitance density, C_i, for 300 nm thick SiO_2 layer at 1 KHz was found to be 10.6±0.003 nF/cm^2. C_i, for blend devices was measured from MIS structure (Si/SiO_2/TIPS-pentacene:PS blend film/Au) and found to be 3.1±0.4 nF/cm^2 at 1 KHz.

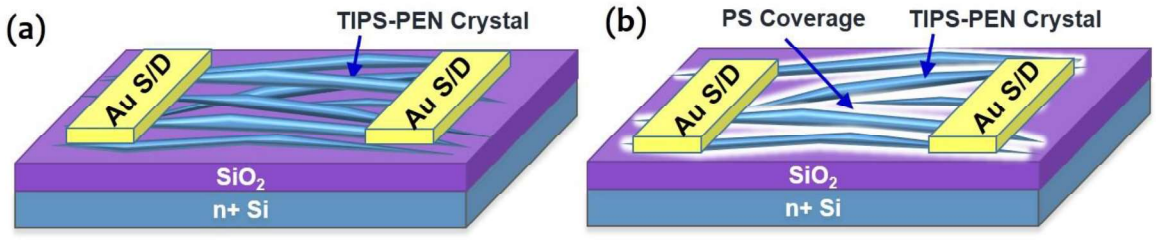

Figure 4.1: Device structure of neat TIPS-pentacene OFETs with SiO_2 dielectric **(a),** and TIPS-pentacene:PS blend OFETs **(b).**

4.4 RESULTS & DISCUSSIONS

4.4.1 Crystallite Characterization

Optical micrographs of crystals obtained from solutions of neat TIPS-pentacene, and TIPS-pentacene:PS blend are shown in Figure 4.2. As expected, in crystals obtained from neat TIPS-pentacene solution, no additional layer was observed, as seen in Figure 4.2(a). However, optical micrograph of Figure 4.2(c) clearly shows a polymeric layer beneath the crystal, which provides elementary sign of the separation of semiconductor molecules and polymer during solvent evaporation. The case of TIPS-pentacene:PS blend (blend of small-molecule semiconductor and insulating polymer) is different than the cases of PANI-PS and polypyrrole-PS blends where conducting and insulating polymer are blend components. Though both types of blends have two-phase structures, spherical aggregates of conducting polymers embedded in the insulating polymer matrix have been observed in latter [Bae et al., 2003, Bhadra et al., 2013, Bhadra et al., 2016, Hosseini and Entezami, 2003], whereas the former forms long crystallites of the semiconductor on the insulating polymer layer.

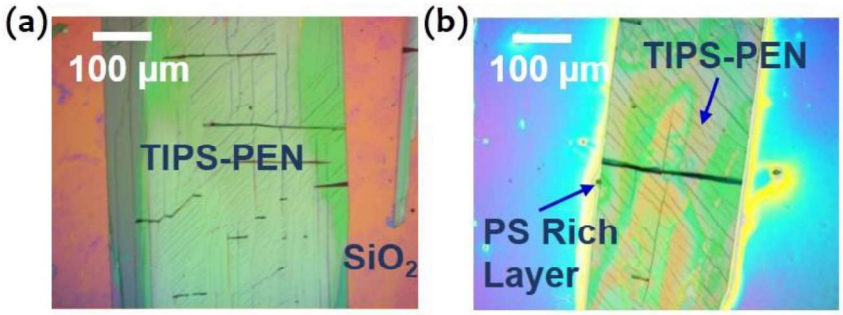

Figure 4.2: Optical micrograph of a crystal obtained from solutions of neat TIPS-pentacene on SiO_2 substrate **(a)**, and TIPS-pentacene:PS blend on SiO_2 substrate**(b)**.

To further confirm the semiconductor and polymer phase separation, the device cross-section was analyzed with SEM. Figure 4.3(a) shows the microscopy image of a TIPS-pentacene crystal on Si/SiO_2 substrate. In agreement with corresponding optical micrography result, no additional layer was seen between the TIPS-pentacene crystal and SiO_2. However, a tri-layer phase separated structure of TIPS-pentacene:polymer blend film was clearly observed in Figure 4.3(b) in line with most of the studies reported thus far [Jung *et al.*, 2010, Kang *et al.*, 2008, Li *et al.*, 2011, Madec *et al.*, 2008, Ohe *et al.*, 2008], where TIPS-pentacene rich phase is expelled to both air-film and film-substrate interfaces, and a polymer rich phase is developed in the middle of these phases. The process of vertical phase separation indeed critically depends on several factors which include surface wettability, material properties, rate of solvent evaporation etc. [Coveney, 2015]. It is crucial to note that vertical segregation is also highly influenced by the molecular weight [Kang *et al.*, 2008] and crystallinity of the polymer [Madec *et al.*, 2008].

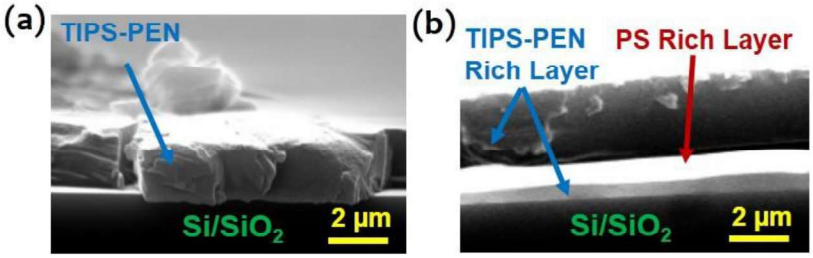

Figure 4.3: Cross sectional SEM image for neat TIPS-pentacene film **(a)**, and TIPS-pentacene:PS blend film **(b)**. Fig. 4.3 (b) shows a clear phase separation in TIPS-pentacene:polymer blend structure.

Figure 4.4 shows AFM images of neat TIPS-pentacene crystals of both cases and polymer blended TIPS-pentacene crystal which confirm the general terracing structure of TIPS-pentacene for each case [Kim *et al.*, 2014, Diao *et al.*, 2013]. Similarity of these images indicates the invariability of the terracing structure from incorporation of polymers in the solution. Figure 4.4(c) shows the X-ray diffractogram of neat TIPS-pentacene and TIPS-pentacene:PS blend films. TIPS-pentacene:PS blend films were found to be more crystalline with a lesser FWHM of 2.90×10^{-3} than the neat TIPS-pentacene film with a higher FWHM of 2.92×10^{-3}. Addition of polymer in the solution retards the solvent evaporation due to increase in the viscosity of the solution [Wicks *et al.*, 2007]. Due to slower rate of solvent evaporation, semiconductor molecules get more time for molecular arrangement, which ultimately leads to a higher degree of crystallinity in TIPS-pentacene:PS blend films than neat TIPS-pentacene case [Lee *et al.*, 2009, Kim *et al.*, 2008].

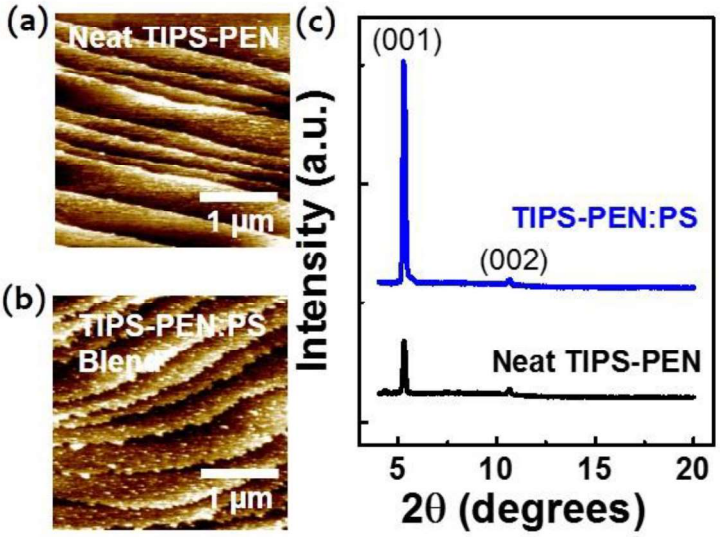

Figure 4.4: AFM image of a crystal obtained from solutions of neat TIPS-pentacene **(a)**, and TIPS-pentacene:PS blend **(b)**. **(c)** X-ray diffractogram of neat TIPS-pentacene and TIPS-pentacene:PS blend film indicating higher crystallinity in the blend films.

4.4.2 Electrical Performance

Figure 4.5 shows the output and transfer characteristics of representative neat TIPS-pentacene and TIPS-pentacene:PS blend OFETs. TIPS-pentacene:PS blend OFETs outperformed neat TIPS-pentacene devices with excellent electrical characteristics. Extracted parameters for both types of TIPS-pentacene devices are given in Table 4.1. Devices fabricated with neat TIPS-pentacene solution exhibited considerably lower mobility with average μ_{sat} (7 devices) and μ_{max} of 0.10±0.06 and 0.2 $cm^2\ V^{-1}\ s^{-1}$ respectively. Average μ_{sat} calculated from 13 devices of the same batch for TIPS-pentacene:PS blend devices was 1.5±0.6 $cm^2\ V^{-1}\ s^{-1}$ with maximum mobility (μ_{max}) soaring as high as 2.6 $cm^2\ V^{-1}\ s^{-1}$, which is one amongst the highest reported mobility values for TIPS-pentacene OFETs. Moreover, all the high mobility values for TIPS-pentacene reported till date has been obtained with considerably high operating voltages (-40 to -100 V) [Giri *et al.*, 2011, Giri *et al.*, 2014, Xue *et al.*, 2015], whereas high mobility values are obtained here for a moderate operating voltage (-30 V). Apart from mobility, TIPS-pentacene and polymer blend devices also feature very high I_{ON}/I_{OFF} (>8×10^6). Relatively large values of standard deviations in average mobility values for all categories of OFETs are due to inherent feature of nonuniformity of the drop cast devices. The process trans-conductance, which is the product of mobility and capacitance density, is more reliable parameter to determine the superiority of the device. The maximum value of this parameter was 8.06 $nF\ V^{-1}\ s^{-1}$ for TIPS-pentacene:PS blend devices, with respect to 2.12 $nF\ V^{-1}\ s^{-1}$ for neat TIPS-pentacene

OFETs. The higher value of process trans-conductance for blend devices suggests the electrical excellence of these devices.

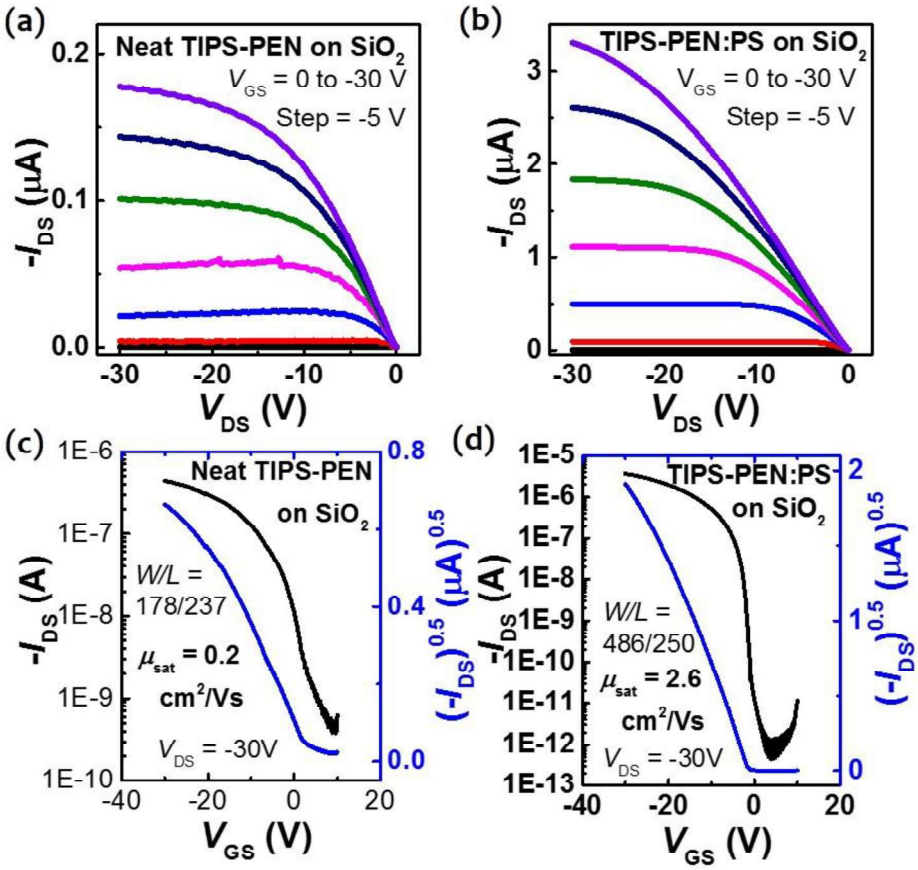

Figure 4.5: (a) & (b) Output and **(c) & (d)** transfer characteristics of a representative neat TIPS-pentacene and TIPS-pentacene:PS blend OFET respectively.

Table 4.1: Summary of extracted electrical parameters for studied devices

Device	μ_{sat} ($cm^2\ V^{-1}\ s^{-1}$)	μ_{max} ($cm^2\ V^{-1}\ s^{-1}$)	C_i ($nF\ cm^{-2}$)	$\mu_{max}C_i$ ($nF\ V^{-1}\ s^{-1}$)	V_{TH} (V)	I_{ON}/I_{OFF}	SS (V/dec.)	D_{it} ($cm^{-2}\ eV^{-1}$)
Neat TIPS-pentacene	0.10 ±0.06	0.2	10.6	2.12	2.52 ±1.52	10^3-10^6	4.1 ±1.7	(4.6±1.9) $\times10^{12}$
TIPS-pentacene :PS Blend	1.5 ±0.6	2.6	3.1	8.06	-2.70 ±1.88	10^5-10^7	1.4 ±0.9	(0.5±0.4) $\times10^{12}$

Performance enhancement in blend devices has been achieved due to process of vertical phase stratification in the solution cast TIPS-pentacene:PS blend film. Vertical phase separation results in multifaceted improvements in the quality of dielectric-semiconductor interface and semiconductor morphology which largely depends on the characteristics of the phase separation [Kang *et al.*, 2008, Li *et al.*, 2011]. It is important to note that most of the studies have reported the bottom-segregated TIPS-pentacene layer on SiO_2 as the functional dielectric-semiconductor interface in the bottom contact devices [Kang *et al.*, 2008, Li *et al.*, 2011, Ohe *et al.*,

2008]. However, for the top contact devices in this study, interface of top segregated TIPS-pentacene and middle polymer rich layer acts as the dielectric-semiconductor interface. This inference is further supported by a much lower capacitance density for the case of TIPS-pentacene:PS blend devices than that of neat TIPS-pentacene devices. At this functional interface, performance improvement can be attributed to various factors intricately dependent on each other. First factor is the reduced dipolar disorder and carrier localization at the interface due to a less polar, low-k polymeric dielectric, which reduces the broadening of density of states and ultimately the trap state density [Hulea *et al.*, 2006, Kalb *et al.*, 2010, Sworakowski, 1999, Veres *et al.*, 2003]. Lower D_{it} values for polymer blend devices, as shown in Table 4.1, further validate this fact quantitatively. Second factor can be the improved active layer morphology with the inclusion of polymer binder [Li *et al.*, 2011]. Polymer binder impedes the solvent evaporation, which in turn supports a better degree of molecular arrangement and hence a higher crystalline order [Kim *et al.*, 2008, Lee *et al.*, 2012]. This was also verified through X-ray diffraction study, where TIPS-pentacene:polystyrene blend films have shown enhanced degree of crystallinity (Figure 4.4(c)). Table 4.2 compares performance of some previously reported TIPS-pentacene:polymer blend OFETs with this study. Distinct performance advancement over other studies can easily be noticed on the basis of superior mobility, high I_{ON}/I_{OFF}, moderate operating voltage and a high value of product of capacitance density and maximum mobility.

Table 4.2. Comparative Summary of TIPS-pentacene:polymer blend OFETs on rigid substrates

Ref.	Substrate /Dielectric	Dev. Config.	Polymer Binder	Ratio	V_{DD}	C_i (nF cm^{-2})	μ_{max} (cm^2 V^{-1} s^{-1})	I_{ON}/I_{OFF}
[Madec *et al.* 2008]	Si/SiO_2 (300 nm)	BGTC	PS	1:4	80	-	~0.03	10^4
[Kang *et al.* 2008]	Si/SiO_2 (300 nm)	BGBC	PαMS	1:1	40	11.5	0.54	10^5
[Li *et al.* 2011]	Si/SiO_2 (140 nm)	BGBC	PS	-	10	-	1.50	>10^7
[Lada *et al.* 2011]	Glass/ Cytop (~1 µm)	TGBC	PS	1:3	60	1.7	1.80	-
[Cho *et al.*, 2013]	ITO/ organic insulators	BGTC	APC	1:4	40	9.4	0.68	10^6
[Hwang *et al.*, 2014]	Glass/ Al_2O_3 (50 nm) & Cytop (45 nm)	TGBC	PTAA	1:1	8	35.2	0.70	10^4
This work	Si/SiO_2 (300 nm)	BGTC	PS	1:3	30	3.1	2.6	~10^7

4.4.3 Electrical Stability

Reliability of OFETs significantly depends on the electrical stability during operation [Tiwari *et al.*, 2009, Sirringhaus, 2009]. To study the electrical stability, firstly, OFETs were subjected to constant bias-stress. Figure 4.6 shows the time dependent normalized I_{DS} decay in saturation regime for neat TIPS-pentacene and TIPS-pentacene:PS blend devices under bias-stress for 2 hours at V_{DS} = V_{GS} = -30 V. Under constant bias-stress, I_{DS} monotonically decreases for both cases. Reason for this reduction in I_{DS} is the bias-stress induced V_{TH} shift (ΔV_{TH}) which occurs due to charge trapping in various regions in the device including at semiconductor-dielectric interface [Street *et al.*, 2006, Mathijssen *et al.*, 2008, Sharma *et al.*, 2010]. Figure 4.6 indicates that polymer blend devices cope with bias-stress reasonably well. I_{DS} decay is higher

for neat TIPS-pentacene devices (~80%), because of excessive charge trapping due to -OH groups present on SiO_2 layer [Zhang *et al.*, 2013]. Terminating -OH group of SiO_2 layer further attracts moisture at its surface, which in turn aggravates charge trapping. In devices with blends, the location of major charge trapping is shifted from -OH rich, moisture attracting SiO_2 surface to hydroxyl free dielectric-semiconductor interface of low-k polystyrene and top segregated TIPS-pentacene, where reduced dipolar disorder and carrier localization at the interface cause lower charge trapping [Hulea *et al.*, 2006, Kalb *et al.*, 2010, Sworakowski, 1999, Veres *et al.*, 2003] and subsequently a considerably lower I_{DS} decay of ~30%.

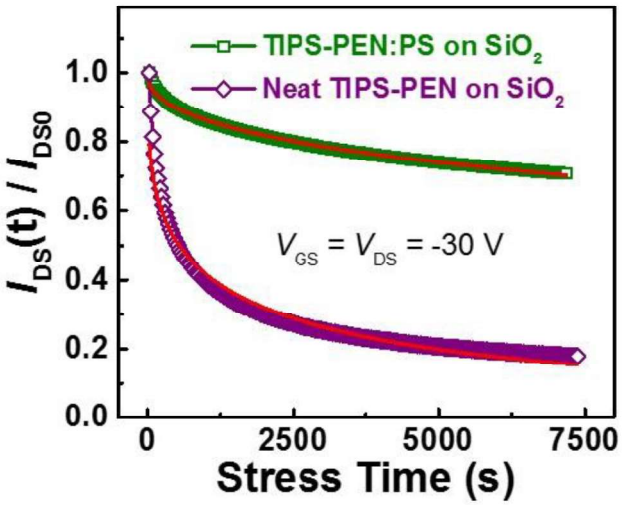

Figure 4.6: Drain current decay as a function of stress time. Total stress time was 2 h and current values were recorded in the interval of 30 s.

To further explain the I_{DS} decay analytically, the ratio of the I_{DS} in saturation regieme at time t and 0 s during bias-stress can be given as a stretched exponential function [Tiwari *et al.*, 2009],

$$\frac{I_{DS}(t)}{I_{DS}(0)} = \exp\left(-2\left\{\frac{t}{\tau}\right\}^{\beta}\right) \qquad (4.1)$$

where β is a temperature dependent dispersion parameter and τ is relaxation time, a measure of typical trapping time of charge carriers. β reflects the width of involved trap distribution. β and τ extracted from experimental data by fitting stretched exponential are given in Table 4.3.

Table 4.3. Fitting parameters for stretched exponential

Device	β	τ (s)
Neat TIPS-pentacene	0.38	8.70×10^{3}
TIPS-pentacene:PS blend	0.44	3.59×10^{5}

τ values for these devices support the inference drawn earlier according to which neat TIPS-pentacene devices are marred with extensive charge trapping with considerably small trapping time of 8.70×10^{3} s whereas in devices with a phase separated layer of hydrophobic

polymer like PS, trapping is substantially reduced with relatively large trapping time of order of 10^5 or higher. Longer trapping time of order of stress duration and higher indicates lesser charge trapping with lesser I_{DS} decay and hence it should result in a smaller shift in V_{TH}.

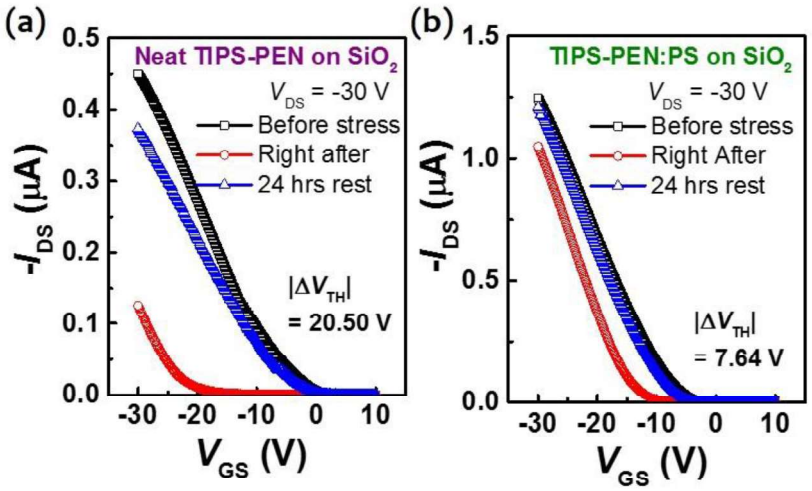

Figure 4.7: Recovery from the effects of bias stress in the saturation regime for a neat TIPS-pentacene device with SiO_2 **(a)**, and TIPS-pentacene:PS blend device **(b)**.

To have a deeper insight on bias-stress instability of device performance, transfer characteristics of the devices under bias stress study were also recorded just before stressing, just after stressing, and after 24 hours of stressing, which are shown in Figures 4.7. For the studied representative device, a noticeable amount of ΔV_{TH} is observed after stressing the device, which is lesser in TIPS-pentacene:PS blend device ($|\Delta V_{TH}|$=7.6 V) compared to neat TIPS-pentacene devices ($|\Delta V_{TH}|$=20.5 V), due to lesser charge trapping at a better quality of semiconductor-polymer interface. TIPS-pentacene:PS blend devices recover almost completely in 24 hours with no reduction in I_{DS}. However, neat TIPS-Pentacene devices which have suffered higher shift of transfer characteristics could not achieve their pristine state even after 24 hours. Incomplete recovery of neat TIPS-pentacene devices indicate the presence of a huge density of deep trap states on hydroxyl rich bare SiO_2 [Sharma *et al.*, 2010, Burson *et al.*, 2013, Isenberg and Saragi, 2014], from where the de-trapping of charge carriers is difficult. In contrast, for blend devices, a lower $|\Delta V_{TH}|$ is obtained due to lesser charge trapping. The lesser charge trapping of blend devices can be observed qualitatively from lesser I_{DS} decay in Figure 4.6 and quantitatively from larger τ values in Table 4.3. The complete recovery of blend devices signifies the dominance of shallow traps at the semiconductor polymer dielectric interface, from where charge carrier can be de-trapped with relative ease.

Results of repeatability study are shown in figure 4.8. Here, transfer characteristics of the devices were recorded continuously for 100 cycles with an interval of 1 second between each cycle. These results are commensurate with previous obtained results of I_{DS} decay and recovery. Because of enormous charge trapping on bare SiO_2 surface, V_{TH} shifts towards negative voltages ($|\Delta V_{TH}|$=7.8 V) with reduction in on current (I_{ON}) of about 7%. However, due to high quality of dielectric semiconductor interface with aforementioned reasons, TIPS-pentacene:PS blend devices showed reliable transfer characteristics with highly stable I_{ON} and small shift in threshold voltages ($|\Delta V_{TH}|$=1.4 V). Interestingly, major trapping occurs during first few cycles, filling almost every deep trap state, after which it is reduced considerably in subsequent cycles.

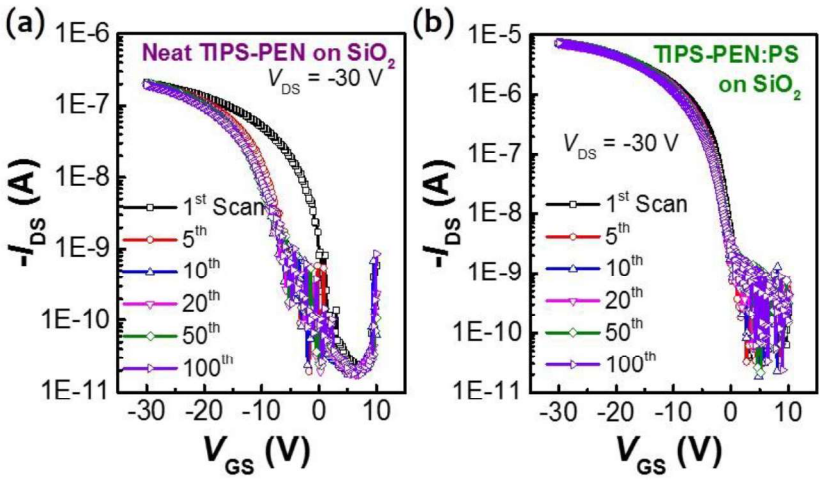

Figure 4.8: Repeatability of electrical characteristics for a neat TIPS-pentacene device with SiO_2 **(a),** and TIPS-pentacene:PS blend device **(b).** TIPS-pentacene:PS device demonstrates a well consistent performance with nearly unchanged performance parameters.

4.5 CONCLUSIONS

A detailed investigation was performed for OFETs based on TIPS-pentacene for high charge carrier mobility and electrical stability. Two types of devices were fabricated on Si/SiO_2 substrates; neat TIPS pentacene, and TIPS-pentacene:PS blend. Average mobility of 1.5 $cm^2\ V^{-1}\ s^{-1}$ (maximum of 2.6 $cm^2\ V^{-1}\ s^{-1}$) was achieved for TIPS-pentacene:PS blend devices, much higher than neat TIPS-pentacene devices with average mobility values of 0.1 $cm^2\ V^{-1}\ s^{-1}$ (maximum of 0.2 $cm^2\ V^{-1}\ s^{-1}$). Vertical phase stratification occurring in blends devices resulted in formation of high quality dielectric-semiconductor interface and improved degree of crystalline nature in the active layer, which materialized in the enhanced electrical performance and stability in the final devices. The bias-stress induced decay in the drain current was much lesser (~30%) in TIPS-pentacene:polymer blend OFETs in comparison to that of neat TIPS-pentacene OFETs (~80%). Electrical characteristics of neat TIPS-pentacene devices were not fully recoverable after rest duration of 24 hours due to extensive degree of charge trapping in deep trap states. However, TIPS-pentacene:PS blend devices were almost completely recovered due to lesser degree of charge trapping at a better quality of dielectric-semiconductor interface. A high electrical stability in TIPS-pentacene:PS blend OFETs was inferred from repeatability studies also.

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