5
TIPS-pentacene based Flexible OFETs

After demonstration of high performance and stability in OFETs on rigid substrates, it is highly imperative to realize the same on flexible platforms for success of many futuristic applications of organic electronics. In addition, obtaining high performance in flexible OFETs was the second main aim of the research work undertaken for this dissertation. Keeping this objective under focus, two types of OFETs (neat TIPS-pentacene on HfO_2/PVP and TIPS-pentacene:PS blends on HfO_2) were fabricated and studied for their electrical performance and stability in this chapter.

5.1 SOLUTION PROCESSED FLEXIBLE OFETs

Union of the emerging fields of flexible electronics and organic electronics has a lot to offer to technological world in combined terms of physical adaptability, simple processing and low cost. Flexible OFETs are the fundamental functional elements in various classic flexible organic electronics applications such as flat panel display drivers and low cost environmental and biological sensors [Fiore *et al.*, 2015, Gelinck *et al.*, 2010, Liu *et al.*, 2015, Min Hee *et al.*, 2012, Uno *et al.*, 2015, Yun *et al.*, 2014], and have been explored with full enthusiasm. Significant endeavors are being made by researchers across the globe to produce high performance flexible organic devices by solution processing for its edge of affordability and simplicity over vacuum processing. Demonstration of high performance solution processed flexible OFETs is challenging due to several factors. First is the inherent imperfection of flexible substrates, which does not support high performance in devices. Second is the lesser degree of control on the growth of solution processed film and corresponding dielectric-semiconductor interface. As also seen in chapter 4, the dielectric-semiconductor interface is one of the crucial functional locations, which governs the overall device performance and stability [Sun *et al.*, 2010, Zhang *et al.*, 2011]. As the incorporation of an organic polymeric dielectric is imperative to augment the quality of the aforementioned interface [Kang *et al.*, 2008], same can be implemented to ameliorate the performance of flexible solution processed OFETs. Organic polymers, which are also solution processed in general, can be used in OFETs as gate dielectric in two ways, either as an extra buffer layer between inorganic dielectric and solution processed semiconductor or together with semiconductor as a blend. For the first strategy, such a polymeric insulator is required over which subsequent solution processing of semiconductor is feasible. Poly(4-vinylphenol) (PVP) is such a polymeric insulator which has been used very commonly with various organic semiconductors where dielectric and semiconductor layers are to be deposited separately [Hwang *et al.*, 2012, Raghuwanshi *et al.*, 2016]. For the second strategy of blending semiconductor and polymer solutions, organic polymers like polystyrene (PS) have been used as compatiable polymers which have resulted in high quality of dielectric-semiconductor interface and subsequent high device performance [Li *et al.*, 2011, James *et al.*, 2011, Feng *et al.*, 2016] on rigid substrates. OFETs fabricated with blend solutions derive their superior electrical performance from vertical phase separation between polymer and semiconductor [Hwang *et al.*, 2012, Min Hee *et al.*, 2012, James *et al.*, 2011]. However, many of these high performance solution processed OFETs are fabricated either on rigid platforms or operate at high voltages [Abe *et al.*, 2014, Smith *et al.*, 2009, Yi *et al.*, 2012]. With aim of realizing various futuristic applications of flexible solution processed organic electronics, it is highly essential to materialize the superior

device performance in flexible solution processed OFETs and same is very important to explore in detail.

In this chapter, two device strategies (neat TIPS-pentacene on HfO_2/PVP and TIPS-pentacene:PS blends on HfO_2) have been implemented on flexible substrates. The high quality of dielectric-semiconductor interface developed in blend OFETs results in an excellent electrical performance in these devices with maximum field-effect mobility up to 0.93 $cm^2 V^{-1} s^{-1}$ (average of 0.44±0.25 $cm^2 V^{-1} s^{-1}$) in comparison to that of 0.23 $cm^2 V^{-1} s^{-1}$ (average of 0.11±0.08 $cm^2 V^{-1} s^{-1}$) for neat TIPS-pentacene devices. Near zero threshold voltages and high on-off current ratios of order of 10^5 were achieved for both types of devices. In addition, under the effects of gate bias stress, blend devices exhibited lesser levels of current decay than their neat counterparts.

5.2 FABRICATION OF FLEXIBLE OFETs

Indium tin oxide (ITO) coated flexible polyethylene terephthalate (PET) substrates (thickness = 127 µm, surface resistivity 60 Ω/sq.) were used to fabricate OFETs in bottom-gate top-contact architecture. Substrates were cleaned by ultrasonic bath in methanol, de-ionized water and 2-propanol respectively, and then were dried in N_2 blow. A 40 nm thick HfO_2 was deposited on the cleaned substrates by atomic layer deposition (ALD) using tetrakis(dimethylamido)hafnium (TDMAH) and H_2O as precursors at deposition temperature of 100 °C. For fabricating dielectric layer in neat TIPS-pentacene devices, a solution of 3.4 wt. % PVP (M_W ~ 25,000) and 1.1 wt. % poly(melamine-coformaldehyde) which is a cross-linking agent, was prepared in propylene glycol monomethyl ether acetate (PGMEA) and was stirred at room temperature for 24 hours. PVP solution was spin coated at 1500 rpm for 30 sec on the top of HfO_2 layer. Samples were then kept on hotplate at 80 °C for few minutes to quickly evaporate the solvent PGMEA, which was followed by annealing at 90 °C for 3 hours to promote cross linking. A 0.5 wt. % solution of TIPS-pentacene was prepared in toluene by stirring at 70 °C for 3 hours. This solution was drop casted on PVP deposited flexible substrates. For blend films, solutions of TIPS-pentacene and PS (M_W ~ 280,000), 0.5 wt. % each were separately prepared in toluene by stirring at 70° C for 3 hours. The blend solution was prepared by mixing TIPS-pentacene and polymer stock solutions in 1:1 ratio by volume, followed by a vigorous shaking. TIPS-pentacene:polymer blend solution was then dispensed on HfO_2 deposited substrates. To create a solvent rich environment for the drying film, the substrates were covered with a glass petri dish. 200 nm thick source-drain contacts of Au were thermally deposited using shadow masks under a high vacuum of 10^{-6} Torr. Figure 5.1(a) and 5.1(b) show the schematic diagrams of the device structures for both types of OFETs. The exact channel length (L) and width (W) of the OFETs were obtained from the lengths and widths of semiconductor crystals joining source and drain contacts. All solution preparations and sample processing steps were done in dark and ambient conditions. C_i for neat TIPS-pentacene devices was obtained from HfO_2/PVP parallel plate capacitors and found to have value of 24.46±0.71 nF/cm^2 at 1 KHz. C_i for TIPS-pentacene:PS blend devices was measured at 1 KHz from MIS structure (ITO/HfO_2/TIPS-pentacene:PS blend film/Au) and was found to be 18.14±1.56 nF/cm^2.

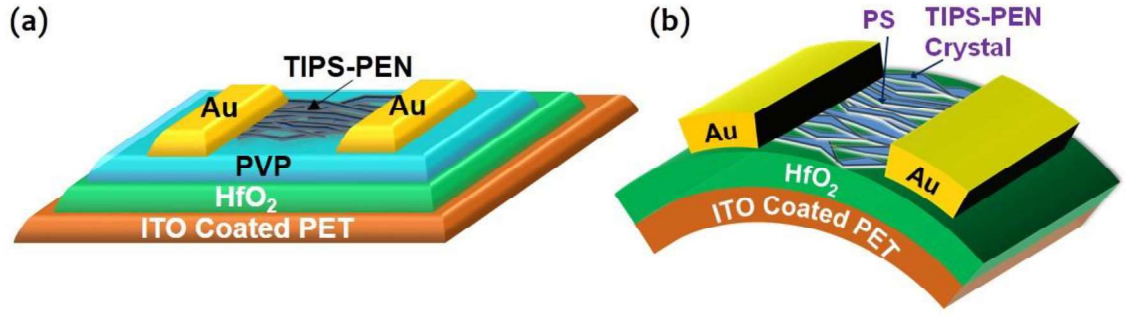

Figure 5.1: Device structure of flexible top contact neat TIPS-pentacene OFET **(a)**, and TIPS-pentacene:PS blend OFETs **(b)**.

5.3 RESULTS & DISCUSSIONS

5.3.1 Crystallite Characterization

Figure 5.2(a) shows the digital image of fabricated flexible OFETs. Figure 5.2(b) and 5.2(c) show the optical micrographs of the crystals obtained from neat TIPS-pentacene solution on HfO_2/PVP and TIPS-pentacene:PS blend solution on HfO_2 deposited substrates. In the optical micrograph of TIPS-pentacene crystal obtained from blend solution, a distinct PS rich layer developed gradually through vertical phase separation can also be observed.

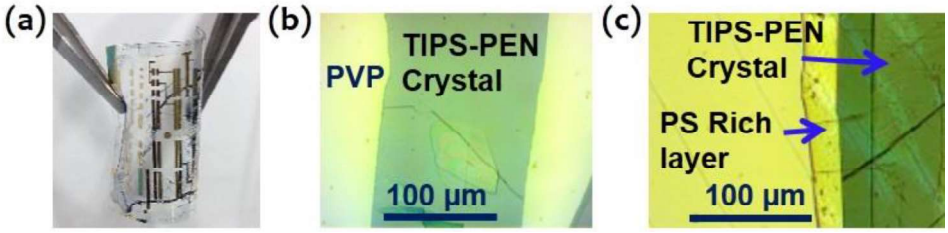

Figure 5.2: (a) Digital image of fabricated devices. Optical micrographs of semiconductor crystal obtained from neat TIPS-pentacene solution **(b),** and TIPS-pentacene:PS blend solution **(c).**

The PS rich layer was found to be uniformly present under the TIPS-pentacene crystals also which was confirmed by selectively etching TIPS-pentacene using n-hexane. Figure 5.3 shows optical micrographs of blend films before and after etching from n-hexane, where etching reveals the presence of a uniform PS layer beneath the TIPS-pentacene crystal.

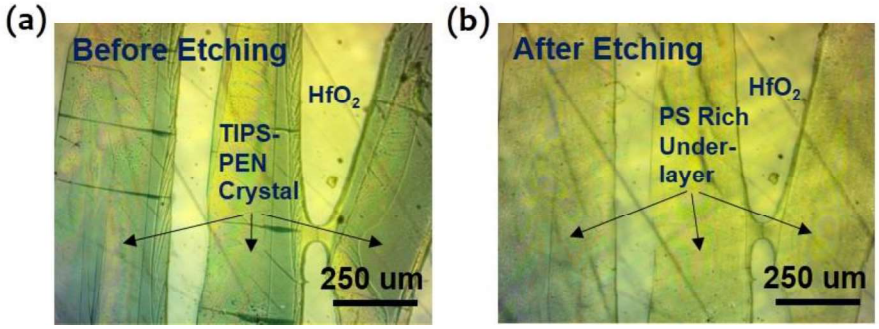

Figure 5.3: Optical micrographs of TIPS-pentacene:PS blend crystals before etching **(a),** and after etching from n-hexane **(b).**

Figure 5.4(a) and 5.4(b) show the AFM image of HfO_2 and PVP surfaces. Average surface roughness of HfO_2 was 5.1 Å, which was further improved by PVP (average roughness of 2.9 Å) providing an extremely smooth surface for semiconductor deposition. General terracing morphology of TIPS-pentacene crystals was observed for both cases, as shown in AFM images of figure 5.4(c) and 5.4(d), which indicate invariability of the surface morphology of TIPS-pentacene crystals on inclusion of polymer in the semiconductor solution. This is also in the agreement with the conclusions drawn earlier in chapter 4.

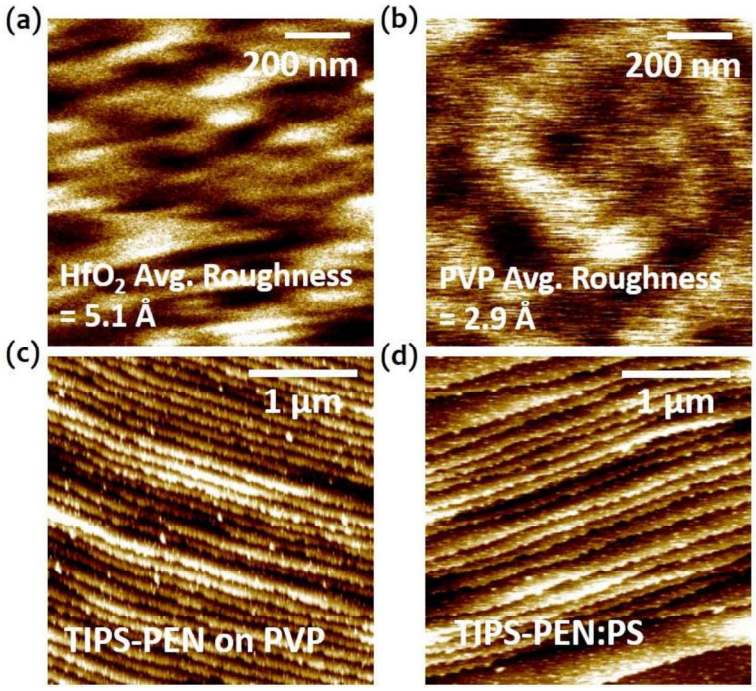

Figure 5.4: Surface morphology of HfO_2 **(a),** cross linked PVP **(b),** crystal obtained from the neat TIPS-pentacene solution **(c),** and TIPS-pentacene:PS blend solution **(d).**

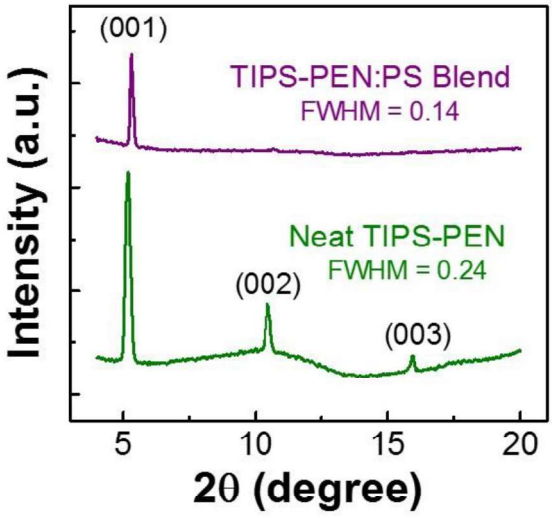

Figure 5.5: X-ray diffratograms for TIPS-Pentacene crystals obtained from neat TIPS-pentacene and TIPS-pentacene:PS blend solutions.

Figure 5.5 shows the X-ray diffractograms for TIPS-pentacene crystals obtained from both types of solutions. These X-ray diffractograms affirm high degree of crystallinity of the crystals obtained from both types of solutions. Figure suggests that crystal growth in the blend films occurs along a single and preferential orientation only, most probably due to PS chains acting as effective nucleation sites [Lee *et al.,* 2009]. The absence of any seed site in the neat TIPS-pentacene solution causes the crystal growth along multiple orientations, as evident from higher order *(00l)* peaks in diffractogram for neat TIPS-pentacene crystals. However, crystals in the blend devices grown along (001) orientation were found to be more crystalline with a full width at half of maximum (FWHM) of 0.14 in comparison to that of neat devices with FWHM of 0.24. As discussed in the chapter 4 before, incorporation of polymer may retard the solvent evaporation, which can be the cause of the higher degree of crystallinity of the final blend film.

5.3.2 Electrical Performance of flexible OFETs

Figure 5.6 shows output and transfer characteristics for representative neat TIPS-pentacene and TIPS-pentacene:PS blend devices. TIPS-pentacene:PS blend OFETs outperformed their neat counterparts with μ_{sat} of 0.44±0.25 $cm^2 V^{-1} s^{-1}$ (μ_{max} of 0.93 $cm^2 V^{-1} s^{-1}$). μ_{sat} for neat TIPS-pentacene OFETs was found to be 0.11±0.08 $cm^2 V^{-1} s^{-1}$ (μ_{max} of 0.23 $cm^2 V^{-1} s^{-1}$). In addition, high current on-off ratios of the order of 10^5 were obtained for both cases. Table 5.1 presents summary of various extracted device parameters for a set of 5 and 12 numbers of neat and blend devices respectively.

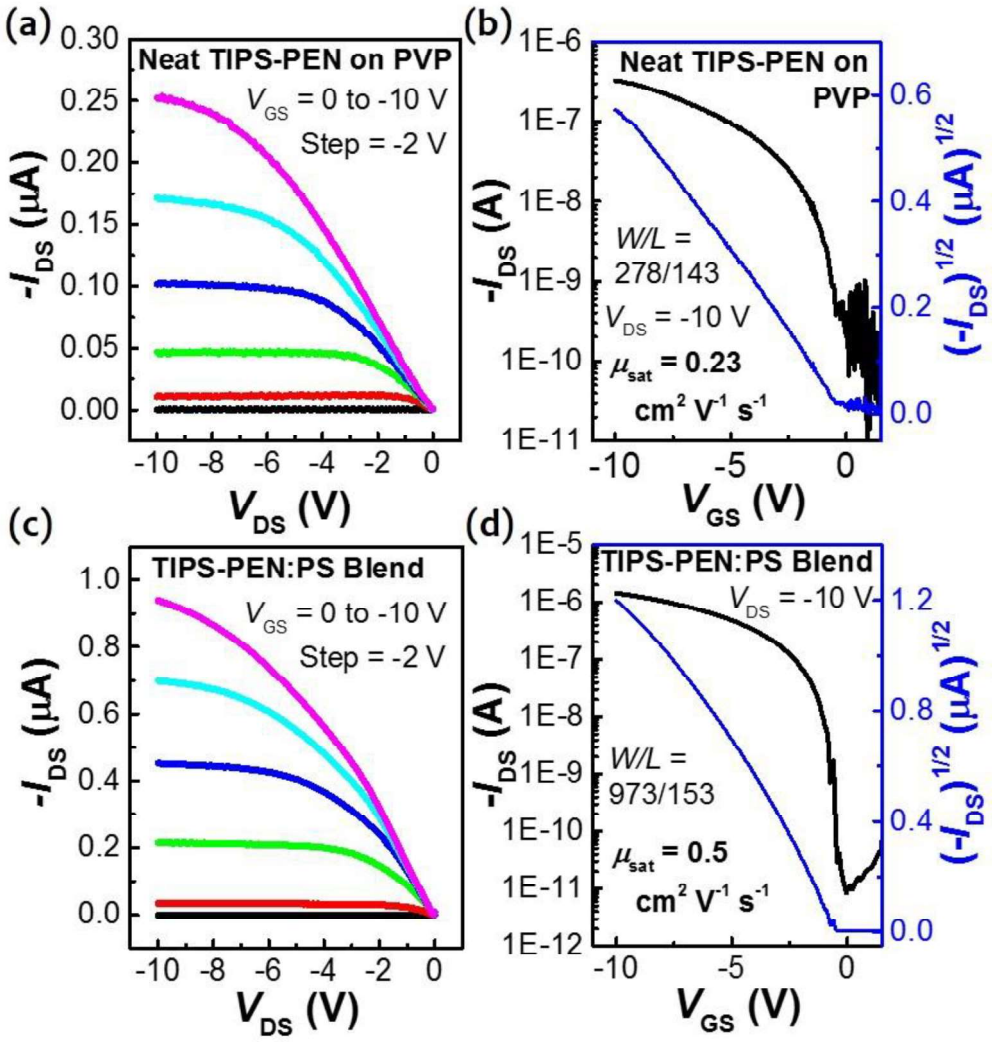

Figure 5.6: Output and transfer characteristics for a representative neat TIPS-pentacene **(a), (b)** and TIPS-pentacene:PS blend OFET **(c), (d).**

Table 5.1. Summary of the extracted electrical parameters for both type of OFETs.

Device	μ_{sat} ($cm^2 V^{-1} s^{-1}$)	μ_{max} ($cm^2 V^{-1} s^{-1}$)	V_{TH} (V)	I_{ON}/I_{OFF}	*SS* (V/dec.)	D_{it} (10^{12} $cm^{-2} eV^{-1}$)
Neat TIPS-PEN	0.11±0.08	0.23	0.08±0.3	~10^5	0.81±0.22	3.72±0.92
TIPS-PEN:PS	0.44±0.25	0.93	-0.3±0.19	~10^5	0.56±0.21	0.77±0.23

One of the observably distinct attribute of these OFETs is the lower voltage operation at -10 V in comparison to many of the reported flexible TIPS-pentacene based OFETs thus far [Yi *et al.*, 2012, Chung *et al.*, 2011]. Better performance in blend OFETs can be associated with the uniform and intimate quality of the semiconductor-polymer interface, which is developed gradually during vertical phase separation. During the process of phase separation, crystallization of a purer TIPS-pentacene film occurs at top (air-film) and bottom (film-substrate) interfaces, while a polymer-rich layer is developed in the middle of the two TIPS-pentacene layers [Jung *et al.*, 2010, Li *et al.*, 2011, Madec *et al.*, 2008]. A similar phenomenon has been already reported for the blend films of TIPS-pentacene and PαMS [Ohe *et al.*, 2008, Kang *et al.*, 2008]. The purer film of TIPS-pentacene at HfO_2 interface may also be the cause of high electrical performance [Kang *et al.*, 2008]. Alternatively, at the interface of top segregated TIPS-pentacene and middle PS rich layer, which acts as the functional dielectric-semiconductor interface in top contact devices, dipolar disorder is reduced and carrier localization takes place due to a less polar, low-k polystyrene, which reduces the broadening of density of states and ultimately the trap state density [Hulea *et al.*, 2006, Kalb *et al.*, 2010, Sworakowski, 1999, Veres *et al.*, 2003], as dicussed before in chapter 4 also. Another reason can be the ameliorated semiconductor morphology which is eventually developed at the dielectric-semiconductor interface during slow solvent evaporation in the drop cast method. The slow rate of solvent evaporation in the drop cast procedure is further decelerated by addition of the polymer, which subsequently promotes a better degree of molecular arrangement and therefore a higher degree of crystallinity. This was verified earlier through XRD studies, where TIPS-pentacene:polystyrene blend films have shown enhanced degree of crystallinity as compared to neat TIPS-pentacene films (Figure 5.5). All these events gradually aids in achieving a dielectric-semiconductor interface with highly uniform quality [Li *et al.*, 2011, Ohe *et al.*, 2008]. Superior conditions at the dielectric-semiconductor interface in blend OFETs can further be confirmed quantitatively by lower values of interface trap density (D_{it}) in comparison to neat TIPS-pentacene OFETs. D_{it} for blend OFETs was found to have a value of $(0.77\pm0.23) \times 10^{12}$ cm^{-2} eV^{-1} in comparison to $(3.72\pm0.92) \times 10^{12}$ cm^{-2} eV^{-1} for neat case. The fine quality of interface facilitates an efficient quality of charge-transport in the semiconducting film, close to the dielectric-semiconductor interface, which is reflected through performance of devices.

5.3.3 Bias-stress Stability

Figure 5.7 shows the normalized decay in I_{DS} for both types of OFETs under biasing conditions of $V_{GS} = V_{DS} = -10$ V. Duration of bias-stress was 40 minutes to 1 hr. Decrease in I_{DS} is because of trapping of charge carriers at various locations in the devices and subsequent V_{TH} shift. The major trapping of charge carriers can occur in the bulk of the semiconductor [Chang and Subramanian, 2006], at the dielectric-semiconductor interface [Street *et al.*, 2006] in the disordered regions of the semiconductor [Salleo *et al.*, 2005] and in the grain boundaries of the semiconductor [Tello *et al.*, 2008]. Blend OFETs exhibit lesser decay in I_{DS} (~4%) in comparison to neat devices with a much higher decay (~30%), which can be attributed to the uniform quality of dielectric-semiconductor interface developed gradually through vertical phase separation in contrast to relatively abrupt dielectric-semiconductor interface in the neat devices. In addition, the presence of hydroxyl groups on PVP chains, which act as electron trapping sites, further aggravates charge trapping on the dielectric-semiconductor interface in the neat devices leading to larger current decay.

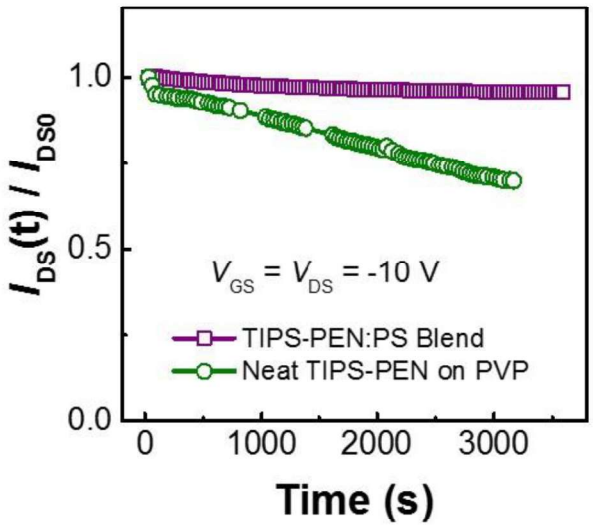

Figure 5.7: Bias stress induced decay in normalized drain current in TIPS-pentacene OFETs as a function of stress time at V_{DS} = -10 V, V_{GS} = -10 V.

5.4 CONCLUSIONS

In this chapter, two types of flexible solution processed OFETs, neat TIPS-pentacene on HfO_2/PVP dielectric and TIPS-pentacene:PS blends on HfO_2 dielectric, were examined for their electrical performance. With similar morphologies of TIPS-pentacene crystals in both cases, the crystalline quality of TIPS-pentacene was found to be higher in blend devices. Fine quality of dielectric-semiconductor interface and higher crystallinity of active layer lead to superior performance in blend devices as compared to their neat counterparts. Blend devices exhibited maximum field-effect mobility up to 0.93 $cm^2 V^{-1} s^{-1}$ with average of 0.44±0.25 $cm^2 V^{-1} s^{-1}$ compared to 0.11±0.08 $cm^2 V^{-1} s^{-1}$ for neat devices for -10 V operation. High current on-off ratios of the order 10^5 and near zero threshold voltages were obtained for both types of devices. In addition, blend devices demonstrated lesser levels of current decay than neat devices under effect of bias stress.

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