6
Electro-Mechanical Stability of Flexible OFETs

Along with high electrical performance and stability in flexible OFETs, high invariability in the device performance upon bending is also highly essential. Many applications of flexible electronics such as e-skin, e-nose and wearable sensing devices, involve bending of substrates carrying the devices. Under such practical conditions, behavior of high performance OFETs remains underexplored and literature lacks in reports on operational stability of high performance flexible OFETs under mechanical and electrical stress. In order to practically realize these applications of flexible electronics, a high electro-mechanical stability of the device performance is desired. Performance of an ideal electro-mechanical stable device should remain unaffected under the stress it is subjected to. In the previous chapter, flexible blend OFETs were found to show high performance and stability than their neat counterparts due to a high-quality dielectric-semiconductor interface. In this chapter, these blend OFETs have been selected for exploration of electro-mechanical stability with further reduced operating voltage of -5 V due to their inherent high performance. Outcomes discussed in this chapter have been recently published [Bharti *et al.*, 2016].

6.1 ELECTRO-MECHANICAL STABILITY

A high degree of mechanical stability is one of the highly sought after objectives of large-area flexible electronics for display and sensor applications. Such electronic systems should demonstrate high bendability (with bending radius of few millimetres) as well as extended abilities of rolling and creasing without loss in their electrical performance [Sekitani *et al.*, 2010]. Together with high electro-mechanical stability, devices should inherently exhibit excellent electrical performance. Such desired features mandate development of high performance devices with high stability, which can undergo high magnitude of strain (smaller bending radii) without compromise in electronic performance [Sekitani *et al.*, 2010]. However, for most of the cases, a degradation in device performance has been reported because of bending, which is the result of deteriorating changes at various locations in the device [Raghuwanshi et. al., 2016, Lakatos, 2000]. The resultant degradation in device performance is generally irreversible. Most trivial reasons for bending induced performance reduction include deformation of substrate films, rupture of contact electrodes or the gate electrode, degradation of the gate insulating layer, damage in the semiconductor layer, and deterioration in the uniformity of the dielectric-semiconductor interface [Sakai *et al.*, 2014]. Since these modifications in the devices may not be visible easily, it is difficult to determine the exact reason of performance degradation. In order to minimize the effects of bending and hence to obtain devices which are resistant to bending-induced degradation, it is highly imperative to enhance the uniformity of functional interfaces (dielectric-semiconductor, metal-semiconductor, substrate-dielectric, etc.). It is conceptually expected that a device with highly uniform quality of these interfaces will be the least affected by the damaging effects of mechanical strain.

The quality of the interface of the dielectric material and organic semiconductor is of vital significance, not only for electrical performance [Sun *et al.*, 2010, Zhang *et al.*, 2011], but also for operational stability of the device. In the previous chapter, between two types of flexible

OFETs, TIPS-pentacene:PS blend OFETs were found to outperform neat TIPS-pentacene OFETs. As concluded in chapter 4 and 5, process of vertical phase separation in TIPS-pentacene:PS blend OFETs causes formation of a high quality, defect free dielectric-semiconductor interface, which ultimately leads to inherent superior device performance as well as electrical stability in comparison to their neat counterparts. Such high performance blend OFETs with superior dielectric-semiconductor interface can be the ideal devices for applications requiring high bending stability. For this reason, blend devices are selected here for demonstrating high electro-mechanical stability. There are several reports on high performance blend OFETs with various semiconducting and polymeric materials [Shin *et al.*, 2013, Smith *et al.*, 2012, Jung *et al.*, 2010, Li *et al.*, 2011, Lee *et al.*, 2012, Min Hee *et al.*, 2012], however unfortunately operational stability is scarcely explored. Despite under-exploration of this aspect of device performance, operational stability of high performance OFETs in practical applications still remains a major concern.

In this chapter, the electro-mechanical stability in high performance, TIPS-pentacene:PS blend OFETs has been investigated. Here, blend OFETs are operated at further reduced voltages, without any compromise in the device performance. With an operating voltage of -5 V, devices exhibited high field-effect mobility up to 1.1 $cm^2 V^{-1} s^{-1}$ with an average of 0.5±0.3 $cm^2 V^{-1} s^{-1}$, low threshold voltage of -0.4±0.3 V, high on-off current ratios of ~10^5. Under the effect of constant and continuous mechanical strain corresponding to bending radius of 5 mm for duration of 2 days, very stable electrical characteristics have been obtained. Moreover, the effect of multiple cycles of compressive and tensile strain at bending radius of 5 mm has also been investigated. After 100 such cycles, devices still show stable electrical characteristics. Bias-stress experiments disclosed a very high characteristics trapping time of ~10^8 s which signifies very low degree of charge trapping at the dielectric-semiconductor interface in pristine devices. Levels of bias-stress induced current decay after subjecting the devices to a constant mechanical strain up to 2 days were similar to that for pristine devices; however, the decay was slightly higher after undergoing multiple cycles of consecutive stress and strain [Bharti *et al.*, 2016].

6.2 EXPERIMENTATION

TIPS-pentacene:PS blend devices were fabricated in top-contact bottom-gate configuration on indium tin oxide coated flexible polyethylene terephthalate substrates with HfO_2 gate dielectric. Fabrication procedure is similar to what is described earlier in the previous chapter. To examine the electro-mechanical stability, the devices were subjected to strain along the channel direction by bending the substrate with R_{bend} of ±5.0 mm (corresponding to ±1.27 % strain) with a rate of ±0.635 %/s. This kind of bending is graphically shown in Figure 6.1(a). Devices were also subjected to multiple cycles of tensile and compressive strain application. This strain cycle strategy is schematically illustrated in Figure 6.1(b). After each bending, devices were flattened for measurements. The strain on the device was calculated using the equation:

$$Strain(\%) = \frac{t_{sub}}{2R_{bend}} \times 100 \qquad (6.1)$$

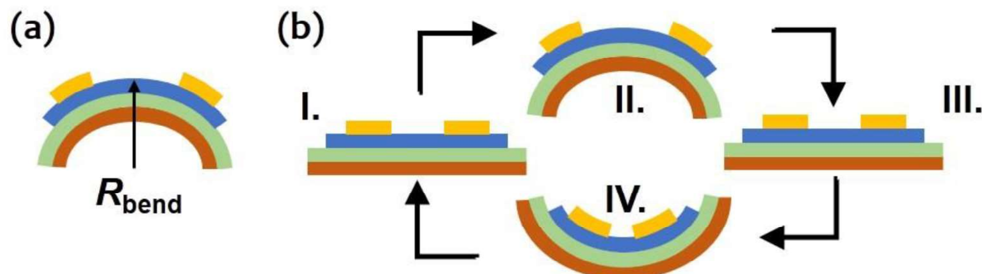

Figure 6.1: Strategy for application of tensile strain **(a),** and multiple cycles of tensile and compressive strain **(b).** A single cycle of strain application follows I.→II.→III.→IV.→I.

6.3 RESULTS & DISCUSSIONS

6.3.1 Characterization of Blend Crystallite

Figure 6.2(a) displays the surface morphology of a TIPS-pentacene crystal, which was found to demonstrate its usual terracing structure [Diao *et al.*, 2013, James *et al.*, 2011]. The optical micrographic image of a TIPS-pentacene crystal obtained from the blend solution is shown in Figure 6.2(b), where a PS rich layer formed gradually through the process of vertical phase separation can also be distinctively observed. To ascertain the thicknesses of phase separated layers, line profiles across the crystals were measured using a surface profilometer. Figure 6.2(c) plots the line profile along the solid line in Figure 6.2(b), which measures the average thickness of PS rich layer and TIPS-pentacene rich crystal to be 140±20 nm and 416±88 nm respectively (average of 7 points). Reason of the different thicknesses of PS rich layer and TIPS-pentacene crystals can be their different solidification and crystallization behaviors.

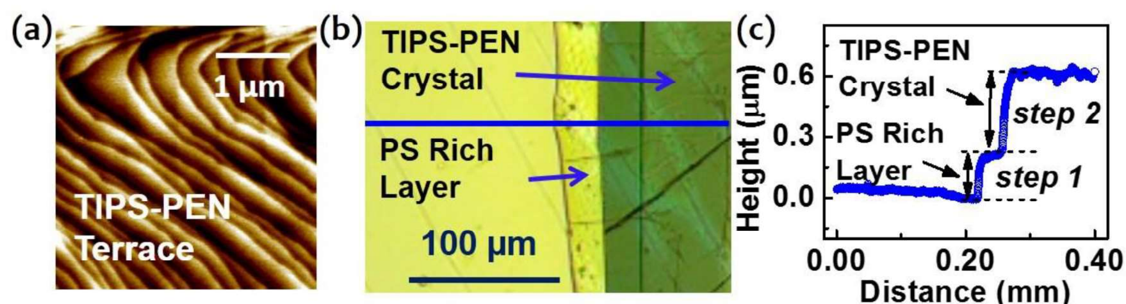

Figure 6.2: **(a)** AFM image of the TIPS-pentacene crystal obtained from the PS blend solution. **(b)** Optical micrograph of a TIPS-pentacene crystal revealing a distinct PS rich layer under the TIPS-pentacene crystal. **(c)** Line profile along the solid line in the optical micrograph. Thicknesses of the PS rich layer and TIPS-pentacene crystal were found to be 140±20 nm and 416±88 nm respectively.

6.3.2 Electrical Characterization of Flexible Low-Voltage Blend OFETs

Figure 6.3(a) and 6.3(b) show the output and transfer characteristics of a representative TIPS-pentacene:PS blend device. Such devices function well at a small operating voltage of -5 V with excellent p-channel behavior. In comparison to some of the previous reports where a large capacitance density, C_i was necessary for low voltage operation in OFETs, it is noteworthy that low voltage operation of blend devices is achieved here with a low value of C_i (i.e. 18.14±1.56 nF/cm^2 at 1 KHz). The average μ_{sat} obtained from a set of 20 devices was 0.5±0.3 cm^2 V^{-1} s^{-1} with maximum mobility of 1.1 cm^2 V^{-1} s^{-1}. Table 6.1 lists the values of major electrical parameters for blend devices. As per discussion earlier in the previous chapter, superior performance in the blend devices has been achieved because of the vertical phase separation, where a tri-layer structure of TIPS-pentacene/PS/TIPS-pentacene is formed during solvent evaporation.

Table 6.1. Summary of the electrical parameters for TIPS-pentacene:PS blend OFETs

μ_{sat} (cm^2 V^{-1} s^{-1})	μ_{max} (cm^2 V^{-1} s^{-1})	V_{TH} (V)	I_{ON}/I_{OFF}	SS (V/dec.)	D_{it} (10^{12} cm^{-2} eV^{-1})
0.5 ±0.3	1.1	-0.4 ±0.3	~10^5	0.31 ±0.19	1.26 ±0.84

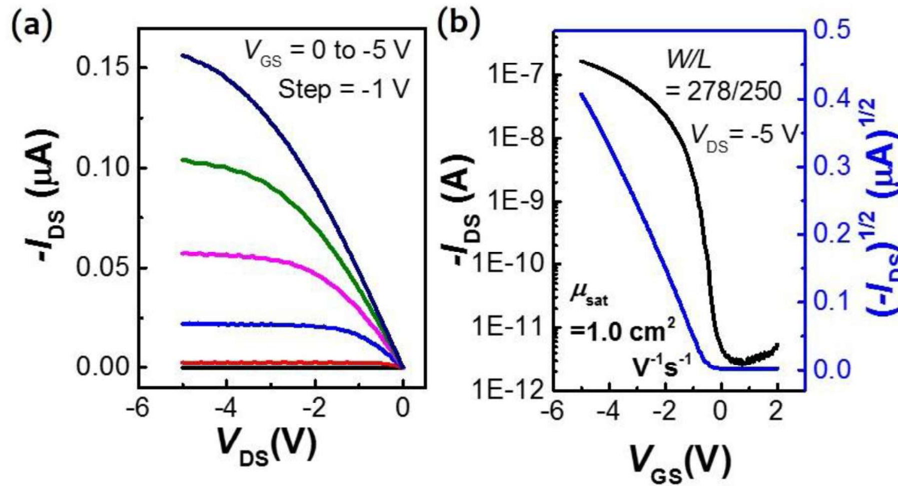

Figure 6.3: Output **(a)** and transfer **(b)** characteristics of a representative TIPS-pentacene:PS blend flexible OFET.

6.3.3 Electro-mechanical Stability of Blend OFETs

Figure 6.4(a) shows the variation in the transfer characteristics of a representative device under a constant magnitude of tensile strain corresponding to bending radius of 5 mm with increasing strain duration. A very little degradation was observed in the transfer characteristics of the device on bending it up to 2 days, which certainly affirms a high electrical stability upon bending. Figure 6.4(b) shows the effect of duration of strain on μ_{sat} and V_{TH} for a set of 5 devices. Major deterioration in the device parameters occurs at the initial strain application, after which these become relatively independent of the strain duration. This behavior can be directly associated with the variation in dielectric-semiconductor interfacial conditions [Raghuwanshi *et al.*, 2016, Raghuwanshi *et al.*, 2016]. Primary cause of this initial degradation can be the growth of micro-defects or micro-cracks and their propagation under applied strain [Leterrier *et al.*, 2010, Lewis, 2006]. Generation of defects/cracks and their propagation are complicatedly dependent on numerous factors like modulus contrast of the substrate and the film, crack length, interfacial adhesion, film cohesion and film thickness [Leterrier *et al.*, 2010, Lewis, 2006]. Any pre-existing defect in the inorganic HfO_2 layer may also expedite the deterioration. However, in TIPS-pentacene:PS blend devices, very little change is observed in mobility and threshold voltage on bending the devices up to 2 days, which certainly points out towards very high quality of dielectric-semiconductor interface, thus achieving high electrical stability upon bending.

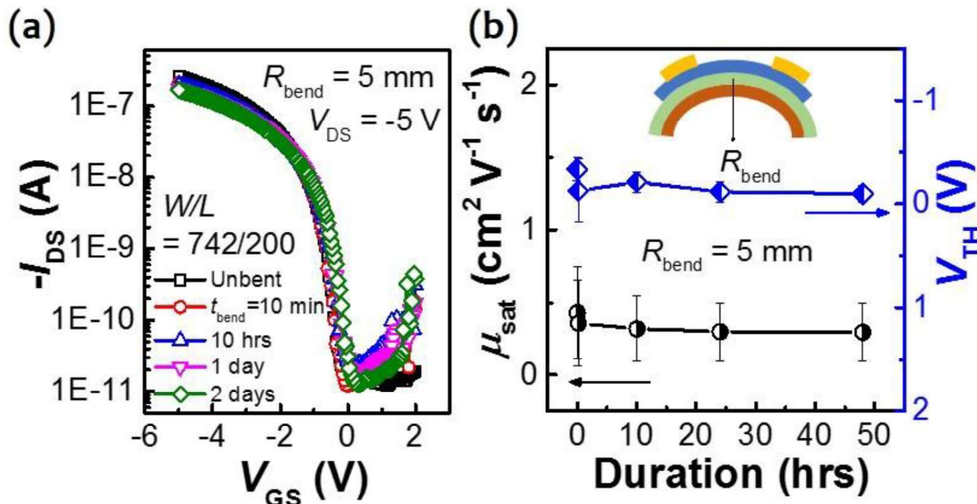

Figure 6.4: (a) Transfer characteristics of a representative device for strain duration varying from un-bent to 2 days. **(b)** Variation in mobility and threshold voltage with strain duration.

Further, the devices were subjected to multiple cycles of strain application. Each cycle consisted of a tensile and a compressive strain application at ±5mm bending radius (±1.27 % strain with a rate of ±0.635 %/s) for 5 sec each (depicted in Figure 6.1(b)). Figure 6.5(a) and 6.5(b) show the result for this study on logarithmic and linear scales respectively, where the exceptional electrical stability on the application of 100 such cycles can be noticed. After application of 100 such strain cycles, mobility of the representative device changed from 0.32 to 0.29 $cm^2\ V^{-1}\ s^{-1}$. All these outcomes signify the nearly stable quality of the dielectric-semiconductor interface under various consecutive strain applications. These minor variations in the performance indicate a high electromechanical stability in blend devices.

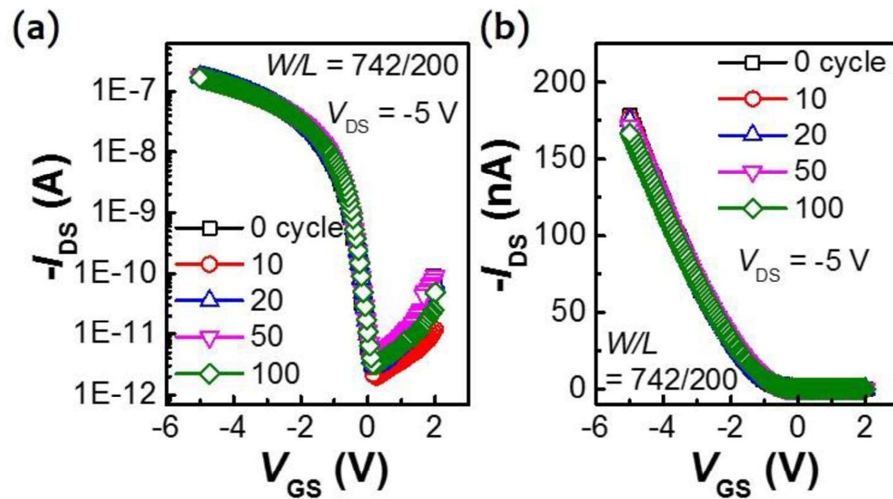

Figure 6.5: Transfer characteristics of device on logarithmic scale **(a)**, and linear scale **(b)** after undergoing multiple cycles of mechanical stress at R_{bend} of ±5 mm for a t_{bend} of 5 s.

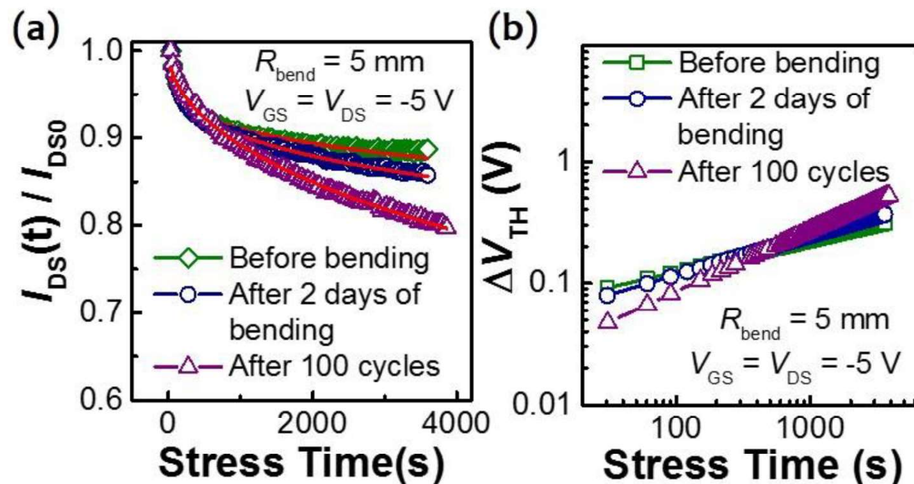

Figure 6.6: (a) Bias-stress induced decay in normalized drain current for various device conditions. **(b)** Shift in threshold voltage with stress time.

Figure 6.6(a) shows the bias stress induced decay in normalized drain current (I_{DS}) under constant stress conditions of V_{GS} = V_{DS} = -5 V for a duration of 1 hour for various device conditions. As discussed before in chapter 4 and 5, bias-stress causes trapping of charge carriers at several locations in the device, subsequently resulting in a shift in V_{TH} and decay in I_{DS}. From the Figure 6.6(a), it can be seen that bias-stress induced decay in the drain current for

pristine device is very low (~10 %), which is largely retained even after a long strain duration of 2 days. However, drain current decay increases to ~20 % after application of 100 strain cycles. With continuous application of strain for 2 days and multiple strain cycles, micro-defects or micro-cracks are generated and propagated in the semiconductor film and/or at the dielectric-semiconductor interface. These defects largely act as charge trapping locations, which ultimately lead to shift in V_{TH} and decay in I_{DS} as discussed before.

Mathematically, the normalized decay in I_{DS} in the saturation regime which is the ratio of the I_{DS} at time t and 0 s, can be expressed as following [Tiwari, Zhang, Potscavage and Kippelen, 2009],

$$\frac{I_{DS}(t)}{I_{DS}(0)} = \exp\left(-2\left\{\frac{t}{\tau}\right\}^{\beta}\right) \quad (6.2)$$

where β is a temperature dependent dispersion parameter which signifies the width of involved trap distribution. τ is the charge carrier relaxation time, a measure of characteristic trapping time of charge carriers. Values of β and τ have been extracted for various device conditions by fitting the experimental data of Figure 6.6(a) in (6.2) and also listed in Table 6.2.

Table 6.2: Extracted parameters from normalized I_{DS} decay for various device conditions

Device	*Β*	τ (s)
Pristine	0.263	1.11×10^{8}
2 day's strained	0.327	8.82×10^{6}
After 100 cycles	0.510	2.72×10^{5}

Larger value of τ indicates a lesser degree of charge trapping which leads to a lesser shift in threshold voltage (V_{TH}) [Zschieschang *et al.*, 2008]. From Table 6.2, it can be noticed that value of τ is decreased with subsequent strain applications, and larger values of shift in V_{TH} are expected. Alternatively, shift in V_{TH}, at each stress duration can be calculated using extracted values of β and τ in a stretched exponential function which was proposed originally by Libsch and Kanicki [Libsch and Kanicki, 1993]. The expression is as following,

$$|\Delta V_{TH}(\mathrm{t})| = |V_{GS} - V_{TH0}|\left[1 - \exp\left\{-\left(\frac{t}{\tau}\right)^{\beta}\right\}\right] \quad (6.3)$$

where V_{GS}-V_{TH0} is the effective voltage drop across gate and V_{TH0} is the initial threshold voltage at t = 0 s. Using (6.3), V_{TH} shifts with stress duration have been calculated and plotted in Figure 6.6(b) for various device conditions. From the Figure, it can be observed that shifts occurring in V_{TH} are small and have magnitudes of ~0.3 V, 0.4 V and 0.5 V for an unstrained device, the device strained for 2 days and the device undergone 100 cycles strain application respectively after 1 hour of bias-stress. It is interesting to note that the shift in V_{TH} increased slightly from 0.3 V to 0.5 V, even after 2 days of continuous mechanical strain application and undergoing multiple strain cycles, which certainly indicates that the quality of the dielectric-semiconductor interface is not deteriorated considerably even after undergoing consecutive strain applications.

6.4 CONCLUSIONS

TIPS-pentacene:PS blend flexible OFETs fabricated by a simple drop cast procedure and showing excellent device performance at lower operating voltages, were investigated for their performance reliability under joint effects of mechanical strain and electrical stress. High

mobility values up to 1.1 $cm^2 V^{-1} s^{-1}$, low threshold voltages, and high current on-off ratios ~10^5 were achieved while operating at -5 V. This outstanding device performance can be ascribed to uniform quality of dielectric-semiconductor interface in these devices. These devices exhibited high stability and largely unaffected electrical performance under the consecutive effects of continuous mechanical strain for 2 days and 100 sequential cycles of tensile-compressive strain. Under the effects of bias-stress, a low I_{DS} decay of ~10% was obtained with very large trapping time of ~10^8 s, and resulting threshold voltage shift of 0.3 V. Similar levels of bias-stress induced decay in the drain current were maintained after 2 days of tensile strain however drain current decay was increased to ~20% after 100 strain cycles. Nonetheless, the resulting shift in threshold voltage was still small (~0.5 V), which confirmed a high overall electro-mechanical stability in TIPS-pentacene:PS blend devices.

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