5
Electrical and Impedance characterization of sol-gel prepared CZTS thin film solar cell

5.1 Introduction

This chapter focuses on the details of fabrication of Al:ZnO/ZnO/CdS/CZTS/Mo/Glass heterostructure solar cell device structure. Structural, morphological and optical properties of CZTS absorber layer prepared using sol-gel spin coating are investigated and is implemented in the CZTS device structure with other partner layers to fabricate the complete solar cell. The open circuit voltage decay (OCVD) and capacitance voltage characteristics of the fabricated cell is investigated to determine the minority carrier life time and carrier concentration at the bulk CZTS. Solar cell impedance characterization has been performed and several equivalent circuits have been tried to understand the physics behind the solar performance.

5.2 Experimental details

CZTS layer has been synthesized using sol-gel spin coating technique that is optimized for uniform large area synthesis of the film [G. K. Gupta & Dixit, 2017]. In brief, sol for spin coating has been prepared in 2-methoxyethanol by dissolving copper (II) chloride dehydrate, anhydrous zinc chloride, tin (II) chloride and thiourea precursors in 2: 1.2: 1: 8 atomic ratio as a source of Cu, Zn, Sn and S elements in CZTS, respectively. The excess atomic zinc concentration has been intentionally considered to get good photovoltaic response [T. J. Huang, Yin, Qi, & Gong, 2014]. The sol thus prepared has been used for spin coating the film on SLG and Mo coated SLG substrate. The spinning of sol and the drying of deposited film is done at 3500 rpm and 300 °C, respectively. The drying of spin coated film is done for 5 minutes on the hot plate, followed by a natural cooling. This spinning and drying of film is repeated several times to get the desired thickness. The CZTS thin film thus prepared is subjected to final annealing treatment in a tubular furnace in presence of 5% H_2S + Ar gaseous environment. The temperature profile adopted during the annealing process is shown in **Figure 5.1 (a).** At the beginning slower heating rate of 5 °C/ min is opted up to 200 °C to provide sufficient time for alloying of the constituent elements. After that a fast heating rate of 10 °C/min is maintained up to 550 °C to minimize the loss of volatile constituents from the film. The film is kept at 550 °C for 30 min and finally cooled down naturally at room temperature to achieve the kesterite CZTS phase.

CZTS solar cell has been fabricated on 1 inch x 1 inch molybdenum (~ 1.5 μm thick) coated SLG substrate. CdS buffer layer of ~ 50 ± 20 nm thickness has been deposited on the top of CZTS absorber using chemical bath deposition, as described in **section 3.3.** An intrinsic ZnO and aluminum doped ZnO (Al:ZnO/AZO) films are deposited using RF and DC sputtering to form a bilayer window, respectively as described in **section 3.4.** The thickness of i-ZnO and Al:ZnO layer are kept ~80 ± 20 nm and ~ 1 μm, respectively. The schematic representation of the fabricated CZTS solar cell device structure is shown in **Figure 5.1 (b). A** relatively higher thickness of Al:ZnO layer is opted to the better top electrode electrical conductivity. Finally, the fabricated device structure is scribed into smaller 3 mm x 3 mm solar cell structures to avoid any

necessity of metallic grid contact on the top of Al:ZnO layer, which is usually integrated for efficient current collection.

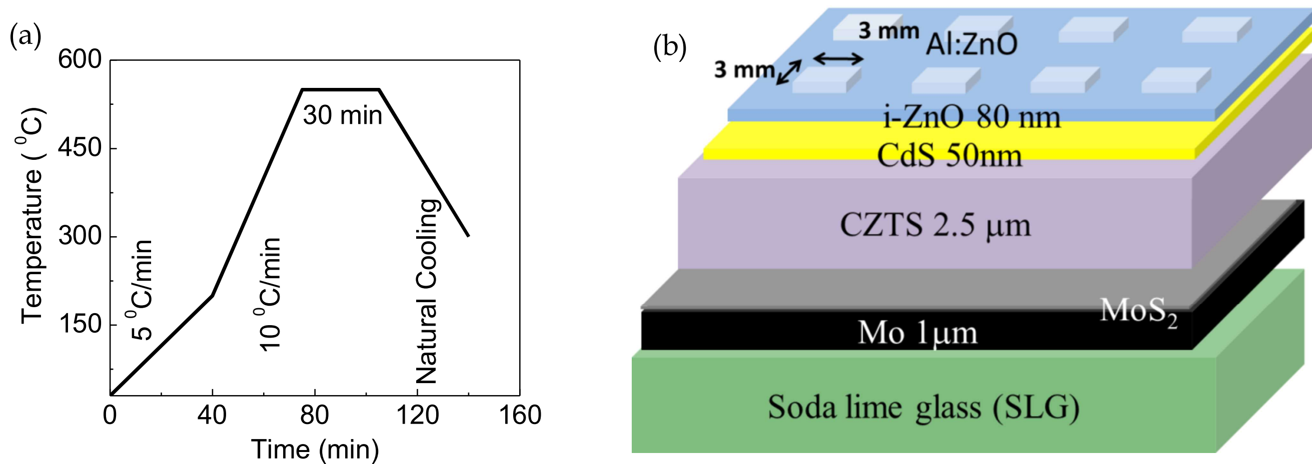


Figure 5.1 (a) Temperature profile used for final annealing of CZTS thin film under 5%H_2S+Ar gaseous environment (b) schematic representation of stacked multilayer (Al:ZnO/ZnO/CdS/CZTS/Mo/SLG) solar cell heterostructure with 3 mm x 3 mm area scribed for smaller solar cell structures.

5.3 Result and discussion

5.3.1 Structural and microstructural characterization

Structural and microstructural characteristics of the synthesized CZTS thin film are investigated using X-ray diffraction (XRD) pattern. XRD data is plotted along with the reference peaks of kesterite CZTS, taken from the reference data ICDD PDF # 260575 and is shown in **Figure 5.2 (a)** for CZTS grown over SLG substrate. **Figure 5.2 (b)** shows the XRD pattern of CZTS grown over Mo coated SLG substrate. The obtained XRD pattern is well in agreement with the reference ICDD PDF # 260575 and suggests formation of CZTS in kesterite crystallographic phase.

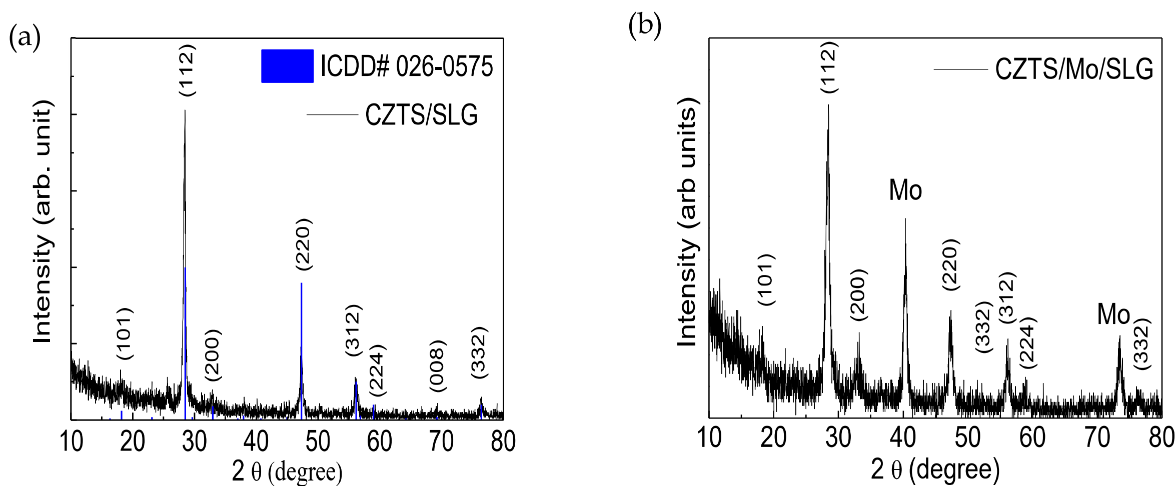


Figure 5.2 XRD pattern of the post annealed CZTS thin films on (a) SLG substrate (CZTS/SLG), with reference kesterite CZTS phase (ICDD# 026-0575) (b) Mo/SLG substrate (CZTS/Mo/SLG)

Table 5.1 Crystallographic data of CZTS thin film obtained from the XRD measurement.

Samples	<h k l>	2θ (degree) (observed)	FWHM (degree)	d_{exp} (Å)	Strain ε ($x10^{-3}$)	Grain Size D (nm)	Average grain size (nm)	Dislocation density δ (lines m^{-2})	Lattice parameter (a = b, and c), Measured (Å)
CZTS	<112>	28.46	0.385	3.133	6.62	22.23	24.37 ± 6	1.683 ± 0.0006 $x10^{15}$	a=b= 5.427
	<220>	47.32	0.395	1.919	3.93	22.93			c= 10.848
	<312>	56.22	0.428	1.635	3.49	21.97			c/2a=0.9994
	<332>	76.48	0.348	1.244	1.92	30.35			

These XRD patterns confirm the formation of polycrystalline film with four major diffraction peaks observed at 28.46°, 47.32°, 56.22° and 76.48°; correspond to (112), (220), (312) and (332) diffraction planes of kesterite CZTS, respectively. These CZTS films are relatively more textured along (112) direction. The calculated lattice parameters, grain size, dislocation density and strain are summarized in **Table 5.1**. Very low strain of the order of ~10^{-3}, is observed due to large thickness of CZTS film. Microstructural and compositional measurements are done using scanning electron microscopy (SEM) and energy dispersive X-ray (EDX) measurements, respectively. The surface SEM micrograph, **Figure 5.3 (a),** shows void free, uniform and smooth granular growth of CZTS thin film. The elemental composition shown in the inset of **Figure 5.3 (a)** represents slightly Zn rich and Cu poor stoichiometry which is considered suitable for high performing CZTS solar cell devices.

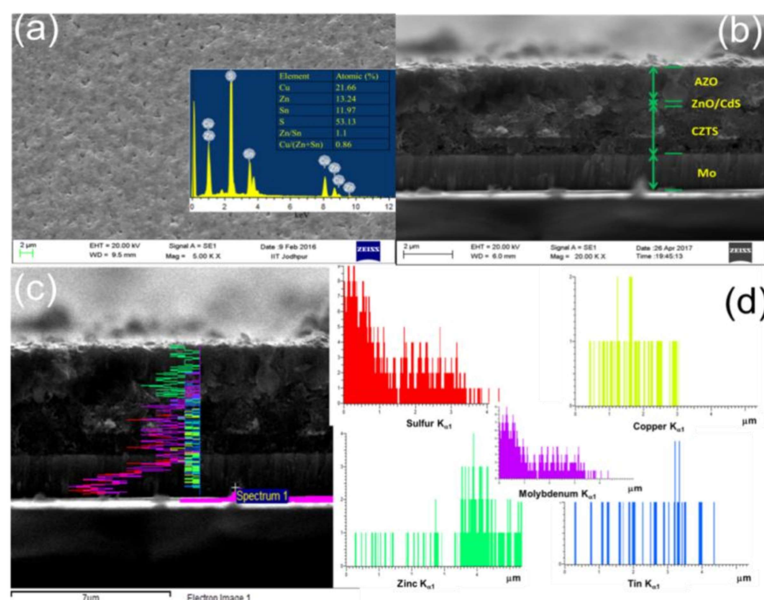


Figure 5.3 Scanning electron micrograph of (a) CZTS thin film over Mo coated SLG substrate, (inset showing atomic fractions obtained through EDAX measurement); (b) cross sectional micrograph of stacked (AZO/ZnO/CdS/CZTS/Mo/SLG) device structure; (c) Cross sectional line scan showing elemental distribution across the layers; and (d) respective elemental distribution across the layers

The cross-sectional micrograph is shown in **Figure 5.3 (b)**, illustrating the stacks of different layers for AZO/i-ZnO/CdS/CZTS/Mo/SLG device, as marked for clarity. The sputter deposited Mo thin film on SLG substrate showed columnar growth with thickness ~ 1.5 µm as observed in the cross sectional micrograph **Figure 5.3 (b)**. The Cross-sectional SEM micrograph substantiate the growth of uniform and well adhered CZTS film on the top of ~ 1.5 mm thick Mo coated on SLG substrate. The columnar growth of Mo is clearly visible in the cross sectional micrograph. However no signature of interfacial MoS_2 layer is seen, which is probable during the sulfurization of CZTS film. The formation of a thin MoS_2 layer can be inferred from the observed broadening near (200) peak. This broadening is usually attributed to the formation of MoS_2 layer at CZTS and Mo interface [Shin et al., 2013][Cui et al., 2016]. A thin MoS_2 layer at the interface of CZTS and Mo provides added advantages of strong CZTS adherence layer on Mo coated SLG substrate [Shin et al., 2013][Cui et al., 2016]. Cross-sectional elemental line scan on the fabricated device structure shown in **Figure 5.3 (d)** suggests the significant presence of sulfur at CZTS/Mo interface. However, it is very difficult to distinguish MoS_2 layer using EDX as the energy corresponding to characteristic Kα peak of sulfur (2.307 keV) is nearly equal to the energy corresponding to Lα peak (2.293 keV) of molybdenum. The cross-sectional micrograph of the CZTS device shown in **Figure 5.3 (b)** also explains that CZTS absorber thickness is ~ 2.5 ± 0.2 µm, showing dense structure with larger grains. Additionally, some voids can also be observed in the cross sectional micrograph of CZTS layer, which may lead to the poor electrical response. CdS and i-ZnO layer are not clearly visible in the cross sectional micrograph because of their lower thickness of CdS layer ~ 50 nm and due to the inability to distinguish i-ZnO layer with top Al:ZnO layer, respectively. Relatively thicker Al:ZnO layer is clearly visible in the cross sectional micrograph which is intentionally made to get good electrical conductivity.

5.3.2 Optical characterization

The optical properties are measured diffuse reflectance analysis (DRA) measurements in the wavelength range 200 nm to 900 nm for the prepared CZTS thin film over SLG substrate. The spectral absorbance of the prepared CZTS film is calculated using Kubelka –Munk model which is used in the Tauc relation to find the direct band gap as discussed earlier in **section 4.4**. The intercept of extrapolated linear region of the Tauc plot in the energy axis as shown in **Figure 5.4** suggest a direct optical band gap of ~ 1.5 eV for the prepared CZTS thin film.

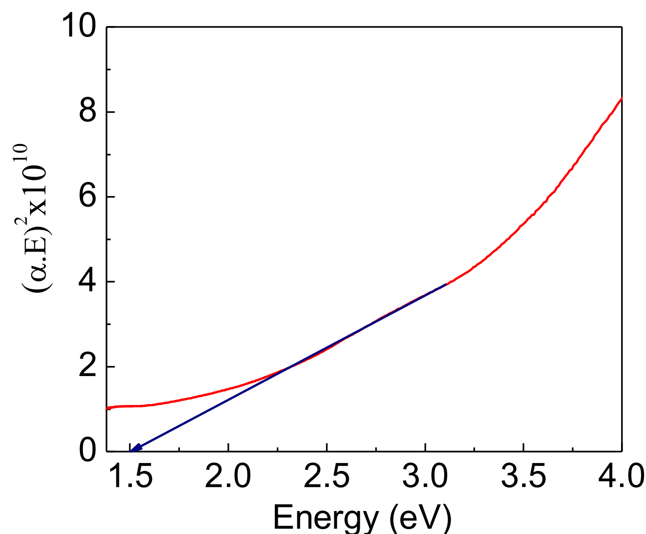


Figure 5.4 $(\alpha.E)^2$ versus energy E (eV) curve for CZTS/SLG thin films with an arrow showing the extrapolated linear region of the curve

5.3.3 Current –Voltage characteristics of CZTS device

Current voltage (*I-V*) characteristics of the fabricated CZTS solar cell measured under dark and under 1 Sun illumination are shown in **Figure 5.5 (a).** Series and shunt resistances are calculated at zero voltage and zero current condition of the illuminated I-V characteristics. The obtained device parameters are listed in the inset of **Figure 5.5 (a)**. Solar cell efficiency on similar set of devices has been measured and efficiency ~ 1.1% ± 0.2% is recorded. The reverse saturation current density and ideality factor are calculated by fitting the dark current characteristics of CZTS solar cell with diode equivalent circuit of solar cell as discussed in **section 2.4** and are summarized in **Figure 5.5 (b).** Different slopes observed in the dark current characteristics substantiate the variation of ideality factor with applied bias voltage. The measured reverse saturation current density and the ideality factor in low bias region (J_{01}, n_1), V < 0.45 V and high bias region (J_{02}, n_2), V > 0.45 V are (8 x10^{-6} A/cm^2, 2.7) and (1.27 x10^{-3} A, 12.4), respectively. The relatively large ideality factor explains the presence of large recombination in the device. Further a very large value of ideality factor ~ 12.4 observed at high applied bias governs the accelerated carrier recombination due to large carrier injection and interface recombination present in such heterostructure device.

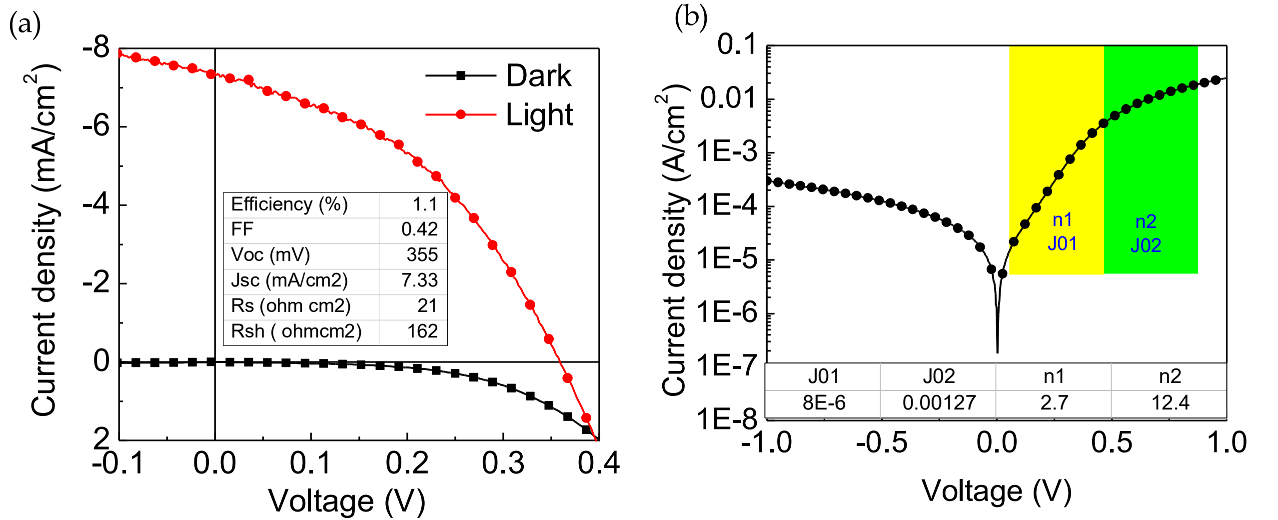


Figure 5.5 (a) Current density versus voltage (J - V) characteristics under dark and under 1 sun illumination conditions with inset showing device parameters (b) dark current-voltage characteristics for Al:ZnO/ZnO/CdS/CZTS/Mo/SLG solar cells and Open Circuit Voltage Decay analysis

Open circuit voltage decay (OCVD) data is measured using PGSTAT302N AUTOLAB having bandwidth 1 MHz and equipped with fast chrono-potentiometry option for these fabricated CZTS solar cells. A high forward current is passed across the device to ensure high level carrier injection and then the device is abruptly open circuited. Under high level injection, the minority carrier electron concentration in CZTS is quite large as compared to its thermal equilibrium value. Once device is open circuited, these minority carrier diffuses through the bulk of CZTS and recombine. The minority carrier life time 'τ' is related to the OCVD rate (dV_{OC}/dt) as

$$\tau = \frac{nk_BT}{q\left(\frac{1}{dV_{oc}/_{dt}}\right)} \quad (5.1)$$

where n is ideality factor, q is electronic charge, k_B is Boltzmann constant and *T* is temperature in Kelvin [Schroder, 2005]. The observed OCVD curve shown in **Figure 5.6** for the CZTS device shows exponential decay characteristics and can be well explained by the exponential fit using equation below [Mahan, Ekstedt, Frank, & Kaplow, 1979]

$$V_{oc}(t) = \frac{kT}{q}\left[\exp\left(\frac{qV_0}{k_BT} - 1\right)\right]\exp\left(\frac{-t}{\tau}\right) \quad (5.2)$$

where V_0 is the open circuit voltage at the termination of excitation. The minority carrier life time is estimated from the exponential fit of OCVD curve and is ~ 23 μsec in these photovoltaic devices. This obtained minority carrier life time value is much lower than previously reported values by Patel et al. [Patel, Mukhopadhyay, & Ray, 2013] for the same system, but relatively in agreement with other reported life time values measured using the same OCVD process [Milan Tapajna, Jaroslav Pjencak Andrej Vrbicky, Ladislav Harmatha, 2004].

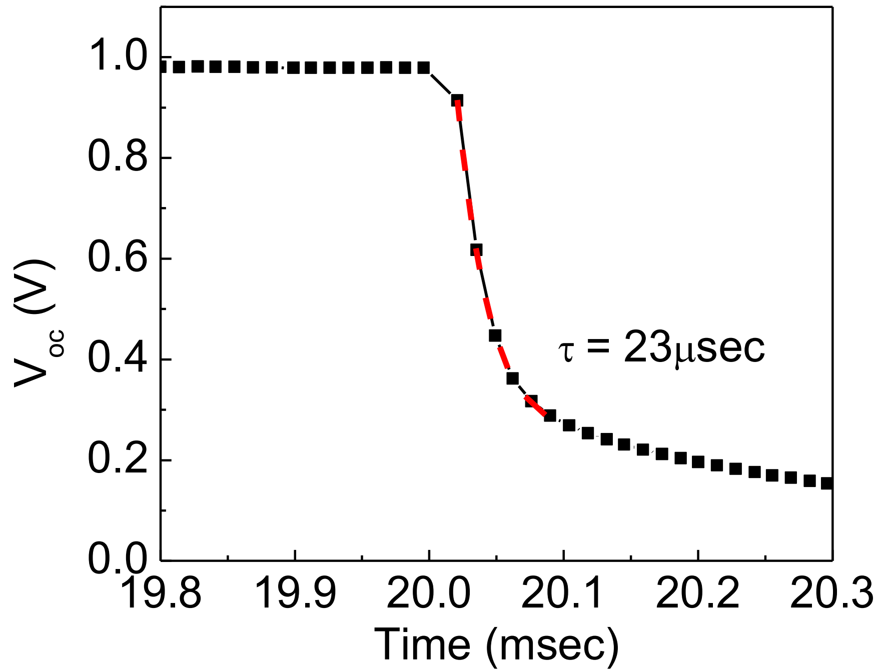


Figure 5.6 (a) Open circuit voltage decay (OCVD) curve for the CZTS heterostructure device

5.3.4 Capacitance voltage (C-V) characteristics and Mott-Schottkey analysis

The capacitance of the fabricated CZTS heterostructure device is measured at different frequencies and under a range of applied DC bias voltage. The resulting curve from this C-V measurement is shown in **Figure 5.7 (a)**.

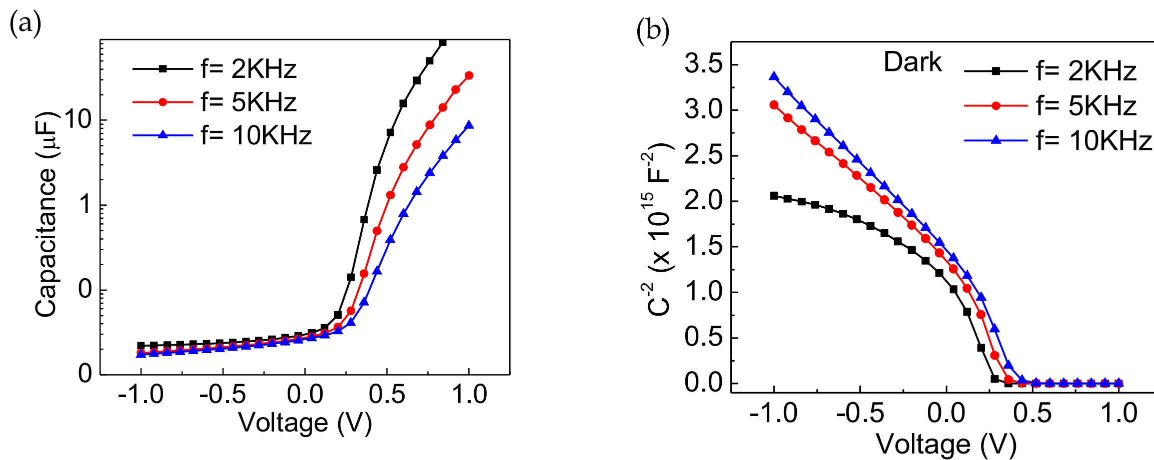


Figure 5.7 Capacitance - voltage characteristics (a) and Mott-Schottky plots (b) for Al:ZnO/ZnO/CdS/CZTS/Mo/SLG solar cell, measured at different frequencies

The total capacitance comprised of depletion and the diffusion capacitance for CZTS heterostructure device. The diffusion capacitance of the device is dominated at higher forward bias potential. We observed that the total capacitance of the device decreases with increasing frequency at a fixed polarization and increases exponentially at fixed frequency with increasing polarization potential as shown in **Figure 5.7**. The observed lowering in device capacitance with increase in frequency is due to the insensitiveness of absorber traps, that do not contribute at high frequencies, thereby reducing the effective charge and thus the device capacitance (C = Q/V). The measured capacitance-voltage characteristics are used to derive Mott-Schottkey (MS) plots i.e. the inverse square capacitance with respect to voltage plot at fixed frequency. These are shown in **Figure 5.7 (b).** The selection of an operating frequency (ω)is quite crucial for the Mott-Schottkey analysis and it should be small enough to satisfy the condition Rs << 1/ωC so that the resistance of bulk material (Rs) does not contribute to the measurement [Zekry, Abdel-Naby, Ragaie, & El Akkad, 1993]. Relatively high frequency is selected for MS analysis to avoid any low frequency dispersion. The MS plot for the CZTS device shown in **Figure 5.7 (b)** shows negative slope in the considered voltage range with nearly equivalent slope at different applied frequencies. However, the intercept of extrapolated linear region of MS curve at $1/C^2 = 0$ differs significantly at different measurement frequencies. This slight deviation in the observed slope at different operating frequency is possibly due to the localized deep states present in the absorber material which do not contribute at higher frequencies. The observed deviation in the point of intersection of the extrapolated linear region of MS plot substantiates the presence of back contact barrier and is related to the change in depletion width of back contact junction at different frequencies [Ge, Chu, Yan, Jiang, & Yang, 2015]. This observation also suggests that the back contact is not purely ohmic in this CZTS heterostructure and has Schottkey junction characteristics.

For an abrupt heterojunction, the acceptor defect concentration (N_a) in p-type CZTS absorber, and flat band potential (V_{fb}) can be obtained from the following expression [Fernandes et al., 2013],

$$\frac{A^2}{C^2} = \left[\frac{2}{q\varepsilon_0\varepsilon_{CdS}\varepsilon_{CZTS}}\right]\left[\frac{N_d\varepsilon_{CdS}+N_a\varepsilon_{CZTS}}{N_aN_d}\right]\left(V_{fb}-V\right) \tag{5.3}$$

where A is the area of the junction, q is electronic charge, ε_0 is permittivity of vacuum, ε_{CdS} is relative permittivity of CdS, ε_{CZTS} is relative permittivity of CZTS, N_d is total n-region ionized donor defect concentration. This expression for an n^+-p hetero-junction can be further simplified into

$$\frac{A^2}{C^2} = \left[\frac{2}{q\varepsilon_0\varepsilon_{CZTS}N_a}\right]\left(V_{fb}-V\right) \tag{5.4}$$

which is used to estimate the effective acceptor carrier concentration in CZTS absorber materials. The value of acceptor carrier concentrations is ~5.8×10^{17} cm^{-3} for CZTS with dielectric constant ~ 6.95 [Ito, 2015]. The calculated depletion width $W_{dep} = {}^{\varepsilon_0\varepsilon_{CZTS}}/_{C_{dep}}$ is ~ 20.5 nm for the investigated CZTS device.

5.3.5 Impedance Spectroscopy analysis

Impedance spectroscopy characterization of the fabricated CZTS solar cell is carried out and corresponding Nyquist plots are shown in **Figure 5.8**. The Nyquist plot obtained from the impedance data is fitted with resister capacitor (RC) equivalent circuit combinations. The equivalent circuits are shown in the inset of respective Nyquist plots **Figure 5.8 (a, b, c)**. The error in the measured and the simulated impedance are presented alongside the right panel of **Figure 5.8 (d, e, f)**.

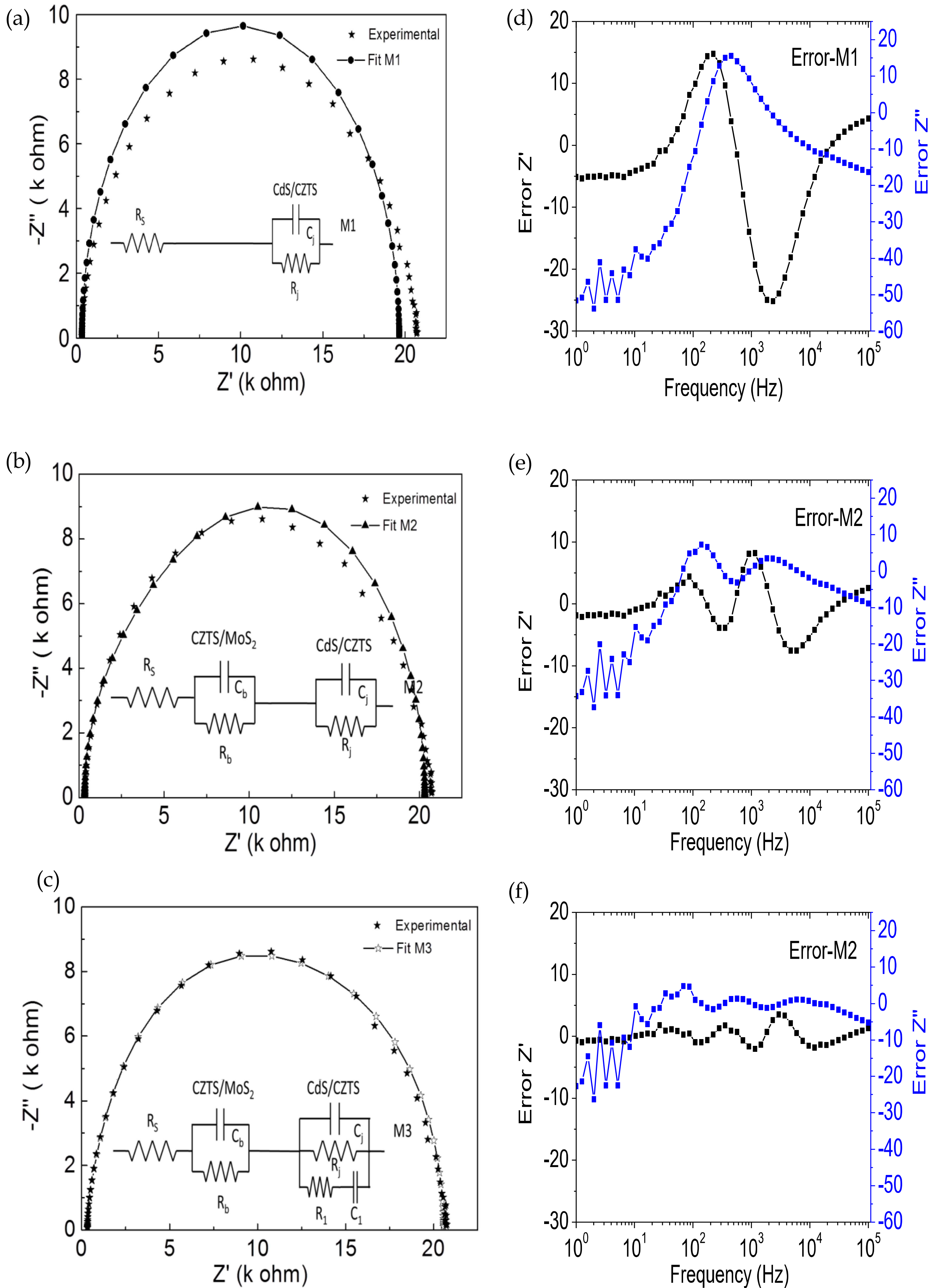
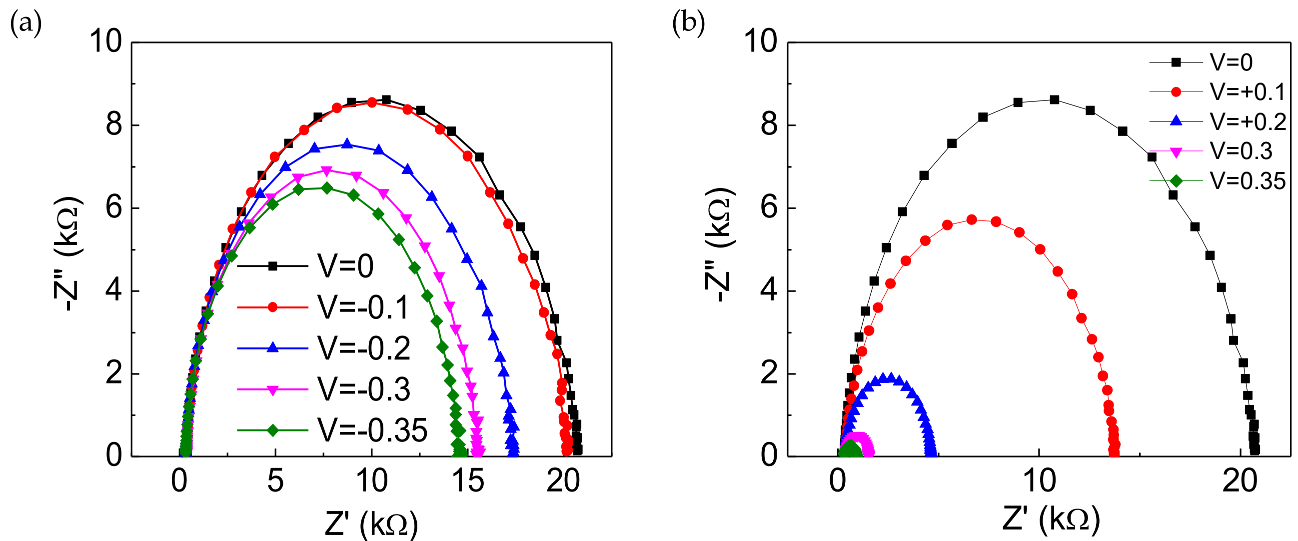


Figure 5.8 (a) Impedance spectrograph for Al:ZnO/ZnO/CdS/CZTS/Mo/SLG solar cell with three different equivalent circuit models M1,M2 and M3, as explained in (a, b, c) and corresponding error in (d, e, f), where M3 corresponds to the best fit to the measured experimental impedance spectrograph.

The obtained semicircular characteristic of the Nyquist plot substantiates the presence of space charge capacitance in the CZTS solar cell. The simplest circuit that can characterize such device is a resistance (Rs) in series with resistance capacitance loop (Rj - Cj). This circuit is shown in the inset of **Figure 5.8 (a)** and named as M1 for further use. In M1, Rs includes resistances due to all the contact and bulk material and the parallel resistance capacitance loop (Rj - Cj) describes the CdS/CZTS heterojunction. The simulated circuit fit using M1 shows large deviation in the intermediate frequency range, as can be inferred clearly from the respective right panel, **Figure 5.8 (d).** This observed deviation in the simulated circuit fitting may be attributed to the non-ohmic back contacts between CZTS and Mo layers. To account the back contact contribution resistance-capacitance loop (Rb - Cb) is added in series with circuit M1 as shown in the inset of **Figure 5.8 (b)** and named it M2 hereafter. This equivalent circuit fitting includes the contribution of non-ohmic back contact which is supported by the capacitance voltage characteristics of the device. The observed deviation in the measured and simulated Nyquist plot using M2 is lower as compared to that of M1. To further improve the circuit fitting a series resistance capacitance (R1 - C1) combination is included in parallel with Rj - Cj in circuit M3 to account for the inhomogeneity and the presence of defect states at CdS/CZTS heterojunction interface as shown in the inset of **Figure 5.8 (c)**. The circuit fitting results suggest that M3 provides the best fit to the experimental data with the maximum error of ~2% whereas error with M1 and M2 equivalent circuit fitting is much larger ~8% and ~ 25%, respectively.

The impedance characteristics of the fabricated CZTS solar cell structure are also carried out at different bias potentials. The impedance measurements for different forward bias potentials are shown in **Figure 5.9 (a)** and for reverse bias potentials are shown in **Figure 5.9 (b).** The entire impedance curve obtained under different bias potential is fitted with equivalent circuit M3. The extracted equivalent circuit parameters obtained at different bias potentials are summarized in **Figure 5.9 (d, e)**. The diameter of the semicircle in the obtained Nyquist plots shrinks with increase in magnitude of bias voltage in both reverse and forward bias conditions and is more pronounced in forward bias condition. For clarity, a zoomed impedance plot is shown in **Figure 5.9 (c)**. The observed shrinkage in the diameter with increase in applied potential is in consistent with the increased carrier concentration of the CZTS device, improving the conductivity and thus reducing the impedance.



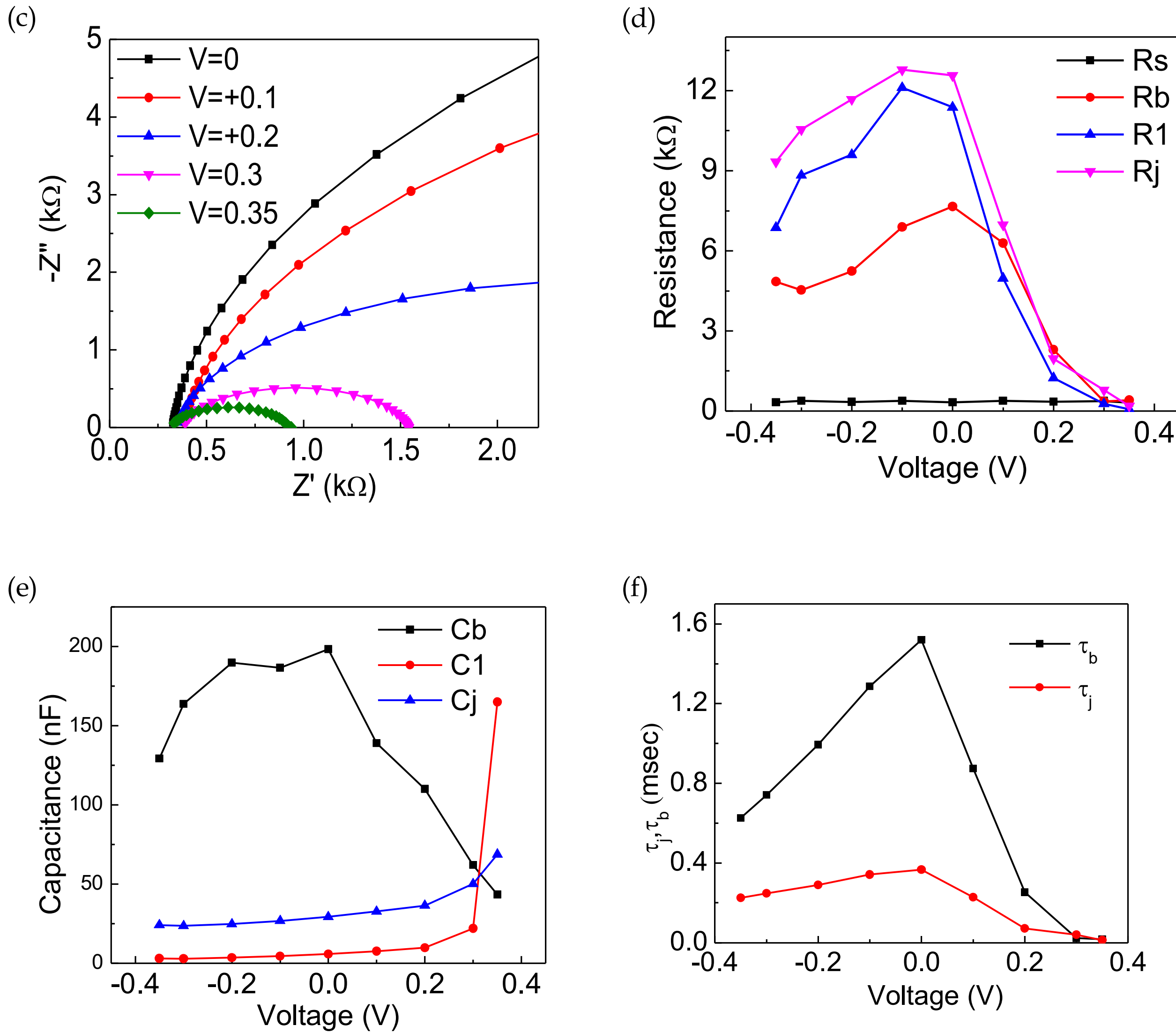


Figure 5.9 Complex plane impedance plot in the dark under (a) forward bias and (b) reverse bias; (c) zoom view of the forward biased impedance plot, (d) resistance variation, (e) capacitance variation, and (f) minority carrier life times ($\tau_j = R_jC_j$ and $\tau_b = R_bC_b$)as a function of bias voltage for Al:ZnO/ ZnO/CdS/CZTS/Mo/SLG solar cells.

The estimated equivalent circuit parameters suggest that the series resistance is nearly independent (355 ± 20 Ω) of bias voltage. This high series resistance observed in the device is attributed due to the formation of Schottky junction at the back contact. When the cell is forward biased, Schottky junction gets reversed bias and vice versa, thereby restricting the current conduction and causing enhanced series resistance for the device [Gunawan, Todorov, & Mitzi, 2010]. The back contact junction limits the current conduction and thus, resulting in reduced capacitance at back contact junction. This reduces the overall capacitance of the cell with increasing forward bias voltage [Ge, Chu, Jiang, Yan, & Yang, 2014]. The observed lower open circuit voltage of the cell is also associated with the generated negative photovoltage at the back contact junction [Ge et al., 2014] which probably plays a major role in large open circuit voltage deficit, usually observed in the kesterite CZTS photovoltaic devices. Back contact capacitance (C_b) of CZTS heterostructure decreases with increasing reverse and forward bias voltages and is consistent with the observed change in diameter of the Nyquist semicircle with applied potential.

The capacitance at CdS/CZTS heterojunction modeled through circuit element C_j in the equivalent circuit M3 behaves like space charge capacitance. The exponential increase in the capacitance with increase in forward bias potential is attributed to the inclusion of diffusion capacitance due to insertion of high forward bias current. The parallel resistance R_j, and R_b in

the equivalent circuit M3 represents the parasitic resistances due to leakage current at the CdS/CZTS and back contact junction, respectively. The estimated time constants are shown in **Figure 5.9 (f)** for CdS/CZTS heterojunction interface (τ_j) and CZTS and MoS_2/Mo back contact interface (τ_b). The time constant values at V = 0.35 V are τ_j= 13.3 μs and τ_b= 17.8 μs. The time constant for the whole CZTS device structure is defined as $\tau = (\tau_j\tau_b/\tau_j+\tau_b)$ and the value is ~ 7.6 μs. The value of time constant obtained from the fitting of impedance data is relatively smaller than that of obtained from the OCVD analysis. The slight difference in the time constant value obtained from these two methods is possibly due to the high population of injected charge carrier in the OCVD measurement and the nonlinear characteristics of OCVD curve that makes it difficult to determine the accurate slope for time constant measurement.

5.3.6 Conclusion

CZTS heterostructure solar cell is fabricated using optimized CZTS absorber film prepared using sol-gel synthesis. High series and lower shunt resistances are observed from electrical measurements and are responsible for the observed low photovoltaic response for these device structures. Equivalent circuit fitting of impedance data suggests the presence of back contact barrier at the back contact interface and significant contribution of trap states near CdS/CZTS interface. The obtained minority carrier life time from the OCVD curve is ~ 23 μs, which is larger than the minority carrier life time ~ 8 μs, observed from impedance measurements. The observed difference in the minority carrier life time value is likely due to the nonlinear characteristics of OCVD curve, which causes difficulties in determining the accurate slope. These studies provide detail electrical characteristics and infer device parameters causing the inferior performance of the device.