3

Mitigation of SHC-ripple in Two-Stage DC-DC-AC Converter: An Adaptive-Sliding Mode Control Approach

In previous Chapter, a comprehensive review of the $2\omega-$ripple problem in the single-phase inverters has been carried-out. Several control techniques for the SHC ripple mitigation have been discussed in detail. The challenges involved in the different control techniques have been discussed thoroughly. The linear control techniques are largely researched to mitigate the $2\omega-$ripple problem in the DC-DC-AC converters. In the two-stage DC-DC-AC converter, the linear control is able to mitigate the SHC ripple at the input without adding extra circuitry to the system, however, the linear control involves various challenges such as the instability problem at the large line-load transients, susceptibility to disturbances and poor dynamic performance of the system. This Chapter presents a new adaptive sliding mode control for the mitigation of the SHC ripple problem at the input of the boost-derived DC-DC-AC converter. The one of the control objective is to minimize the SHC ripple at the source. The second objective of the control is to improve the dynamic performance at the line-load transients. The control technique utilizes the concept of the output-impedance shaping of the front-end DC-DC converter. The adaptive nature of the proposed control shapes the output-impedance of the front-end DC-DC converter such that the output impedance is large at the steady-state that leads to SHC ripple reduction at the DC input and the output-impedance decreases monotonically at the line-load transients to maintain desired dynamic performance. Therefore, the control achieves ripple mitigation along with desired dynamic performance simultaneously. The organization of the Chapter is as follows. In the Section 3.1, the concept of output impedance shaping of the front-end DC-DC converter is discussed. In the Section 3.2, the adaptive switching function and its role in the output impedance shaping is addressed. In the Section 3.3, the existence of the sliding mode, stability analysis, transient response analysis and robustness analysis are presented. In the Section 3.4 and Section 3.5, the simulation results and the experimental results are presented respectively. Section 3.6 summarizes the Chapter-Three.

In Fig. 3.1, the phenomenon of the reflection and propagation of SHC-ripple is depicted.

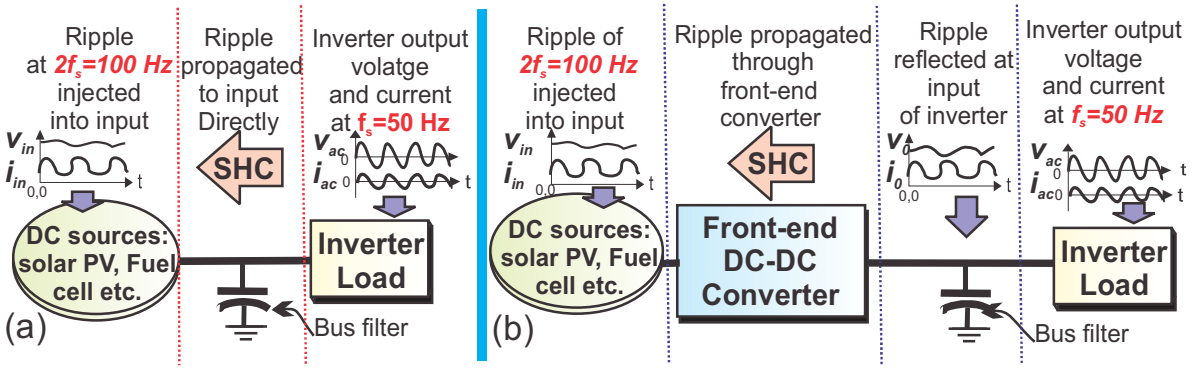

Figure 3.1 : SHC ripple in (a) single stage DC-AC converter (b) two-stage DC-DC-AC converter

In the single-stage converter, the SHC-ripple reflects at the DC link and directly injects into

the DC source for the low capacitance DC-link. However, in the case of the two-stage converter, the SHC-ripple propagates through the intermediate DC-DC converter. In this case, the ripple not only injects into the DC source but also affects the components of the DC-DC converter. In order to comprehend this, Fig.3.2 shows experimental results of two-stage converter for (a) uncompensated and (b) compensated system. In the Fig.3.2, x_1 is the input current and x_0 is the output current of front-end converter or input current of inverter, and V_{ac} is output voltage of inverter. The frequency of V_{ac} is 50 Hz. The ripple in x_1 (Fig. 3.2(a)) and x_0 (Fig. 3.2) is of 100 Hz. Clearly, without compensation, the input current also contains the SHC ripple pulsating over the average value.

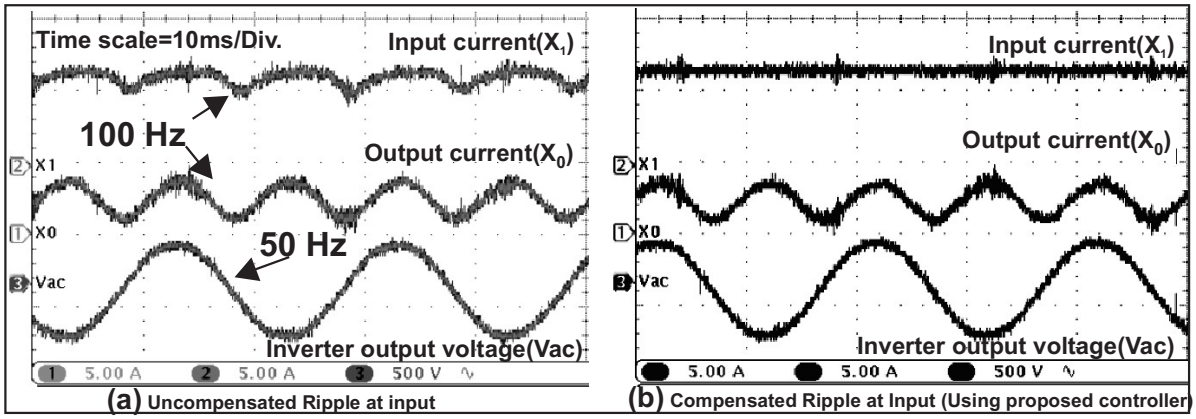

Figure 3.2 : SHC ripple:(a) uncompensated and (b) compensated systems

3.1 CONCEPT OF THE OUTPUT IMPEDANCE SHAPING

In this work, a boost-derived DC-DC-AC two stage converter is considered. The front-end DC-DC converter boosts the low input voltage of the battery-bank and the back-end DC-AC converter serves the purpose of the voltage inversion. A circuit of the boost-derived DC-DC-AC converter is shown in Fig. 3.3.

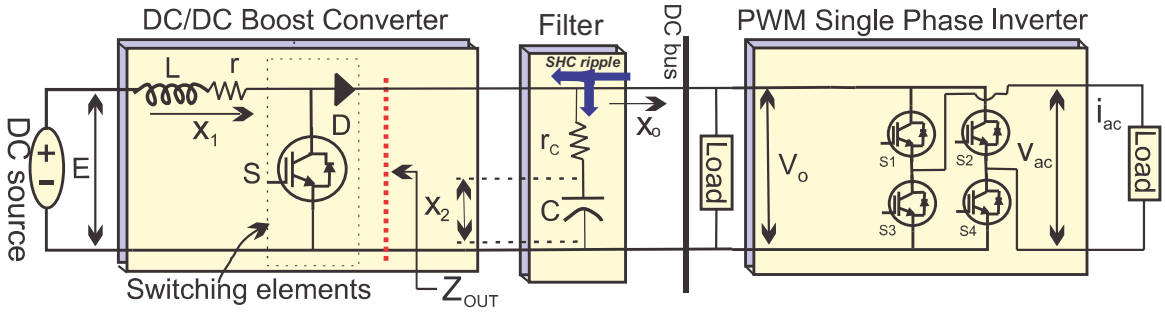

Figure 3.3 : Circuit of two-stage DC-DC-AC converter

The dynamic model of boost converter in error co-ordinates,

$$\dot{e_1} = \frac{1}{L}(E - r(e_1 + x_{1r}) - (1-u)(e_2 + x_{2r})) \tag{3.1a}$$

$$\dot{e_2} = \frac{1}{C}((1-u)(e_1 + x_{1r}) - x_o) \tag{3.1b}$$

The state variables are the inductor current error (e_1) and output capacitor voltage error (e_2), such that $e_1 = x_1 - x_{1r}$ and $e_2 = x_2 - x_{2r}$. Here, x_1 is the inductor (or input) current and x_{1r} is its reference

value. x_2 is the output capacitor voltage (or bus voltage) and x_{2r} is its reference value. The Z_0 is the dynamic load impedance at the output of boost converter. u is control input and E is input voltage. L is inductance and C is output capacitance. r and r_C are the equivalent series resistance (ESR) of inductor and output capacitor respectively. The ESR of film capacitor (used in experimentation) is generally very small. In such case, the output capacitor voltage can be considered equal to output voltage of boost converter.

It should be noted that increase in the output impedance of front-end converter has a significant impact in the reduction of ripple at the DC source side. However, it is not efficient and cost effective to increase the size of passive components in the physical circuit for ripple mitigation. Alternatively, a suitable design of control input (duty of the front-end converter) can play an important role in the ripple reduction. The output impedance of the front-end boost converter seen by the load (as shown in Fig. 3.3) depends on the duty-cycle of front-end converter and can be given by [Ahmad *et al.*, 2012],

$$Z_{out} = \frac{Z_L}{(1-D)^2} \tag{3.2}$$

Here, $Z_L = (r + sL)$ is the impedance of inductor. D is the duty. Clearly, Z_{out} is the function of D. A slight change in duty can modify the output impedance of front-end DC-DC converter. A high output impedance resists the ripple injection into the source and forces its flow through bus capacitor as shown in Fig. 3.3 using arrow. However, this substantial amount of SHC ripple, passing through the output capacitor may cause poor voltage regulation with the insufficient filter capacitance at DC bus. There is a trade-off between ripple reduction and voltage regulation using digital control. Secondly, in many cases, the technique employed for ripple reduction may degrade the dynamic performance of the system. Therefore, an adaptive controller is needed to achieve both the objectives simultaneously.

3.2 PROPOSED CONTROLLER AND ITS ROLE IN THE OUTPUT IMPEDANCE SHAPING

The proposed controller and its role in the ripple reduction at input by output impedance shaping of front-end DC-DC converter is investigated in this Section.

3.2.1 Proposed Adaptive Switching Function

The controller is designed using Sliding Mode Control (SMC) approach. The SMC is one of the nonlinear and robust control approaches. A switching function and a control law are two important design steps of the SMC. The proposed switching function is defined by,

$$\sigma : = e_1 + \alpha e_2 \tag{3.3a}$$

$$\alpha : = \gamma(x_2 - x_{2r})^{\beta} = \gamma e_2^{\beta} \tag{3.3b}$$

Here, $\alpha > 0$ is a time varying power function of e_2. γ is a positive constant and β is an even positive integer. γ limits the value of the α, and steers its value monotonically. The parameter β helps in shaping the profile of α such that α maintains a very small value (say α_{min}) within $x_{2r}(1 \pm R\%)$ (i.e. allowed voltage variation range (AVVR)) at steady-state. Here, the symbol $\%R$ represents percentage output voltage regulation of front-end converter. The value of α increases monotonically when x_2 departs from AVVR. In the Fig. 3.4(a), a typical profile of the α with respect

to per unit bus voltage, $x_2(p.u.)$ is shown. The base voltage for per unit conversion is x_{2r}. For the purpose of illustration, the profile of α is plotted for base or reference voltage, $x_{2r} = 380\,V$, $\gamma = 10^{-10}$, $\pm R\% = \pm 5\%$, and $\beta = 6$.

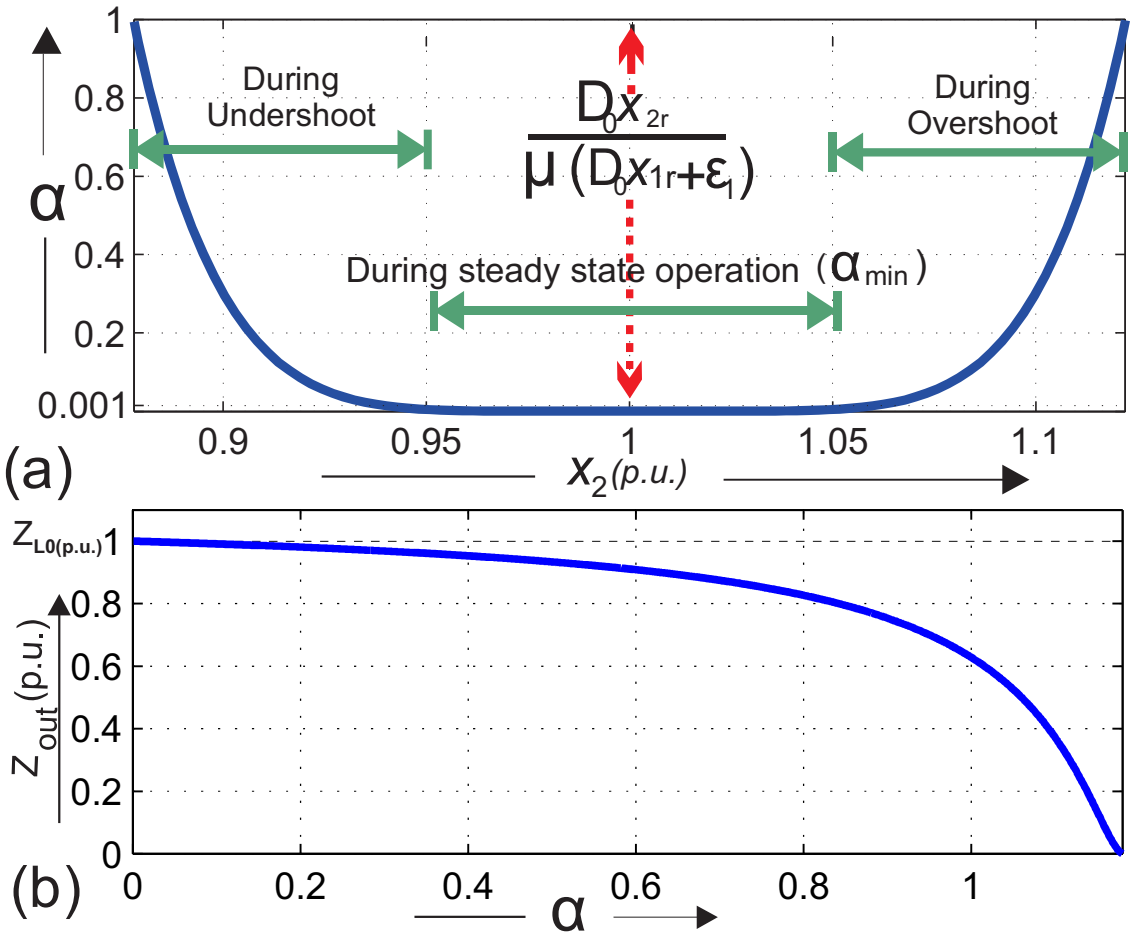

Figure 3.4 : Typical profiles of (a) α versus per unit bus output voltage, x_2 (p.u.) and (b) output impedance (per unit), $Z_{out}(p.u.)$ versus α

We will prove that the output impedance of front-end converter is high for very low α values. This is why a small value of α should be maintained in AVVR. Secondly, we will also prove that the value of α should be increased monotonically when bus voltage departs from the AVVR at line or load transients such that a fast convergence of bus voltage with low undershot/overshoot can be achieved. This is the motivation behind the selection of the profile of α as defined by (3.3b). The range of α is depicted in Fig. 3.4(a). In Fig. 3.4(b), a typical plot of per unit output impedance, $Z_{out}(p.u.)$ versus α is shown.

Now, the time derivative of the switching function is,

$$\dot{\sigma} = \dot{e_1} + \alpha \dot{e_2} + \dot{\alpha} e_2 \tag{3.4}$$

The time derivative of α is $\beta \alpha \frac{\dot{e_2}}{e_2}$. Using this in (3.4),

$$\dot{\sigma} = \dot{e_1} + \alpha(\beta + 1)\dot{e_2} \tag{3.5}$$

We have chosen the reaching dynamics given below [Hung *et al.*, 1993],

$$\dot{\sigma} = -\Gamma\sigma - Qsgn(\sigma) \qquad \Gamma, Q \in \mathbb{R}^+ - \{0\} \tag{3.6}$$

Here, (3.6) ensures the reaching of the system dynamics on the sliding surface ($\sigma = 0$) in finite time, where Γ is the tuning parameter and Q depends on maximum value of disturbance. By solving (3.1), (3.5) and (3.6), the duty of the controller is calculated.

3.2.2 Control Law

The control input, u is deduced using (3.1), (3.5) and (3.6),

$$\begin{aligned} u = 1 - \Big[\frac{-\frac{\alpha\mu}{Z_0}(e_2 + x_{2r}) - r(e_1 + x_{1r}) + E}{(e_2 + x_{2r}) - \alpha\mu(e_1 + x_{1r})}\Big] \\ - \Big[\frac{L(\Gamma\sigma + Qsgn(\sigma))}{(e_2 + x_{2r}) - \alpha\mu(e_1 + x_{1r})}\Big] \end{aligned} \tag{3.7}$$

Here, $\mu = \frac{(\beta+1)L}{C}$.

3.2.3 Output Impedance Shaping of Front-End Converter

During sliding mode $\sigma \approx 0$, then (3.7) reduces to,

$$u = 1 - \frac{-\frac{\alpha\mu}{Z_0}(e_2 + x_{2r}) - r(e_1 + x_{1r}) + E}{(e_2 + x_{2r}) - \alpha\mu(e_1 + x_{1r})} \tag{3.8}$$

In (3.8), for $e_1 = e_2 = 0$, the u is equal to D_0 for ideal converter ($r = 0$). D_0 is equal to $(1 - \frac{E}{x_{2r}})$ and $(1 - \frac{x_{2r}}{Z_0 x_{1r}})$. However, in this particular problem, ripple component can not be neglected completely. Suppose, sliding mode is stable and steady state is reached. During steady state operation, e_1 is equal to ripple in input current say, ε_1 and e_2 is equal to output voltage ripple value say, ε_2. At steady-state, these ripples pulsate over average values of current and voltage respectively. Also, parasitic resistance of inductor (r) is negligible. Considering these in (3.8) and dividing numerator and denominator by x_{2r}, we have the control input at steady state (*say*, D),

$$D = 1 - \frac{-(1 + \frac{\varepsilon_2}{x_{2r}})\frac{\alpha\mu}{Z_0} + \frac{E}{x_{2r}}}{(1 + \frac{\varepsilon_2}{x_{2r}}) - \alpha\mu(\frac{x_{1r}}{x_{2r}} + \frac{\varepsilon_1}{x_{2r}})} \tag{3.9}$$

Here, $|\frac{\varepsilon_2}{x_{2r}}| << 1$ and can be neglected. Also, $D_0 = (1 - \frac{E}{x_{2r}}) = (1 - \frac{x_{2r}}{Z_0 x_{1r}}) < 1$. Using these in (3.9), we have

$$D \approx \frac{D_0 - \delta}{1 - \delta} \tag{3.10}$$

Here, $\delta = \frac{\alpha\mu\varepsilon_1}{x_{2r}-\alpha\mu x_{1r}}$ and $0 < D < 1$. This implies $0 < \delta < D_0$. Furthermore, solving this inequality for α gives,

$$0 < \alpha < \frac{D_0 x_{2r}}{\mu(D_0 x_{1r} + \varepsilon_1)} \tag{3.11}$$

Now, using (3.2) and (3.10), the output impedance of the boost converter is given by,

$$Z_{out} = Z_{L_0}(1-\delta)^2 \tag{3.12}$$

Here $Z_{L_0} = \frac{Z_L}{(1-D_0)^2}$ and $0 < \delta < D_0 < 1$. The δ is the function of α. The value of δ increases/decreases with the increase/decrease in the value of α for the range given by (3.11). This implies, Z_{out} increases/decreases with the decrease/increase in the α. This implies that a high value of Z_{out} can be obtained at $\alpha \approx 0$. It is noted that α can not be zero as it contributes to the convergence of voltage error (see 3.3a). This proves the suitability of the α as shown in Fig. 3.4(a), that maintains the value of α nearly zero for the 5%-voltage regulation i.e. within AVVR. This concludes that the proposed switching function can achieve high Z_{out} in AVVR range, this implies the reduction in ripple at the input.

3.3 STABILITY AND TRANSIENT RESPONSE ANALYSIS

In this Section, stability of the sliding mode and existence of sliding mode are established. Thereafter, study on the system dynamics response at line or load transitions is carried out near to the sliding manifold, $\sigma = 0$.

3.3.1 Existence of Sliding Mode

The existence of sliding mode for the switching function given by (3.3a) can be guaranteed if the $\eta-$ reachability condition [Edwards and Spurgeon, 1998],

$$\sigma^T \dot{\sigma} < -\eta|\sigma|, \quad \eta > 0 \tag{3.13}$$

holds for the reaching dynamics given by (3.6). To establish the condition for the existence, we consider the LHS part of the (3.13) and substituting (3.6) in it gives

$$\sigma^T \dot{\sigma} = -\sigma^T \Gamma \sigma - \sigma^T Q sgn(\sigma) \tag{3.14}$$

Here, σ is the scalar quantity, this implies $\sigma^T = \sigma$. Also, $\sigma sgn(\sigma) = |\sigma|$, this gives

$$\sigma^T \dot{\sigma} = -(\Gamma|\sigma| + Q)|\sigma| \tag{3.15}$$

Comparing the (3.13) with (3.15), we have $\eta \geq \Gamma|\sigma| + Q$. This implies that the existence of sliding mode is guaranteed for all $\eta > \Gamma|\sigma| + Q$ provided $\Gamma, Q > 0$.

3.3.2 Stability of the Sliding Mode

Here, the stability of the sliding mode is proved using Lyapunov approach.

During sliding mode ($\sigma = 0$), system dynamics are stable (i.e. e_1 converges to $e_1 \approx 0$ and e_2 converges to $e_2 \approx 0$, if errors satisfy the bounds,

$$e_1 \in [\bar{\kappa_1} \;\; \bar{\kappa_2}], \quad e_2 \in [\bar{\kappa_3} \;\; \bar{\kappa_4}] \quad for \;\; 0 < \alpha < \frac{x_{2r}}{\mu x_{1r}} \tag{3.16}$$

Here, $\bar{\kappa_1} = -\frac{(1-D_0)\kappa_1\alpha}{\kappa_2}$, $\bar{\kappa_2} = \frac{D_0\kappa_1\alpha}{\kappa_2+\kappa_3}$, $\bar{\kappa_3} = -\frac{D_0\kappa_1}{\kappa_2+\kappa_3}$ and $\bar{\kappa_4} = \frac{(1-D_0)\kappa_1}{\kappa_2}$, where $\kappa_1 = C(x_{2r} - \mu\alpha x_{1r})$, $\kappa_2 = \frac{C\mu\alpha}{Z_0}$ and $\kappa_3 = C(1+\mu\alpha^2)$.

Proof. During sliding mode, ($\sigma = 0$),

$$e_1 + \alpha e_2 = 0 \quad Or, \;\; e_1 = -\alpha e_2 \tag{3.17}$$

Using (3.17), it is obvious that convergence of e_2 results into convergence of e_1. Hence, we need to prove the convergence of e_2 only.

Choose a Lyapunov function, $V = \frac{1}{2}e_2^2$. Its derivative is,

$$\dot{V} = e_2\dot{e}_2 \tag{3.18}$$

Using (3.1b), (3.17) and (3.18), we have

$$\dot{V} = -\frac{e_2^2}{C}((1-u)\alpha + \frac{1}{Z_0}) - e_2(\frac{x_{2r}}{Z_0} - (1-u)x_{1r}) \tag{3.19}$$

Further simplifying (3.19) using $x_{1r} = \frac{x_{2r}}{Z_0(1-D_0)}$, we have

$$\dot{V} = -\frac{e_2^2}{C}((1-u)\alpha + \frac{1}{Z_0}) - e_2\frac{x_{2r}}{Z_0}(1 - (\frac{1-u}{1-D_0})) \tag{3.20}$$

Here, $(1-u)$ lies between 0 to 1. The first term in the RHS of (3.20) is negative for $0 < (1-u) < 1$. Secondly, it should be noted that output voltage increases with the decrease in $(1-u)$ for boost converter, and vice-versa. The x_{2r} is the output voltage of boost converter for $u = D_0$. This implies $(1-u) < (1-D_0)$ for $e_2(i.e. \;\; x_2 - x_{2r}) > 0$, and $(1-u) > (1-D_0)$ for $e_2 < 0$. Using these relations in (3.20), the second term in the RHS of (3.20) also becomes negative. This implies that $\dot{V} < 0$ for $0 < 1-u < 1$. Now, to ensure $0 < (1-u) < 1$ for stability of the sliding mode, the condition can be deduced as follows,
Eq.(3.8) can further be simplified in the form of complimentary of input signal as,

$$1 - u = \frac{(1-D_0)\kappa_1 - \kappa_2 e_2}{\kappa_1 + \kappa_3 e_2} \tag{3.21}$$

In (3.8), the value of r is negligible and hence neglected.
In order to satisfy $0 < 1-u < 1$, the range of e_2 can be defined using (3.21) as,

$$-\frac{D_0\kappa_1}{\kappa_2+\kappa_3} < e_2 < \frac{(1-D_0)\kappa_1}{\kappa_2} \tag{3.22}$$

Here, κ_2 and κ_3 are positive terms. In (3.22), $\kappa_1 = C(x_{2r} - \mu\alpha x_{1r})$ is positive for $\alpha < \frac{x_{2r}}{\mu x_{1r}}$. Also, the range of e_1 is obtained using (3.17). This implies the system is stable when e_1 and e_2 respect the range given by (3.17). This completes the proof. □

3.3.3 Transient Response Analysis

It is noted that α is the convergence factor of voltage error (e_2) in (3.3a). A small value of α makes the voltage error part less significant. This causes sluggish system dynamics at load transients. To investigate the effect of α on system dynamics, we consider (3.20) again. We have already proved that,

$$\dot{V} = -\frac{e_2^2}{C}((1-u)\alpha + \frac{1}{Z_0}) - e_2\frac{x_{2r}}{Z_0}(1-(\frac{1-u}{1-D_0})) < 0 \tag{3.23}$$

for $0 < \alpha < \frac{x_{2r}}{\mu x_{1r}}$. Now, using (3.23), it can be concluded that the increase in the value of α (from 0 to $\frac{x_{2r}}{\mu x_{1r}}$) makes the value of $\dot{V}$ more negative, hence, system dynamics converge at the faster rate. This follows that the undershoot or overshoot dies out at faster rate. Alternatively, the analysis of system stability and system transients response is carried out using equivalent dynamic equations of the closed-loop system about the operating points. Using system dynamic equations of (3.1) and equivalent control input (for $\sigma = 0$) given by (3.8), the closed-loop dynamics are,

$$\dot{e_1} = \frac{\alpha\mu(\frac{(e_2+x_{2r})^2}{Z_0} - (e_1+x_{1r})(E - r(e_1+x_{1r})))}{L((e_2 a + x_{2r}) - \alpha\mu(e_1+x_{1r}))} \tag{3.24a}$$

$$\dot{e_2} = \frac{(e_1+x_{1r})(E - r(e_1+x_{1r})) - \frac{(e_2+x_{2r})^2}{Z_0}}{C((e_2+x_{2r}) - \alpha\mu(e_1+x_{1r}))} \tag{3.24b}$$

The system dynamic equations of (3.24) are linearized about the operating points $(\varepsilon_1, \varepsilon_2)$. ε_2 can be obtained using (3.3b) for a suitable value of α, and ε_1 can be obtained using (3.24) for given ε_2 at steady state (by equating $\dot{e_1} = 0$ or $\dot{e_2} = 0$). A generalized Jacobian matrix, ($\mathbf{A_{cj}}$) about $(\varepsilon_{1j}, \varepsilon_{2j})$ for some $\alpha = \alpha_j$ can be obtained as follows,

$$\mathbf{A_{cj}} = \begin{bmatrix} J_{11j} & J_{12j} \\ J_{21j} & J_{22j} \end{bmatrix}$$

Suppose the two Eigen values of closed loop system matrix, $\mathbf{A_{cj}}$ are λ_j^+ and λ_j^-. Now using $\mathbf{A_{cj}}$, an Eigen values plot for $\alpha = 0.001$ to $\alpha = 0.05$, is obtained and shown in Fig. 3.5.

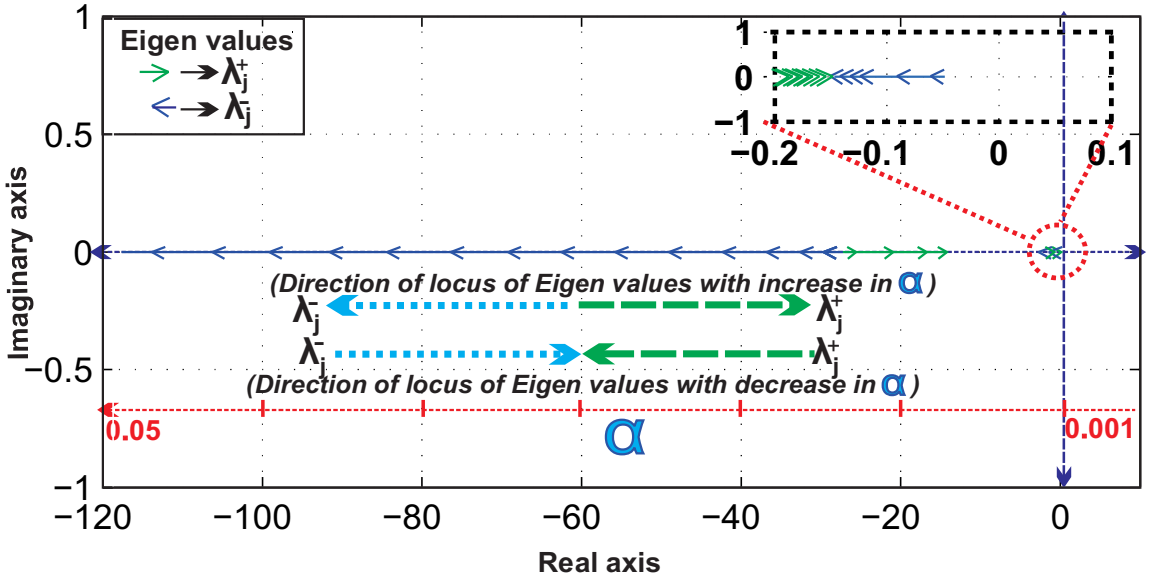

Figure 3.5 : Locus of Eigen values with variations in α

From the Fig. 3.5, it can be observed that the system is stable as the all Eigen values are real and negative. Secondly, for the analysis of system performance, the locus of Eigen values $(\lambda_j^+, \lambda_j^-)$ with variations in α is observed. From the Fig. 3.5, it can be concluded that for high values of α, Eigen values are relatively farther from the imaginary axis and vice-versa. This indicates that the system convergence is faster for higher values of α.

3.3.4 System Robustness Analysis

In this Section, the robustness analysis, in the presence of uncertainty in the system parameters (C, L) is carried out. The objective of this analysis is to verify whether the sliding mode $\sigma = 0$ is established in spite of this uncertainty. This can be done using the reachability condition given by (3.13). It should be noted that the sliding mode ($\sigma = 0$) exists if reachability condition is satisfied. For this, we rewrite the dynamic model of (3.1) as follows,

$$\dot{e} = M(f + gu) \tag{3.25}$$

Here, f, g, u are the function of e and t, such that

$$e := \begin{bmatrix} e_1 \\ e_2 \end{bmatrix},\ f := \begin{bmatrix} f_1 \\ f_2 \end{bmatrix} = \begin{bmatrix} E - r(e_1 + x_{1r}) - (e_2 + x_{2r}) \\ (e_1 + x_{1r}) - (\frac{e_2 + x_{2r}}{Z_0}) \end{bmatrix}$$

$$g := \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} = \begin{bmatrix} (e_2 + x_{2r}) \\ -(e_1 + x_{1r}) \end{bmatrix},\ M := \begin{bmatrix} a & 0 \\ 0 & b \end{bmatrix},\ a = \frac{1}{L},\ b = \frac{1}{C}$$

Variations in L and C will change a by Δa and b by Δb. This implies M changes to $M + \Delta M = \begin{bmatrix} a + \Delta a & 0 \\ 0 & b + \Delta b \end{bmatrix}$. Considering this in (3.25), the dynamic model becomes,

$$\dot{e} = (M + \Delta M)(f + gu) \tag{3.26}$$

Now, using (3.25), (3.7) becomes,

$$u = -(NMg)^{-1}(\Gamma\sigma + Qsgn(\sigma) + NMf) \tag{3.27}$$

Here, N is the row vector i.e. $N = [1 \quad (\beta + 1)\alpha]$. It is to be noted that controller is derived based on nominal model of the system. It is to be established that this controller brings sliding mode in finite time even with uncertainty in the parameters. Now, using (3.5) and (3.26),

$$\dot{\sigma} = N(M + \Delta M)(f + gu) \tag{3.28}$$

The robustness of the system against the variation in the system parameters (L, C) is ensured if reachability condition given by (3.13) is satisfied. Using LHS of (3.13), (3.27) and (3.28),

$$\sigma^T \dot{\sigma} = -\sigma^T((\Gamma\sigma + Qsgn(\sigma))\Delta y - \Delta x) \tag{3.29}$$

Here, $\Delta x = N\Delta M f - N\Delta M g(NMG)^{-1}NMf$ and $\Delta y = 1 + N\Delta M g(NMg)^{-1}$. σ is the scalar quantity. Therefore, $\sigma^T = \sigma$. Also, $\sigma sgn(\sigma) = |\sigma|$. Using this in (3.29),

$$\sigma\dot{\sigma} = -((\Gamma|\sigma| + Q)\Delta y - \frac{\Delta x}{sgn(\sigma)})|\sigma| \tag{3.30a}$$

$$\sigma\dot{\sigma} = -\eta^{'}|\sigma| \tag{3.30b}$$

Here, $\eta^{'} = ((\Gamma|\sigma| + Q)\Delta y - \frac{\Delta x}{sgn(\sigma)})$.

The reachability condition given by (3.13) satisfies, provided that $\eta^{'} > 0$. Suppose $\frac{\Delta x}{\Delta y} = \rho_{max}$. ρ_{max} is the maximum tolerable parametric uncertainty in the system. Using (3.30), for $\eta^{'} > 0$, the following condition must be fulfilled,

$$|\rho_{max}| < |\Gamma|\sigma| + Q| \tag{3.31}$$

Here, $|sgn(\sigma)| = 1$. By design $Q > \rho_{max}$ such that this respects the condition given by (3.31).

From the above discussion, it is clear that the ripple reduction is possible by reducing the value of α. On the other hand, at line or load transients, the sluggish system dynamics can be improved by increasing the value of α. The proposed adaptive surface ensures ripple mitigation and improvement in transients performance by modulating the parameter α. This is why the profile of α is chosen as plotted in Fig. 3.4(a). This makes the switching function nonlinear and adaptive.

The schematic of the proposed control scheme is shown in Fig. 3.6. It is to be noted that the inverter is a load. Therefore, the design of controller for the inverter is not our main objective. This is why an open loop SPWM controller is used for the inverter.

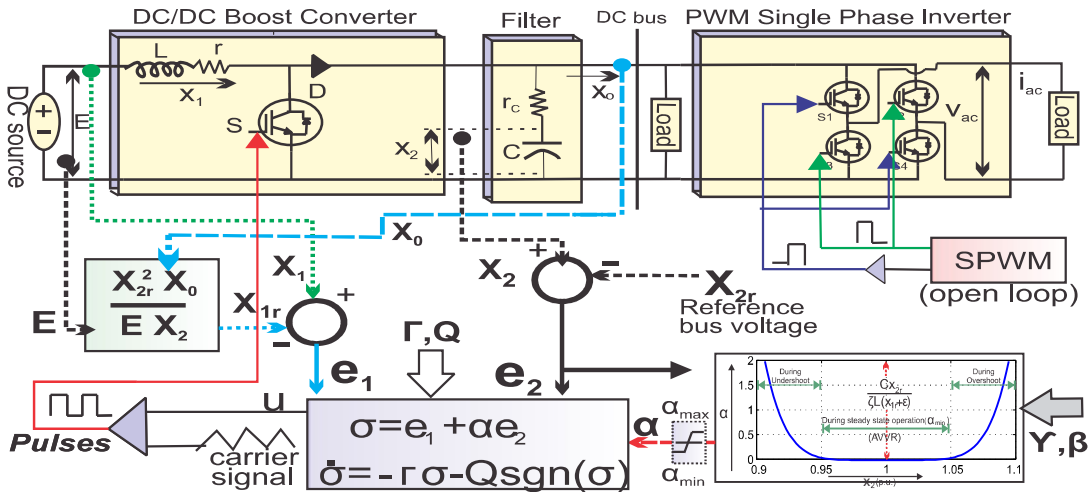

Figure 3.6 : Schematic of the proposed control scheme

3.4 SIMULATION RESULTS

The system parameters, given in Table 3.1, are used for the simulation.

Table 3.1 : System Parameters

Parameter	Value
Rating of lead acid battery and load	110 V, 26 Ah and 2.5 kW
Nominal DC bus voltage	350 V
Inductance (L), (r) and Output or bus capacitor (C)	150 μH; 25 mΩ and 1.9mF
Switching frequency of boost converter (f_s)	25 kHz
Output AC voltage (V_{ac}) and Modulation index, (MI)	220 V, 50 Hz and 0.88
Switching frequency of inverter $(f_{s_{inv}})$	5 kHz

A lead-acid battery available under *SimPowersystems* library of simulink is used as the source in the simulation. The profile of α chosen is similar as in the Fig. 3.4(a). The design parameters are, $\Gamma = 3200, Q = 10, \gamma = 3 * 10^{-6}$ and $\beta = 4$. Two different cases are shown in simulation results: (a) Case I-Impact of the variation in α on ripple reduction (b) Case II-Load transients test for the analysis of system dynamics performance.

Test Case-I Ripple Reduction Test (Impact of α on ripple): The bus voltage (x_2), input voltage (E), input current (x_1) and bus/output current (x_0) of the boost converter are shown in Fig. 3.7.

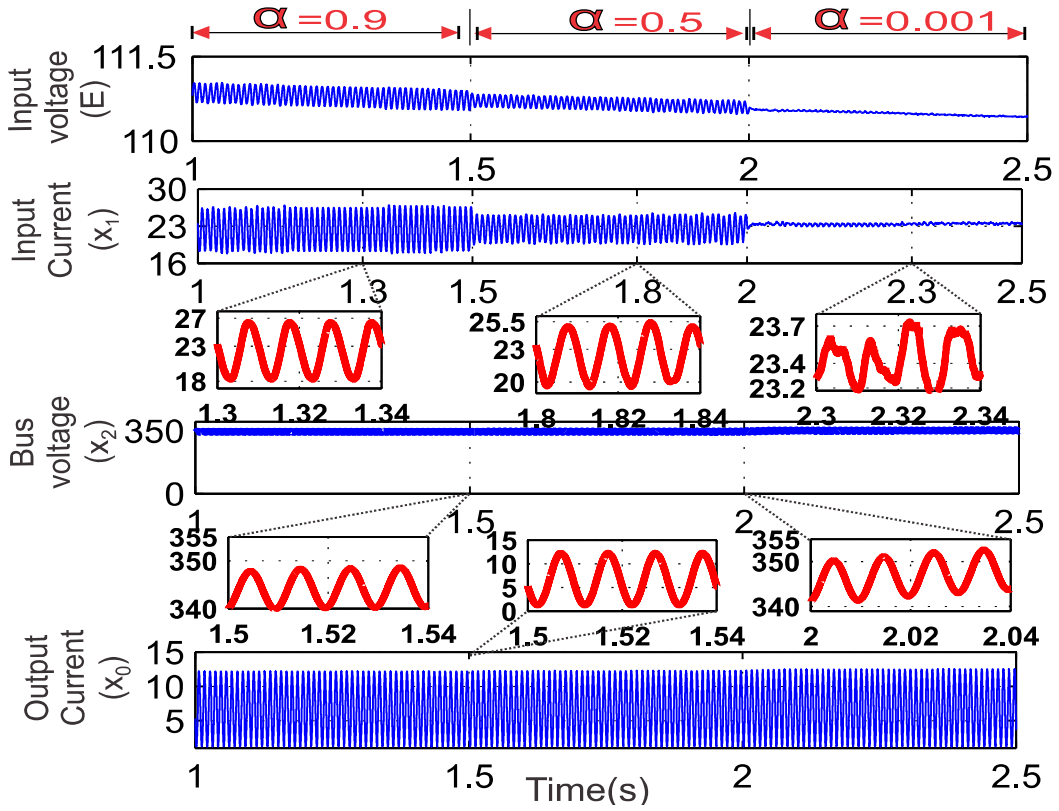

Figure 3.7 : Simulation results of Test Case-I for $\alpha = 0.9, 0.5, 0.001$

This figure shows results for three different values of $\alpha = 0.9, 0.5, 0.001$. The ripple in input current decreases with the decrease in α. For α=0.9, the peak to peak ripple (9 A) in battery current with respect to its average value (23 A) is 39%. This reduces to 1.5% (approx) for $\alpha = 0.001$. This verifies the theory presented in Section 3.2.

For the comparison of load test results of proposed controller, the PI controllers for ripple mitigation are designed using the design guidelines of [Liu and Lai, 2007b]. Firstly, to design PI controllers, the poles and zeros are placed according to Table 3.2.

Table 3.2 : PI Controller Design for 100 Hz Ripple Compensation[Liu and Lai, 2007b]

Parameter	**Design requirements**
(1) Inner and outer compensator design criterion	poles at origin and at half of the switching frequency $(f_s/2)$, zero at or below resonance frequency
(2) Bandwidths of outer loop and inner loop	5 Hz and 550 Hz
Gains of inner compensator and outer compensator	0.13999 and 5.2899

Secondly, the gain of PI controllers are chosen accordingly to obtain the desired bandwidths of inner loop and outer loop. The designed controller gains are given in Table 3.2.

In Fig. 3.8(a), the block diagram of dual loop control scheme for the boost converter, is shown. $\tilde{x_1}, \tilde{x_2}, \tilde{d}, \tilde{x_o}, \tilde{x_{1r}}, \tilde{x_{2r}}$ are the variables in small signal sense. C_i and C_v are PI controllers. H_i and H_v are the sensor gains. G_{vd} and G_{id} are the transfer functions of control-to-output voltage and control-to-inductor current respectively. F_{pwm} is PWM gain. The bode plots of open loop gains without controller (G_i) and with controller (T_i) for inner loop and open loop gains without controller (G_o) and with controller (T_o) for outer loop are shown in the Fig. 3.8(b). f_{oi} and f_{ov} are cut-off frequencies of T_i and T_o respectively. Clearly, as suggested in [Liu and Lai, 2007b], the cut-off frequencies of T_o and T_i are separated by more than half a decade from ripple frequency (2ω). ω is the angular frequency of output voltage of inverter. In Fig. 3.8(b), the bandwidth of T_i is $> 10\omega$ and bandwidth of T_o is far below the ripple frequency i.e. $< \frac{2\omega}{5}$. The purpose of reduction of the voltage loop bandwidth is to increase the output impedance of front-end converter and hence reduction in the SHC ripple at input [Ahmad *et al.*, 2012; Zhang *et al.*, 2014]. However, this results to poor system dynamics.

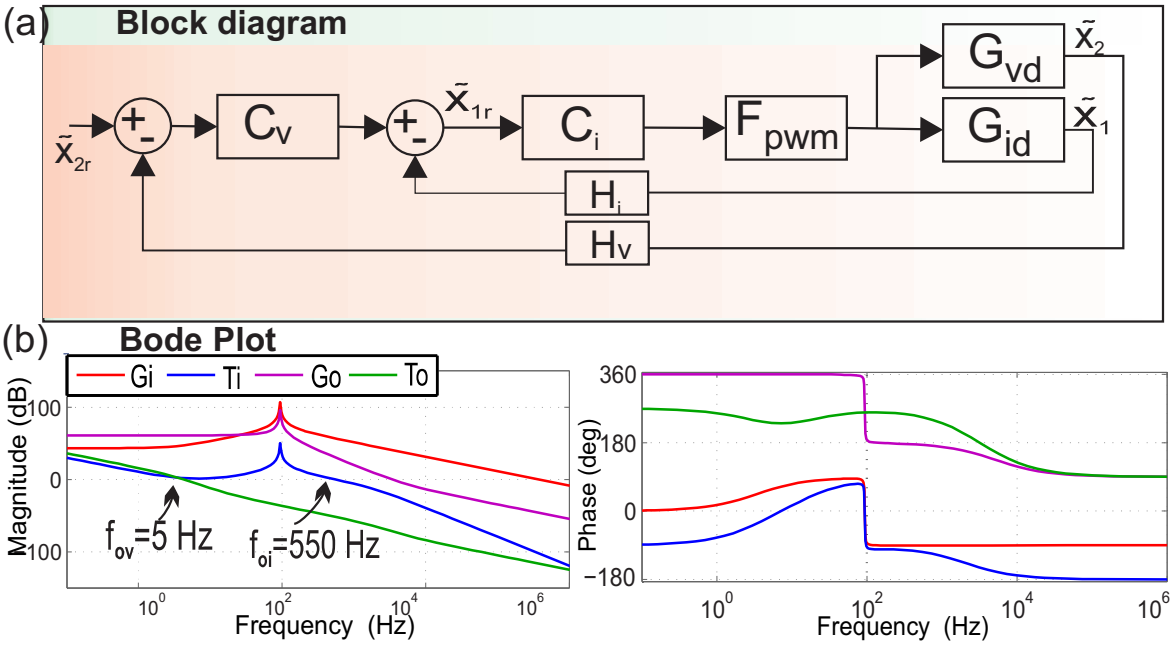

Figure 3.8 : (a) Schematic of dual loop control (b) Bode plot

Test Case-II Load Transient Response Test: The simulations results for the PI controller and the proposed controller are shown in Fig. 3.9. For load test, load application transients and load removal transients are captured and discussed here.

(a) System Response at Load Removal: At t=4 s, the 2 kW-inverter load is removed suddenly. PI controller shows a bus voltage overshoot of 18.5%. The output voltage settles down in 700 *ms* at reference voltage (350 V). The 0.5 kW-inverter load is kept connected. At no-load condition, the system shows very large undershoot/overshoot and sluggish response with PI controller. On the other hand, complete 2.5-kW inverter load is removed suddenly for the proposed controller case. The proposed controller shows an overshoot of 4% only in bus voltage, and settles down there within < 10 *ms*.

(b) System Response at Load Application: At t=8 s, the load is applied. The bus voltage shows undershoot of 17% for PI controller and only 2% for the proposed controller respectively.

The bus voltage tracks reference in 300 *ms* for PI and in 20 *ms* for proposed controller. For the PI controller, the peak to peak SHC ripple in battery current is 3.5% that is more than as in case of the proposed controller (shown at $t = 1$ *s* in Fig. 3.9). Other plots for both cases are also shown.

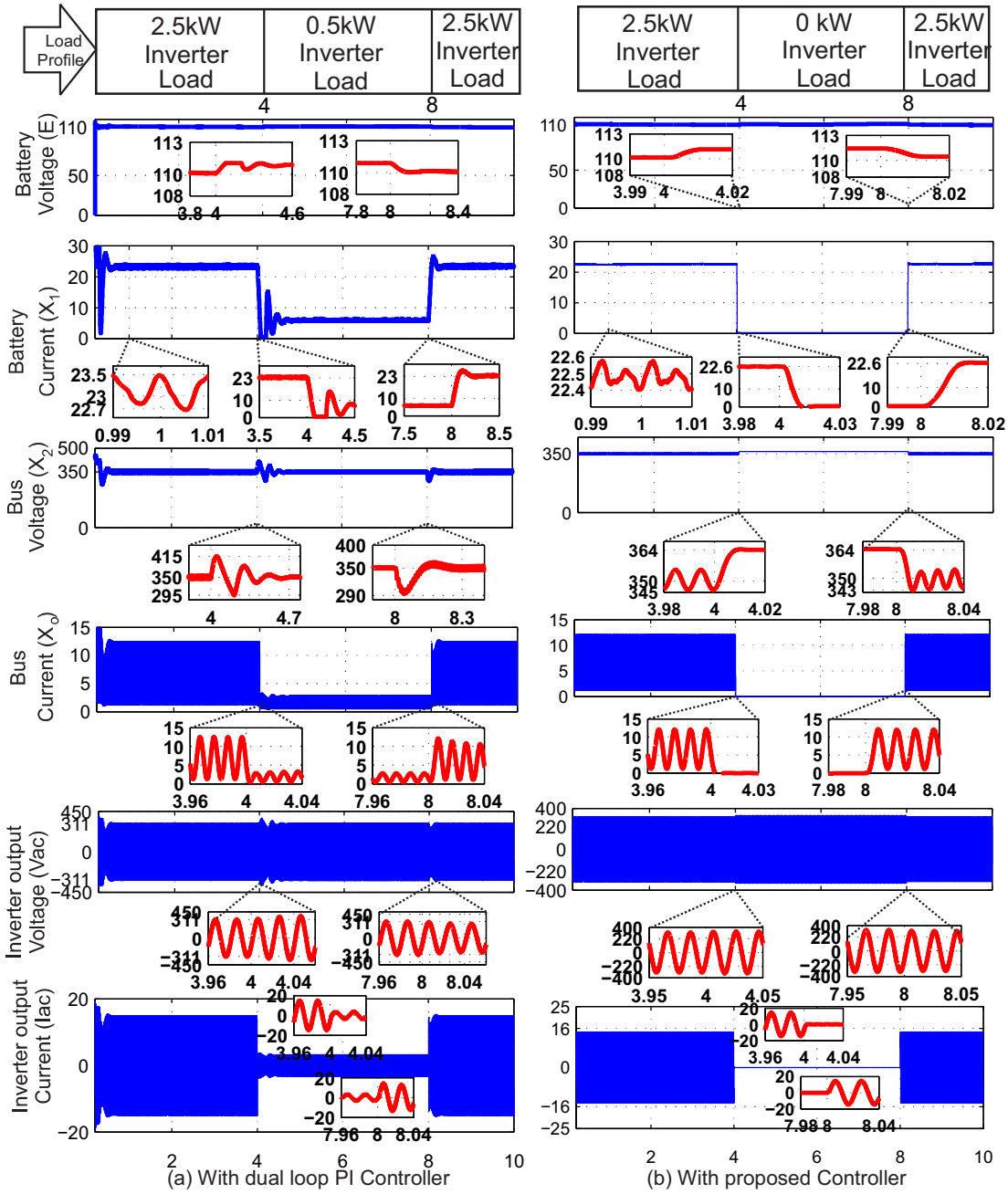

Figure 3.9 : Simulation results for Test Case-II

Additionally, the comparison is also done with nonlinear compensator presented in [Ahmad *et al.*, 2012]. The simulation results of PI, nonlinear compensator of [Ahmad *et al.*, 2012] and proposed controller are summarized in the Table 3.3. Comparing all together, it can be concluded that the proposed controller performs better. Secondly, the conventional method e.g. passive compensation requires a bulky capacitor (30 mF) at DC bus[Ahmad *et al.*, 2012]. However, with the proposed control, only 1.9 mF-capacitor at the DC-bus is required. α is designed for 5% bus voltage regulation. This is why there is a steady state error in bus voltage, which is $< 5\%$ of x_{2r}.

Table 3.3 : Comparison of simulation results for the different controllers

Parameter	**Dual loop PI controller** [Liu and Lai, 2007b]	**Nonlinear compensator** [Ahmad *et al.*, 2012]	**Proposed Controller**
% Peak to Peak ripple in x_1	3.5%	1.8%	1.5% (approx)
Input filter capacitor	220 μF	220 μF	220 μF
Bus filter capacitor	1.9 mF	1.9 mF	1.9 mF
Input voltage	110 V	110 V	110 V
Bus voltage	350 V	350 V	350 V
Inverter Load Transients	0.5 kW to 2.5 kW	0 kW to 2.5 kW	0 kW to 2.5 kW
Bus voltage overshoot/ undershoot	+18.5%/-17%	+4.5%/-4.5%	+4%/-2%
Voltage recovery time at load removal	700 ms	maintains voltage regulation $< 5\%$	voltage regulation$< 5\%$
Voltage recovery time at load application	300 ms	200 ms	20 ms

3.5 EXPERIMENTAL RESULTS

In this Section, the proposed controller is validated using a 1 kW-lab prototype of two-stage DC-DC-AC converter. The experimental setup is shown in the Fig. 3.10. In Fig. 3.10, a boost

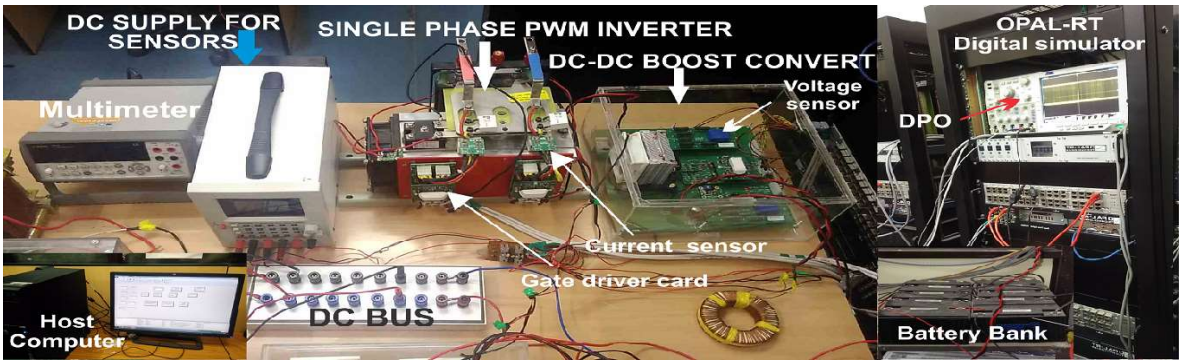

Figure 3.10 : Experimental setup

converter, a single phase PWM inverter, current and voltage sensors, battery-bank and control platform (Real Time Digital Simulator) are shown. The experimental parameters are as follows $E = 120\ V, x_{2r} = 380\ V, C = 1\ mF, L = 2\ mH, Q = 10$ and Γ=2000. The profile of the α is chosen as shown in Fig. 3.4(a). The designed parameters for α are, $\beta = 6$ and $\gamma = 10^{-10}$. Here, the experimental results are shown for three different test Cases, (I) SHC ripple reduction test (II) Load transients test and (III) Line or input voltage variation test. The experimental results are shown for battery as input source in Fig. 3.11-Fig. 3.15. An additional result is also shown using Solar PV (with rated voltage=160 V) as input in Fig. 3.16 for Case-II.

Test Case-I SHC Ripple Reduction Test: For Test Case-I, the experimental results are shown in the Fig. 3.11 (similar as in the Fig. 3.7). Here also, the value of α is varied i.e. $\alpha = 0.9, 0.5, 0.001$. The peak to peak SHC ripple in battery/input current reduces with the decrease in α. The ripple in the input current is negligible ($< 1\%$) for $\alpha = 0.001$. The experimental result for decrease in the ripple at input with decrease in α validates the theory presented in Section 3.2. The input voltage, output voltage and output current are also shown in Fig. 3.11. In Fig. 3.12, FFT diagram for the compensated system with the proposed controller is shown. Fig. 3.12(a) shows that there is neg-

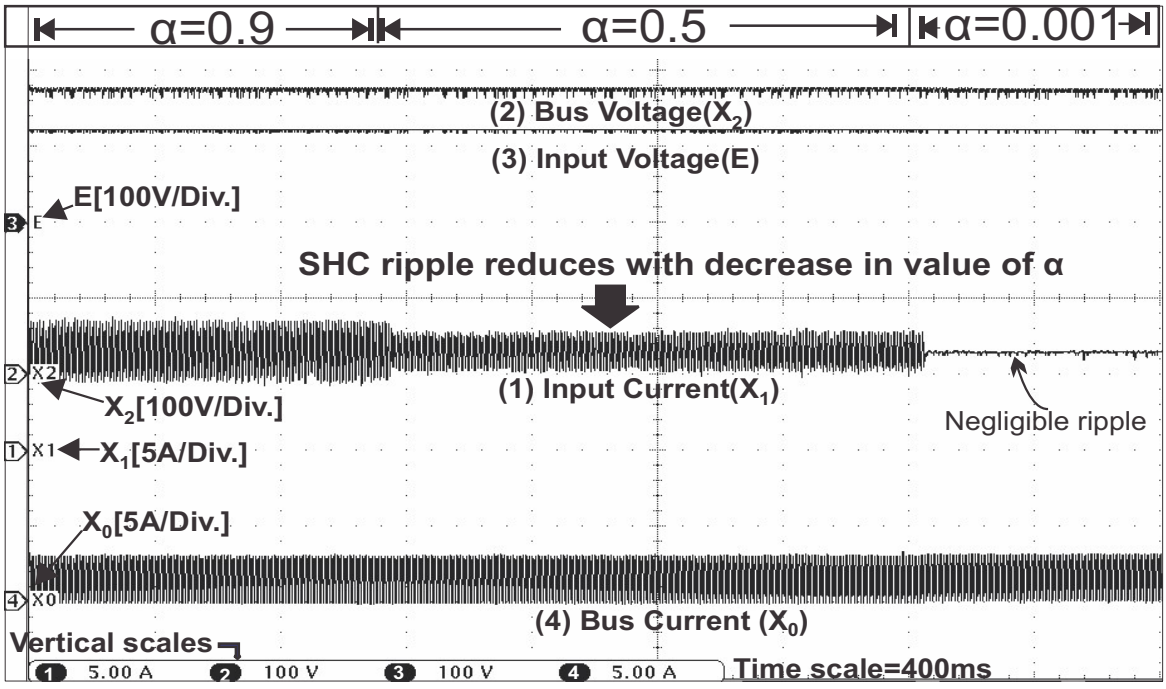

Figure 3.11 : Experimental results of Test Case-I using proposed controller

ligible component of 100 Hz in input current x_1. In Fig. 3.12(b), the output current (x_0) of boost converter contains the 100 Hz ripple component which is obvious. In Fig. 3.12(c), shows the FFT diagram of output voltage of inverter.

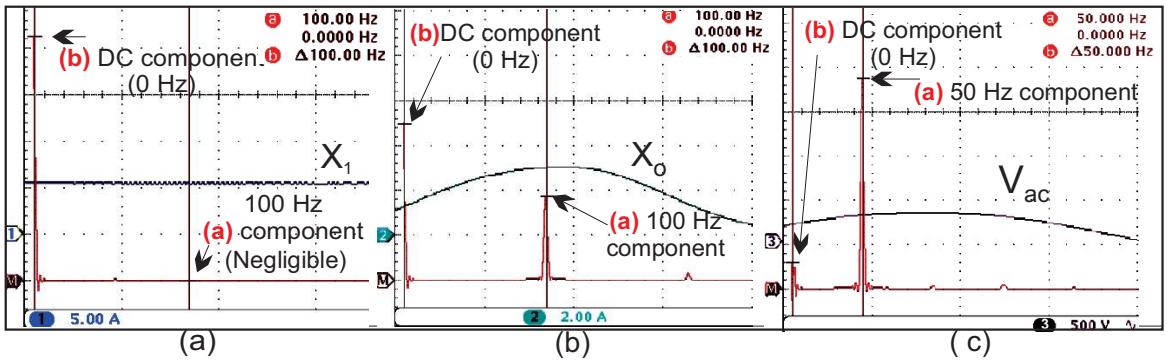

Figure 3.12 : FFT diagram for compensated system: (a) x_1 (b) x_0 and (c) V_{ac}

Test Case-II Load Transients Test: The experimental load transients results for No Load to 1 kW-inverter load and 0.6 kW to 1 kW-inverter load are shown in Fig. 3.13 and Fig. 3.14 respectively. In Fig. 3.13, the battery current (x_1) and output voltage (x_2) of boost converter, and output current (I_{ac}) and output voltage (V_{ac}) of inverter are shown. The experimental results are discussed here for sudden load removal and load application.

(a) Load application Test: A 1 kW-inverter load is applied suddenly at the output of boost converter. The bus voltage shows an undershoot of 8% (approx). It takes 50 *ms* to regain the normal operation within AVVR. The input current of battery, output current and output voltage of inverter are also shown. The battery current and output current of inverter show overshoots at load application but settle within 80 *ms* without oscillations. The inverter AC voltage shows small change.

(b) Load Removal Test: At the removal of the complete inverter load, the bus voltage shows an overshoot of 3% (approx), and settles at 375 V in 160 *ms* without showing any oscillations. The output voltage of the inverter shows small rise. Nonetheless, the battery current and inverter output current shows negligible oscillations at load removal.

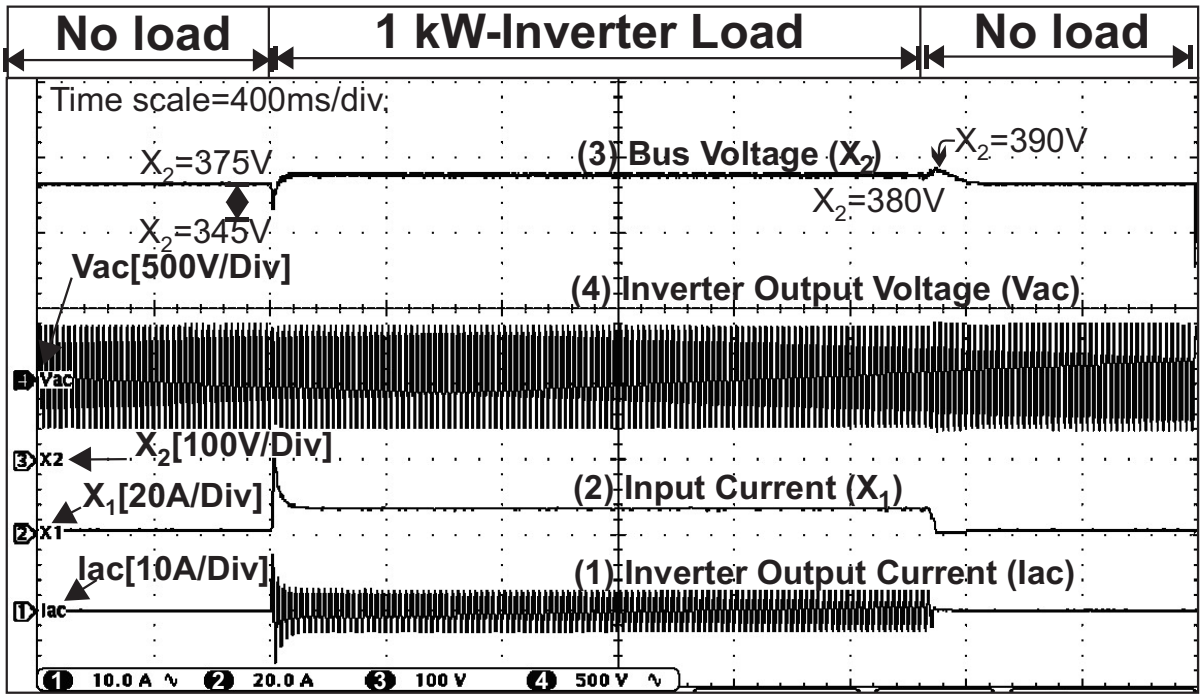

Figure 3.13 : Experimental results of Test Case-II using proposed controller

In Fig. 3.14, similar results as in Case-II, are shown for intermediate load variation from 0.6 kW to 1 kW and vice-versa. The bus voltage shows negligible overshoot at load removal and an undershoot of $< 5\%$ at application of load.

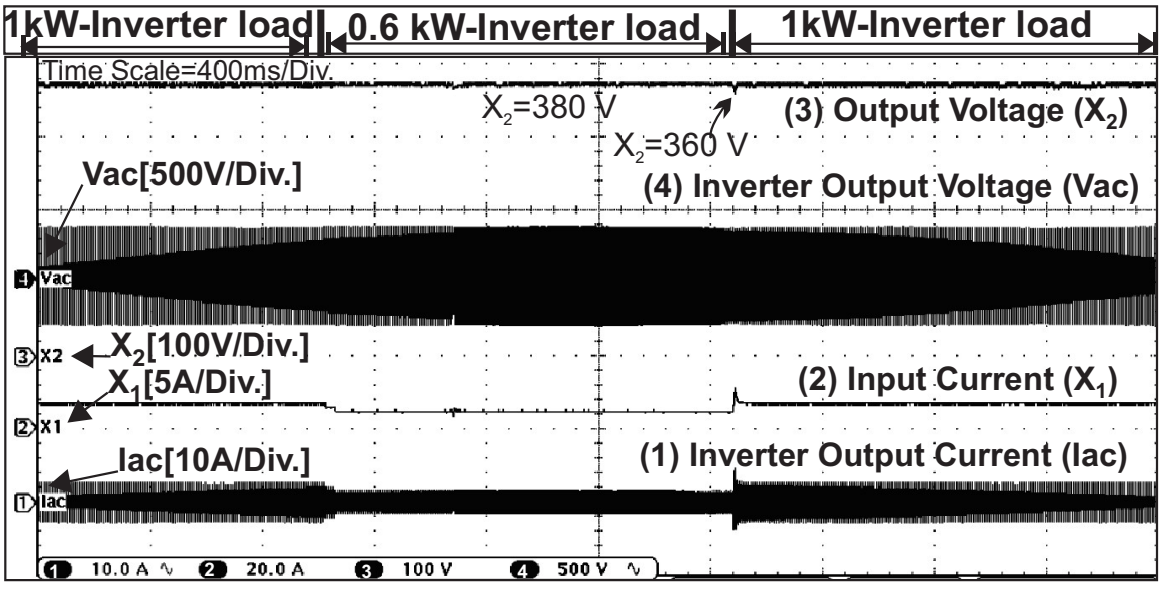

Figure 3.14 : Experimental results of Test Case-II for load variation from 0.6 kW to 1 kW and vice-versa

Test Case-III Variation in input voltage (*E*): The experimental results of Test Case-III are shown in Fig. 3.15. The input power supply is switched-OFF suddenly and switched-ON again. No oscillations in the bus voltage are observed at the switching-OFF the input power. Also, at the re-application of input source, the voltage rises to reference voltage within 80 *ms* without any oscillations. The experimental results (shown in Fig. 3.11-Fig. 3.15) are summarized in Table 3.4.

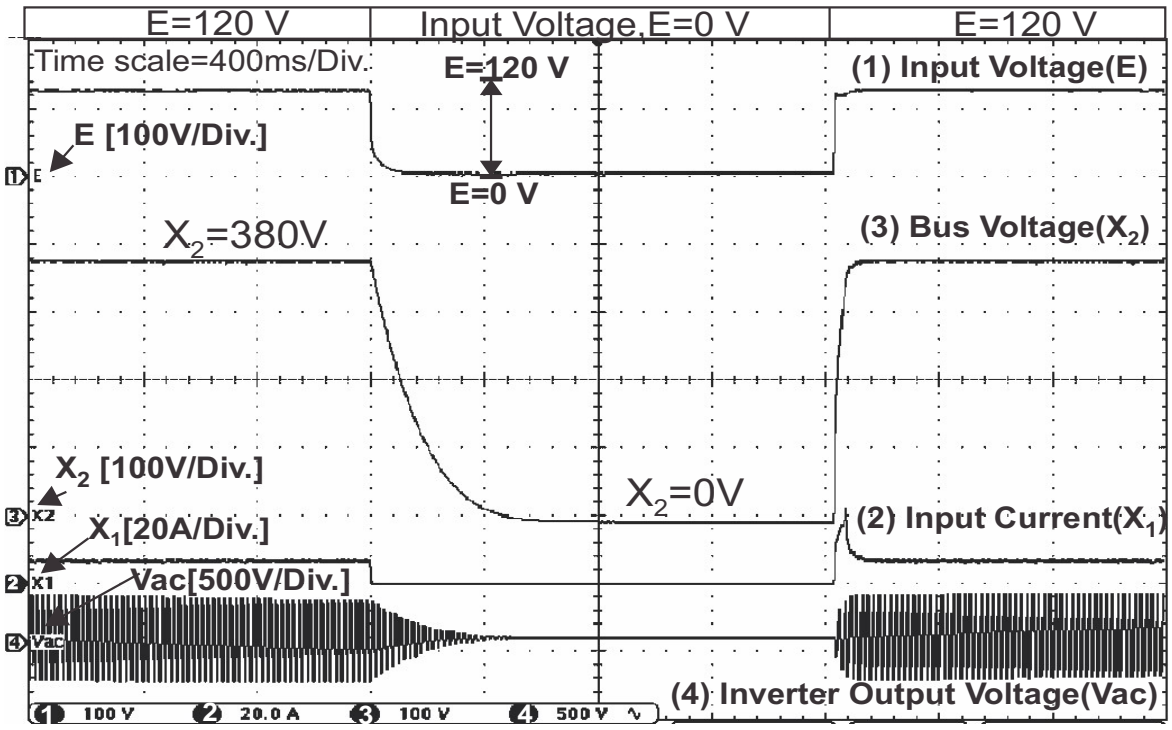

Figure 3.15 : Experimental results of Test Case-III: Variation in input voltage

Additionally, the results for Test Case-II are shown for Solar-PV as source in Fig.3.16.

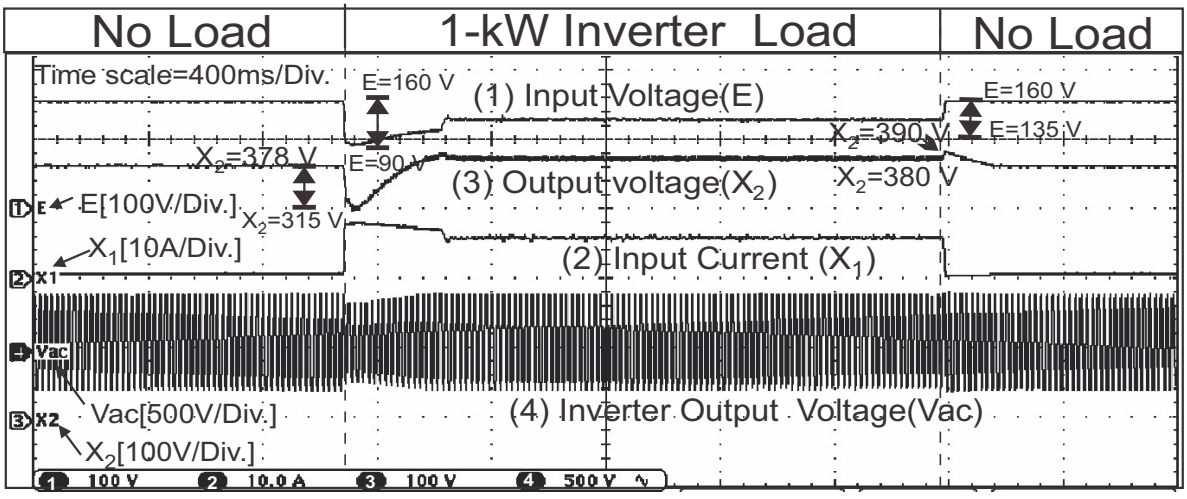

Figure 3.16 : Experimental results for Test Case-II with Solar PV as source

As the input voltage is not regulated one, bus voltage shows a larger undershoot of 16% (approx) at load application and an overshoot of 3% (approx) at load removal in Fig. 3.16. However, the bus voltage is recovered in 320 *ms* (at load application) and 160 *ms* (at load removal) respectively. This concludes that the experimental results validates the effectiveness of the proposed controller in ripple reduction and system dynamics performance. The proposed controller is robust against the line and load transients. The capacitor needed at output of the bus is, 1-mF only; far smaller than used in conventional methods.

Table 3.4 : Comparison of experimental results

Parameter	**Nonlinear Compensator** [Ahmad *et al.*, 2012]	**Proposed Controller**
% Peak to Peak ripple in input current	1.8%	$< 1\%$
Load variations		
Bus voltage undershoot/overshoot	$-7.4\%/+7.4\%$	$-8\%/+3\%$
Bus voltage recovery time	300 *ms*	$<$ 160 *ms*
Line (input voltage, E) variations		
Bus voltage oscillations at complete switch-OFF/switch-ON	– –	No
Bus voltage tracking time on switch-ON	– –	$<$80 *ms*

3.6 SUMMARY

In this Chapter, the SHC ripple mitigation at the input of the boost-derived DC-DC-AC two-stage converter using sliding mode control approach have been presented. The basic concept of the proposed ripple-reduction technique is based on the output-impedance shaping. The proposed adaptive SMC controller aims to shape the output-impedance of the front-end converter such that the SHC ripple is restricted to flow towards the DC source. The parameter α in the proposed switching function decides the ripple mitigation at the steady-state and dynamic performance at the line-load transients. The parameter α is a power function of the DC-link voltage that makes the switching function an adaptive one. The adaptive nature of the proposed SMC controller ensures ripple suppression at the input for the low value of α at the steady-state. The controller adapts a monotonic increase in the value of α at the line-load transients to limit the overshoot and overshoot. The value of α retains small value as soon as the system states converge to the operating point. The proposed controller has achieved ripple reduction at the input without affecting the dynamic performance. The existence and stability of the sliding mode are established. The robustness with respect to parameter variations has also been established. The proposed controller is validated through simulation and experimentation. The experimental results show that the peak-peak SHC ripple is negligible (1%) in the input current with the respect to the average value. The undershoot and overshoot in the DC-link voltage with respect to the nominal voltage are 8% and -3% at the load-transients for the no-load to full-load test. The undershoot and overshoot in the DC-link voltage are negligible for the line-transients. A comparison of the proposed controller with the existing linear controller and a non-linear compensator has been presented. The proposed controller performs better in comparison to the other considered controllers.

The voltage source inverter i.e. DC-AC converter or DC-DC-AC converter with a capacitor at DC link may suffer the short-circuiting of the switches in the same leg(s) of the inverter at the undesired switching of the switches. This causes a large flow of the current through the switches due to the short-circuiting of charged capacitor across the legs and this leads damage to the system. The impedance source inverters resolve this problem and allow the shoot-through operation of

inverter. The quasi-switched boost inverter is one of the impedance source inverters. However, the inversion operation in q-SBI causes the reflection of SHC ripple at the DC-link. In the next Chapter, a modified version of the adaptive sliding mode controller is presented to mitigate the SHC ripple problem in the quasi-switched boost inverter.