# 5
# OFETs with Bi-layer Dielectric on Flexible Polyamide Substrate

After the successful demonstration of high performance operationally stable OFETs on PET substrate, this chapter is about reducing the cost of the substrate and to utilize the benefits of bilayer dielectrics. The high surface roughness of the polyimide substrate was first planarized using a planarization layer. Two types of OFETs with bilayer dielectric PVP/$HfO_2$ and PVA/$HfO_2$ were fabricated on flexible low-cost Kapton tape substrate with TIPS-pentacene: polystyrene as the active layer. Integrating high-k inorganic dielectric with solution-processed low-k polymer dielectric gives both high capacitance density for low voltage operation and a suitable smooth surface for semiconductor deposition. The fabricated devices were also tested in the inverter circuit with external loads. The results discussed in this chapter have been recently published [Raghuwanshi et al.,2019].

## 5.1 INTRODUCTION

Stability of electrical performance of solution-processed flexible organic devices like organic field-effect transistors (OFETs) has been a mainstream constraint limiting their vast potential as an elemental unit in flexible displays, sensors and RFIDs[Bobbert et al.,2012, Yun et al.,2014, Fiore et al.,2015, Feng et al.,2016, Ling et al.,2019, Shi et al.,2019, Xie et al.,2019]. Instability of the device performance can arise due to the inherent nature of the materials used (ambient stability) and/or externally applied stimuli (thermal, electrical, optical, etc.). Former cause of instability can be alleviated by properly selecting dielectric and semiconductor materials with high air-stability [Lu et al.,2016, Nikolka et al.,2017], whereas the latter can be addressed by several combinatory approaches of high-performance materials and optimized device architecture and processing conditions [Iino et al.,2012, Qi et al.,2015, Li et al.,2018]. Several studies on organic devices have reported highly stable electrical performance with improved device strategies like blending organic semiconductor with polymer dielectric, utilizing bi-layer dielectric, using techniques like blade coating, spray coating etc. Such combined approaches have not only demonstrated the improved device stability but also a noticeable enhancement in their electrical performances. Such combined methodologies have been widely accepted to ameliorate the device performance and stability simultaneously and can be implemented in numerous ways like blends of air-stable organic semiconductors and polymers [Hwang et al.,2012, Pitsalidis et al.,2016], conformal and uniform film deposition method[Diao et al.,2013, Onojima et al.,2013], incorporation of multi-layer dielectric (organic and/or inorganic): each exclusively or in successive combination[Ortiz et al.,2010, Subbarao et al.,2015]. The integration of multi-layer dielectric in OFETs is one of the facile and effective approaches which has been widely accepted to ameliorate the device performance and stability simultaneously.

In this chapter, a collective approach has been presented to augment the long-term electrical stability of flexible OFETs. The proposed methodology unifies two different procedures: incorporation of organic/inorganic hybrid multi-layer insulator in OFET architecture and usage of solution-blends of high-performance and air-stable dielectric and semiconducting materials. Two different kinds of TIPS-pentacene: PS blend based OFETs with hybrid insulating layers of (poly(4-vinylphenol)) (PVP)/$HfO_2$ and polyvinyl alcohol (PVA)/$HfO_2$, fabricated using the proposed scheme have been demonstrated on low-cost flexible Kapton tape substrate with high operational stability.

## 5.2 FABRICATION OF DEVICES

OFETs with hybrid dielectric layers were fabricated on polyimide substrate (Kapton tape with thickness 0.10 mm) in top-contact-bottom-gate architecture, Figure 5.1(a) shows the schematic of the fabricated device. Figure 5.1(b) and (c) show the digital image of the substrate used in the study and top view of the fabricated device respectively. Figure 5.1(d-g) shows the molecular structure of TIPS-pentacene, PS, PVP and PVA respectively.

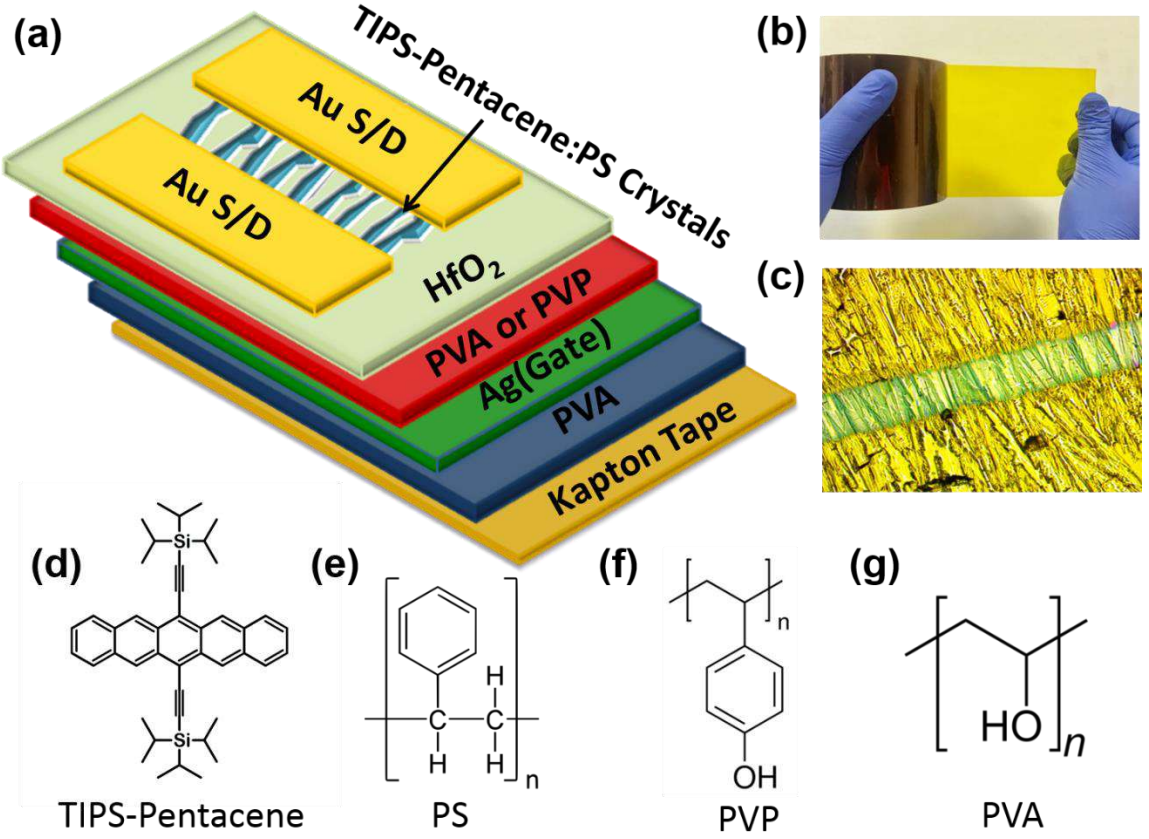


**Figure 5.1 :** (a) Schematic of the bottom gate top contact OFET structure. (b) Digital image of the Kapton tape substrate used in OFET fabrication. (c) Optical microscopic image of the fabricated device from the top. Chemical structure of (d) TIPS-pentacene, (e) Polystyrene, (f) PVP and (g) PVA.

Small pieces of the substrate were pasted on glass slides and cleaned with a high-pressure nitrogen blow to remove the dust particles. To deal with the higher surface roughness of the substrate, thick PVA film was deposited by spin coating above the substrate at 1000 rpm for 60 s, which was later annealed at 60 °C for 10 minutes to evaporate the solvent left. PVA solution was prepared in deionized water with a concentration of 8 wt. % by stirring at 80 °C for 3 h. The 100 nm thin gate electrode was then deposited over the PVA layer by evaporating silver (Ag) through thermal evaporation. For type 1 devices, PVP was used as one of the gate dielectric layers. The solution of 3.4 wt.% PVP (MW ~ 25,000) and 1.1 wt. % poly(melamine-co-formaldihyde) (cross-linking agent) was prepared in propylene glycol monomethyl ether acetate (PGMEA) and the solution was stirred at room temperature for 1 day. PVP film was thus deposited on top of the gate electrode by spin-casting the prepared solution at 1500 rpm for the duration of 60 s. The residual solvent was then evaporated by annealing the samples at 80 °C for a few minutes, further to promote the crosslinking process the samples were annealed at 100 °C for 3 h. Whereas, for type 2 devices PVA was used as one of the gate dielectric layers, for which a solution of 4 wt. % PVA was prepared in deionized water by stirring at 80 °C for 3 h and spin-cast for the duration of 60 s at 2000 rpm over the gate electrode, followed by annealing at 60 °C for 10 minutes. The PVP and PVA films were found to have a thickness of 150 nm and 170 nm respectively. For both

type 1 and type 2 devices after polymer dielectric deposition, a 40 nm thick $HfO_2$ layer was deposited by atomic layer deposition (ALD) at 100 °C. TIPS-pentacene: PS blend was used in a 1:1 ratio by volume for active layer deposition and the layer is formed by the drop-casting method. The blend solution was used to avoid dewetting, improve the active layer coverage and enhance the electrical performance of OFETs. Drop casting was selected over other deposition methods as it yields high crystallinity in crystallites and large grain/crystallite sizes due to ample solvent evaporation time and is especially suitable for TIPS-pentacene deposition. The Au Source-Drain electrodes were deposited by thermal evaporation system under high vacuum using shadow masks. All the fabrication processes were carried out in ambient conditions. Electrical characterizations were carried out in ambient condition and the environmental conditions were maintained relatively constant around characterization setup. Characterizing and analysis tools are similar as discussed in chapter 2. The capacitance density (Ci) was measured from fabricated metal-insulator-semiconductor (MIS) structures for both types of devices and found to have values of 9.3(±1.75) nF/cm$^2$ and 8.0(±1.26) nF/cm$^2$ for type 1 and type 2 devices respectively.

## 5.3 RESULTS & DISCUSSIONS

### 5.3.1 Surface Morphology and Crystallinity Characterization

Figure 5.2(a) and (b) show the surface morphology of the $HfO_2$ layer grown on top of the PVP and PVA layer for type 1 and type 2 devices respectively. $HfO_2$ layer on both kinds of devices has shown very smooth surface morphology with the root mean square (RMS) roughness (Rq) value of 0.84(±0.08) nm for type 1 device and 0.61(±0.05) for type 2 device. In general, the higher surface roughness and irregularities at the dielectric-semiconductor interface adversely affect the device performance, as these irregularities affect the morphology of the semiconductor and act as physical traps to the charge carriers [Fritz et al.,2005, Sun et al.,2010]. The polymer dielectrics (PVP, PVA) used in this study played a vital role to achieve such smooth surface morphology in the bilayer dielectric. The resulted smooth dielectric surface is suitable for ordered growth of semiconductor crystals with lesser traps at the dielectric-semiconductor interface and has a positive impact on the device performance.

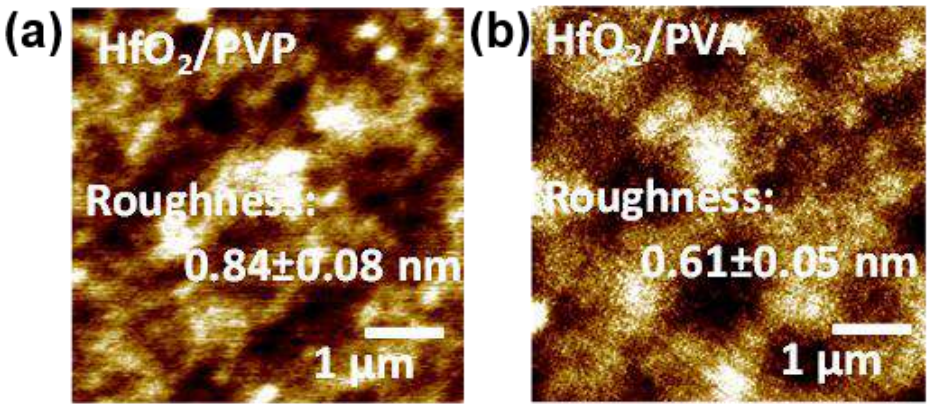


**Figure 5.2 :** Surface morphology of $HfO_2$ layer grown over (a) PVP and (b) PVA layer.

The X-ray diffractogram for TIPS-pentacene crystals on both types of devices is shown in Figure 5.3. The figure affirms a high degree of crystallinity in crystals obtained on both types of devices. The high crystallinity in crystals can be attributed to slow solvent evaporation due to the presence of PS in the solution. The full width at half of the maximum (FWHM) value was found to lesser for type 2 device with a value of 0.04 as compared to type 1 device with a value of 0.08. The difference in FWHM value can be attributed to the difference in surface roughness of $HfO_2$ for the two types of devices, which results in semiconductor crystals to be relatively crystalline in type 2 devices compared to type 1 devices.

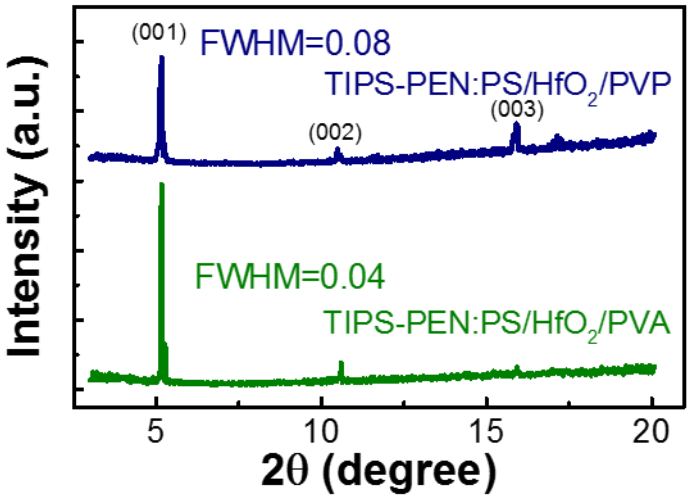


**Figure 5.3 :** XRD pattern for TIPS-pentacene: PS crystals obtained for type 1 and type 2 devices respectively.

### 5.3.2 Electrical Characterization

Figure 5.4 shows the transfer and output characteristics for representative type 1 and type 2 device respectively. Both types of devices have shown excellent p-channel characteristics with the average and maximum field-effect mobility of 0.25(±0.10) and 0.37 $cm^2\ V^{-1}\ s^{-1}$ for type 1 devices and, 0.35(±0.18) and 0.69 $cm^2\ V^{-1}\ s^{-1}$ for type 2 devices respectively. Similarly, near-zero threshold voltage and high current on-off ratio ($I_{on}/I_{off}$) of the order of $10^4$ were achieved for both cases while operating at a relatively low operating voltage of -10 V.

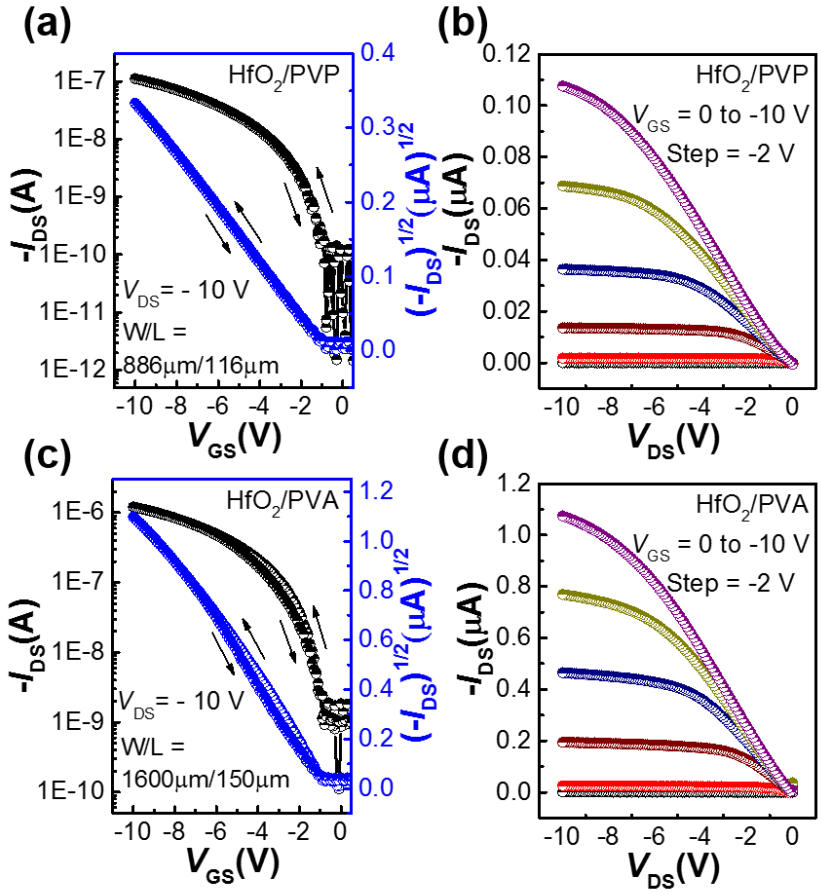


**Figure 5.4 :** (a), (b) Transfer and Output characteristics of the representative type 1 and (c), (d) type 2 OFETs.

The various electrical parameters are summarized in Table 5.1 for both types of devices. The performances of these devices on polyimide substrate were found to be comparable to

various recently reported OFETs on glass and the silicon substrate. Such high performance in these devices can be attributed to many possible reasons. One of which is the smooth dielectric-semiconductor interface obtained due to the process of vertical phase separation, another reason can be the approach of utilizing the benefits of bilayer dielectric with the inorganic dielectrics grown above the polymer dielectric. Various previous studies suggest that the devices suffer from high hysteresis and instability in the performance of devices due to the hydroxyl groups present in the dielectric layer [Lee et al.,2006, Kim et al.,2008, Huang et al.,2013]. The presence of the hydroxyl groups in the dielectric layer are known to destabilize the performance of the devices as these hydroxyl groups absorb water molecules from the ambient and act as a trap to charge carriers. It should be noted that in this study $HfO_2$ layer is grown above the polymer dielectric (PVA or PVP) and both these polymer dielectrics contain polar hydroxyl groups. The high-k dielectric layer grown above these polymer dielectrics acts as an encapsulation layer which doesn't allow the migration of water molecules to the beneath PVA or PVP layer and also restricts the direct contact of the semiconductor film to these hydroxyl group originated traps, thus prevents the trapping of charge carriers and results in high performance of devices. Thus, we have observed negligible hysteresis in both types of devices, with no change in drain current when sweeping from OFF to ON state and ON to OFF state. In addition, type 2 devices were found to have better performance compared to type 1 devices. The better performance of the type 2 devices can be attributed to the highly smooth and trap free interface obtained with PVA dielectric, which is also witnessed by the AFM microscopy as shown in Figure 5.2, which also leads to better crystallinity in the semiconducting film in type 2 devices.

**Table 5.1 :** Summary of the electrical parameters for Type 1 and Type 2 OFETs.

| *Devices* | Capacitace Density (nF/cm²) | $\mu_{sat}$ (cm²/Vs) | $\mu_{max}$ (cm²/Vs) | $V_{TH}$(V) | $I_{on}/I_{off}$ |
|---|---|---|---|---|---|
| **Type 1 (5 devices)** | 9.3(±1.75) | 0.25(±0.10) | 0.37 | -0.88(±0.66) | ~$10^4$ |
| **Type 2 (10 devices)** | 8.0(±1.26) | 0.35(±0.18) | 0.69 | -0.58(±0.71) | $10^4$-$10^5$ |

### 5.3.3 Operational Stability

Further, to investigate the long-term air stability of these devices, the devices were kept in an ambient environment with humidity value ranging from 20-30 % and electrical measurements were carried out at regular intervals for a period as long as 5 months. The major factor that affects the performance of the device in ambient is the moisture present in environmental conditions. These water molecules settle at the interface of the dielectric-semiconductor or in the bulk of the semiconductor and act as charge trapping site, also these water molecules get trapped in the dielectric layer. Trapping in the dielectric layer is more pronounced in polymer dielectrics which contain polar hydroxyl groups. Upon application of the gate voltage, these trapped water molecules get polarized and affect the device performance which results in high hysteresis in transfer characteristics, which leads towards operationally unstable devices. Figure 5.5 (a) and 5(b) shows the transfer characteristics of the representative devices measured at regular intervals for type 1 and type 2 devices respectively and the variation in device parameters such as the mobility and threshold voltages for the set of 5 devices for type 1, and 6 devices for type 2 are shown in Figure 5.5 (c) and (d) respectively. The extracted device parameters reveal the high operational stability of these devices under storage in the ambient environment. Such excellent stability under ambient conditions can be largely attributed to the air-stable and water repellent nature of the TIPS-pentacene: PS blend film. TIPS-pentacene is air-stable in nature and the functional groups at 6 and 13 positions are known to protect the molecule from oxidation under ambient conditions. Also, the TIPS-pentacene: PS film is reported to be

hydrophobic in nature, which further aids in the ambient stability of devices. Another reason for such long-term stability is the concept fabrication technique of encapsulating the polymer dielectrics (PVP and PVA) with a high-k $HfO_2$ layer which restricts the trapping of water molecules in the polymer dielectric layer and thus prevent the degradation of the dielectric layer.

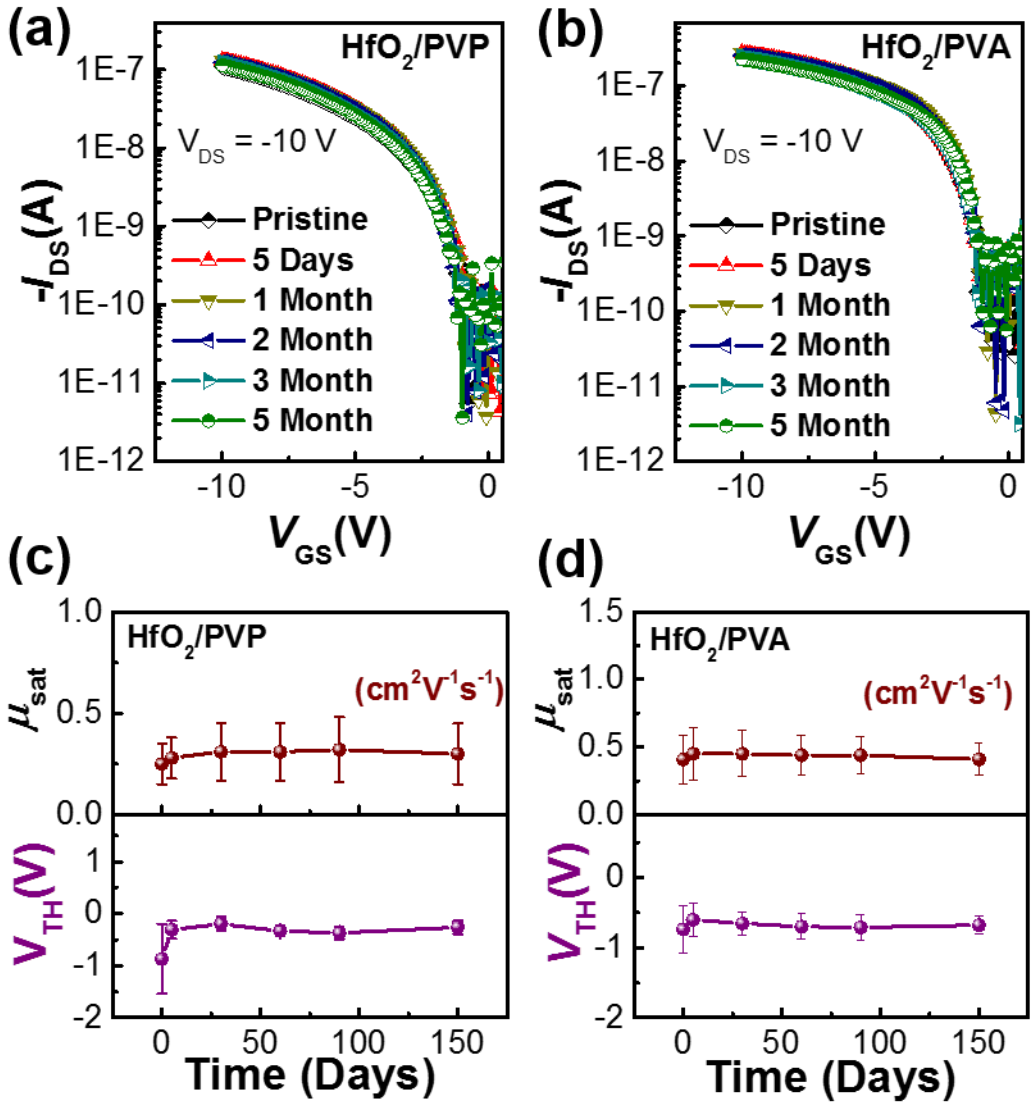


**Figure 5.5 :** Transfer characteristics of the representative devices measured at regular intervals during storage in the ambient environment for (a) type 1 and (b) type 2 device. The plot of variation in $\mu_{sat}$ and $V_{TH}$ with ambient storage time for (c) type 1 and (d) type 2 device.

In addition, the device stability in environmental conditions was tested through the gate bias stress stability test. Figure 5.6 (a) and (b) show the normalized drain current decay characteristics for both types of devices taken at a regular interval of time for 5 months. Each time the devices were given the stress condition of $V_{DS} = V_{GS} = -10$ V for 1 h. Under constant bias stress, the drain current decays for both types of devices in all cases due to trapping of charge in various regions in the device, importantly at the dielectric-semiconductor interface. It was observed that for the pristine case type 1 and type 2 devices have shown drain current decay of ~17 % and ~10.3 % respectively after the application of bias stress for 1 h. In addition, the storage of devices in ambient also leads to increasing trapping cites due to the presence of water molecules in the environment, thus an increase in current decay can be visualized for both types of devices with the storage time. The maximum drain current decay for type 2 devices in 5 months was observed to be ~ 15.5 %, whereas for type 1 device the maximum decay was found to be 26 %.

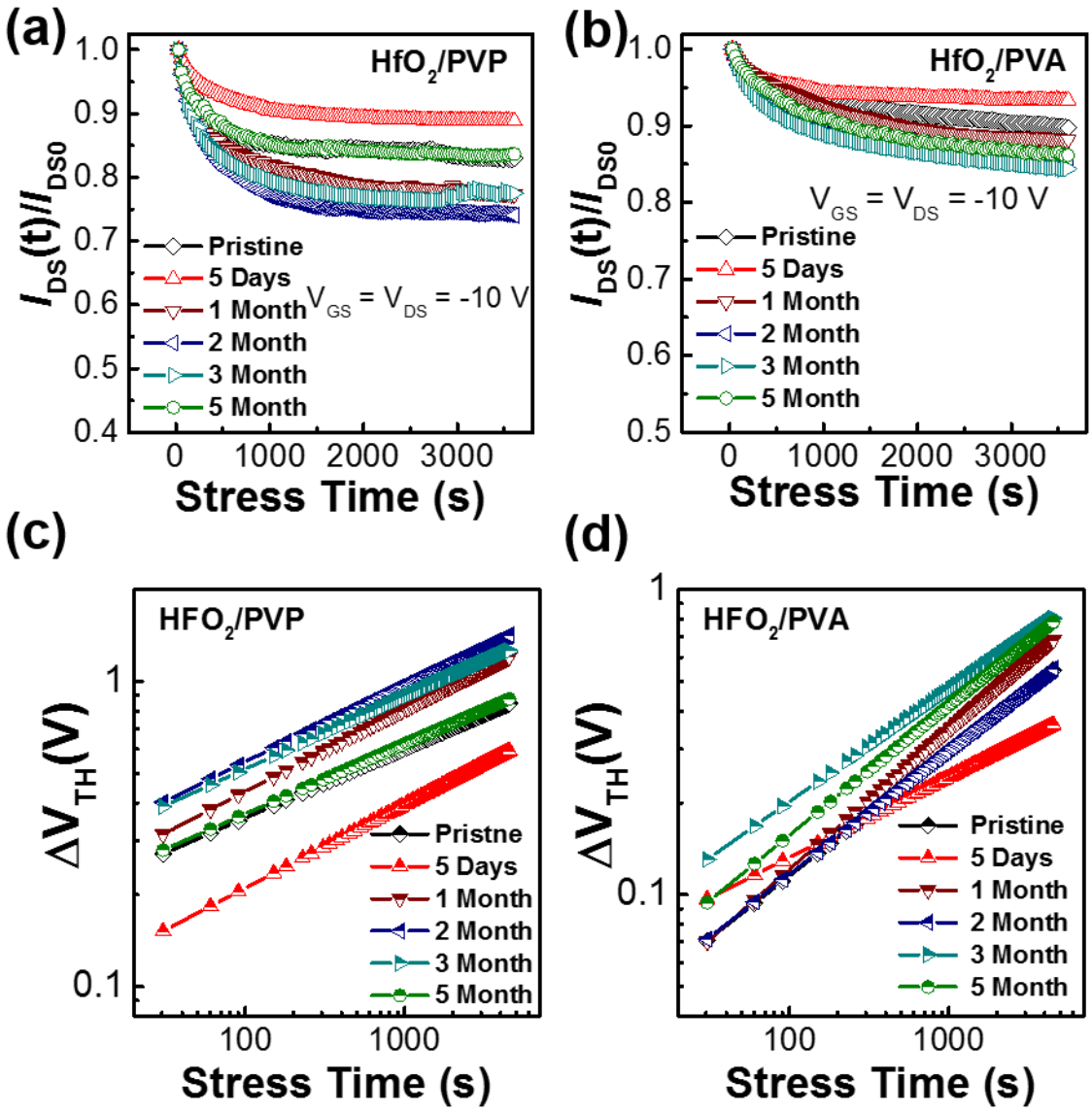


**Figure 5.6 :** Effect on bias stress induced normalized drain current decay after exposure of devices in ambient environment for (a) type 1 and (b) type 2 device. Threshold voltage shift as a function of stress duration after exposure to ambient environment up to 5 months for (c) type 1 and (d) type 2 device.

In the study both hydrophilic polymer dielectrics (PVP and PVA) are encapsulated with the $HfO_2$ layer, largely eliminating their interaction with water molecules. Moreover, the charge trapping depends on quality of primary dielectric-semiconductor interface, which is developed through vertical phase separation between PS and TIPS-pentacene molecules similarly in both kinds of devices and is largely independent of hydroxyl concentration of buried PVA or PVP films and their state of crosslinking in the present case due to encapsulation provided by overlying $HfO_2$ layer. However, smoother morphology of PVA supports to achieve a smoother morphology of overlying $HfO_2$ and in turn a better quality of TIPS-pentacene: PS interface in corresponding devices. Thus the lesser decay in type 2 devices can be attributed to the smoother semiconductor-dielectric interface as compared to the type 1 devices, which limits the charge trapping at the interface resulting in reduced broadening of the density of states, ultimately leading to a lesser density of trap states.

The bias stress-induced normalized drain current decay in the saturation regime can be expressed by the ratio of the $I_{DS}$ at time t and 0 s, and can be given mathematically by Eq. (2.6). The values for $\tau$ and $\beta$ were extracted for all cases by fitting the experimental data in Eq. (2.6) and the values were utilized to get the corresponding shift in threshold voltage which is shown in

Figure. 5.6 (c) and (d) for type 1 and type 2 devices respectively. The bias stress-induced shift in threshold voltage for the pristine case and the maximum shift during the 5-month ambient storage was found to be 0.57 V and 1 V for type 1 devices and 0.47 and 0.7 V for type 2 devices respectively.

To further investigate the operational stability of devices, 100 continuous transfer characteristics measurement cycles were carried for both type 1 and type 2 devices before and after their exposure to the ambient environment for 5 months. The results obtained in this study are shown in Figure 5.7. Both types of devices have shown excellent operational stability with negligible performance spread over 100 continuous transfer measurement cycles in pristine and even after long-term ambient exposure.

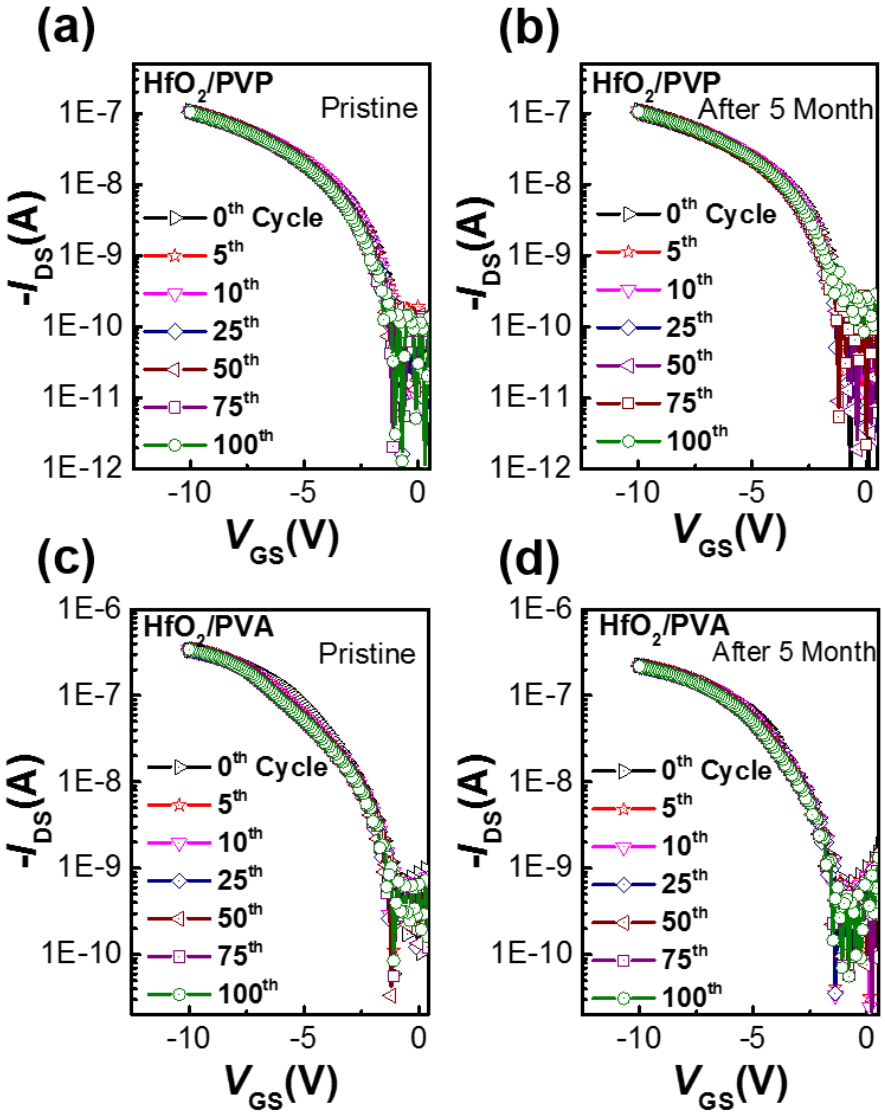


**Figure 5.7 :** Operational stability test with 100 continuous transfer cycle measurements for the pristine case and after exposure to the ambient environment to 5 months for (a), (b) type 1 device and (c), (d) type 2 device.

Further to test the feasibility of these transistors as a circuit component in electronic applications, resistive-load inverters were demonstrated for both types of devices by connecting external load resistance $R_L$ to the fabricated devices. Figure 5.8 (b) and (c) show the static voltage transfer characteristics for type 1 and type 2 devices respectively with the varying load resistance. The resistive loads used in the study were of 26 MΩ, 66MΩ, 106MΩ and 144MΩ. The devices have shown good inverting characteristics while operating well below -10 V. The transfer characteristics reveal that the perfect output high ($V_{out}$ = -10 V) or logic 1 state is obtained with

the low input voltage and a perfect low ($V_{out}$ = 0 V) or logic 0 is obtained at a high input voltage. The transfer characteristics were found to improve with increasing resistive load. The static voltage gain ($dV_{out}/dV_{in}$) is an important parameter for subsequent stage switching and was obtained from the transfer characteristics. The static voltage gain for type 1 and type 2 devices is shown in Figure 5.8 (d) and 5.8 (e) respectively. The calculated maximum gain values were found to be 2.6, 2.8, 3.7 and 3.6 corresponding to 26 MΩ, 66MΩ, 106MΩ and 144MΩ load resistance respectively for type 1 device and were found to have value of 3, 3.1, 3.7, and 6 corresponding to 26 MΩ, 66MΩ, 106MΩ and 144MΩ load resistance respectively for type 2 device.

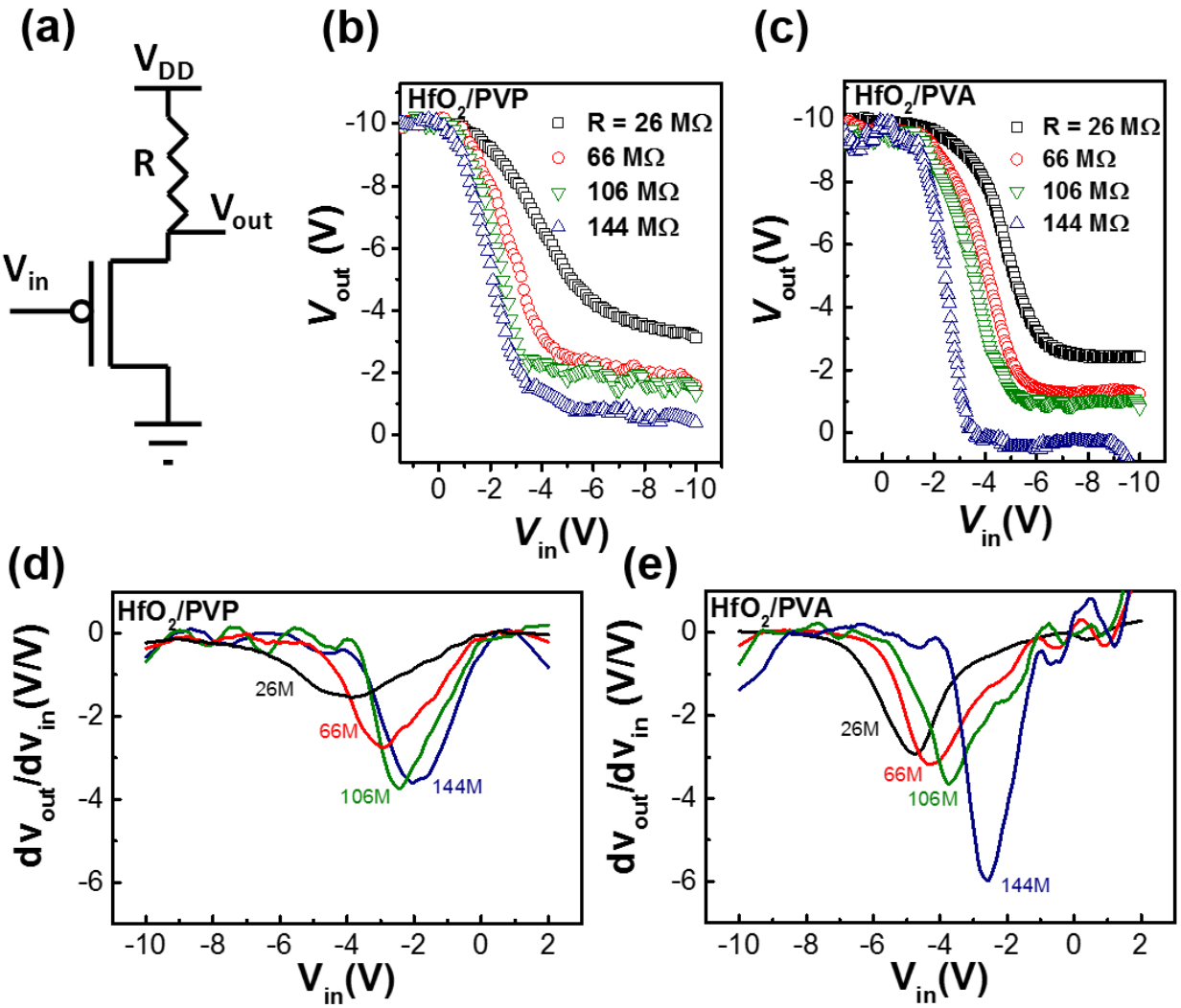


**Figure 5.8: (a)** Schematic representation of the inverter circuit with resistive load, Voltage transfer characteristics of the resistive load inverter circuits with different resistive load for **(b)** type 1 and **(c)** type 2-inverter circuit, Static gain obtained with different resistive load for **(d)** type 1 and **(e)** type 2 device.

In addition, the dynamic response (with $R_L$ = 144MΩ) was also demonstrated for our inverter setup when a square wave switching between 0 and -10 V is applied at gate terminal (Vin). The dynamic switching characteristics are shown in Figure 5.9. For both type of devices, the inverter setup exhibited inverting response by changing the Low/High signal to High/Low signal.

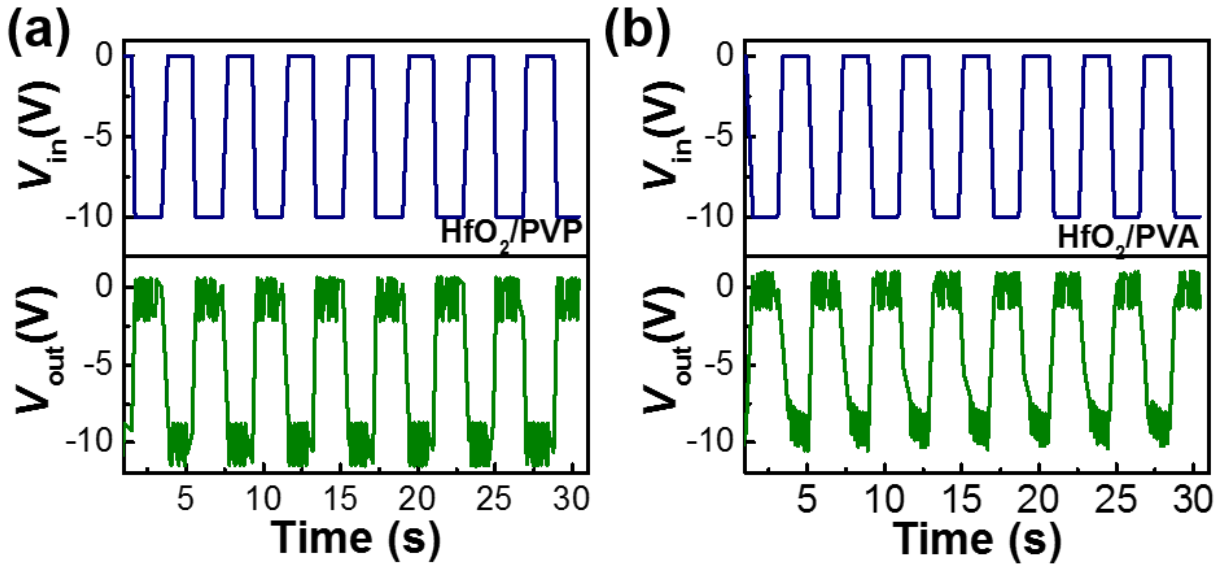


**Figure 5.9 :** Dynamic switching behavior for (a) type 1 and (b) type 2 resistive load inverter with 144 MΩ resistive loads. The upper pulse is the input voltage ($V_{in}$) given and the lower one is the measured output signal ($V_{out}$) for both the cases.

## 5.4 CONCLUSION

In this chapter, OFETs with bilayer dielectric with the inorganic dielectric layer above the polymer insulator are demonstrated and found to have negligible hysteresis, high performance, and operationally stability under ambient conditions on flexible Kapton tape substrate. Maximum field effect mobility of 0.37 $cm^2 V^{-1} s^{-1}$ and 0.69 $cm^2 V^{-1} s^{-1}$ were obtained for PVP/$HfO_2$ and PVA/$HfO_2$ based devices respectively. The devices exhibited avg. and max. field induced mobility of 0.25(±0.10) and 0.37 $cm^2 V^{-1} s^{-1}$ for PVP/$HfO_2$ devices and, 0.35(±0.18) and 0.69 $cm^2 V^{-1} s^{-1}$ for PVA/$HfO_2$ devices respectively with low threshold voltage and $I_{on}$ to $I_{off}$ ratio approaching $10^4$ for both type of devices. Overlapping transfer multiple scans with very less performance variation under ambient conditions were observed. The devices were found to be fairly stable even when electrical stress was applied after a period of 5 months. Devices exhibited small degradation in $I_{DS}$ and small $\Delta V_{TH}$ with high degree of reliability and small performance spreads under combined effects of ambient exposure over a period of 5 months and successive electrical stress. In addition, Inverter based on these OFETs with external load were also demonstrated

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