6
OFETs on Paper Substrate

Along with achieving high performance and operational stability in flexible OFETs, the realization of these devices on substrates that produces lesser electronic waste at the end of the life span is also highly essential. OFETs are generally processable at low temperature and their solution processability aids toward fabrication on the unconventional substrate. Paper is one of those unconventional substrates which has been explored for OFET fabrication because of its advantages of biodegradability, recyclability and of course low cost. Despite these advantages, fabricating OFETs on paper involves various challenges. One of which is the high surface roughness, which is highly undesirable for device fabrication. To overcome the issue a planarization layer is used, which also acts as a barrier layer to the substrate and also provides a smooth surface for device fabrication. In this chapter, OFETs are demonstrated on the paper substrate by utilizing PVA as a planarization layer and the devices were fabricated with bilayer dielectric and TIPS-pentacene: PS blend as an active layer. These devices exhibited remarkable stability under the effects of gate bias stress and a large number of repeated transfer scans with negligible performance spread. In addition, these devices displayed very stable electrical characteristics after long exposure periods to humidity, and excellent shelf life of more than 6 months in the ambient environment. Thermal stress at high temperatures, however, deteriorates the device characteristics due to generation and propagation of cracks in the active semiconductor crystals. Furthermore, novel paper-based phototransistors have been demonstrated with these devices. The outcomes discussed in this chapter have been recently published [Raghuwanshi et al.,2019].

6.1 INTRODUCTION

OFETs which are highly sought after for their applications in display circuitry, RFIDs and sensors truly symbolize the advantages of organic electronics like low cost, lightweight, convenient processing and vast material options over other technology domains. Besides these merits, due to unique advantage of the inherent flexibility in organic materials, OFETs and other organic devices can be successfully realized not only on the conventional rigid substrates like Si and glass but also on unconventional flexible substrates like plastic, paper, and cloth unlike their inorganic counterparts, which are less preferable choices in flexible electronic applications. Incorporation of unconventional substrates like plastic (plastic electronics) [Yi et al.,2012, Schwartz et al.,2013], paper (paper electronics)[Zschieschang et al.,2011, Wang et al.,2017] and cloth (textile electronics)[Choi et al.,2017] in the realization of organic devices is one among several novel research avenues in the area of flexible organic electronics. Plastic electronics have witnessed tremendous advancement in the previous decade with numerous studies conducted on several architectural and procedural aspects. Due to this wide-scale exploration, plastic platforms, even after being costlier than other flexible substrates, remain quite popular globally among researchers for organic device fabrication. However, more economic flexible substrates like paper and cloth suffer from severe microscopic surface non-uniformity and mechanical fragility, which makes the realization of highly stable device performance on these substrates a very challenging task [Tobjörk and Österbacka,2011].

Reports on paper and cloth-based organic devices are rare until recently[Qian et al.,2015, Choi et al.,2017, Wang et al.,2017, Bonacchini et al.,2018]. A few studies report viable device

fabrication on paper substrates and analyze the device performance. High performance and stability have been reported with TIPS-pentacene: PTAA blends OFETs with CYTOP/Al_2O_3 hybrid dielectric on nano-cellulose/glycerol and HD 230 paper substrates [Wang et al.,2015, Wang et al.,2017]. P3HT based OFETs with ion-gel dielectric have also been explored on biodegradable cellulose paper substrates [Qian et al.,2015]. In addition, DNTT based OFETs have shown steep sub-threshold slope with AlO_x-SAM gate dielectric on commercial paper [Zschieschang and Klauk,2015]. However, despite several reports on high-performance paper-based OFETs, the aspect of device stability under external stress conditions remain under-explored. Extensive investigation of this facet of device performance is imperative to address for productive fostering of the field and to cater the increasing demand of solutions to futuristic applications by the route of unconventional electronics.

In this chapter, high performance operationally stable solution-processed organic field-effect transistors have been demonstrated on paper substrate. OFETs have been fabricated using TIPS-pentacene:PS blends on the HfO_2/PVP bi-layer dielectric layer. Even on a non-uniform paper substrate, OFETs exhibit average and maximum mobility values of 0.22(±0.11) and 0.44 $cm^2 V^{-1} s^{-1}$ respectively, avg. threshold voltage of 0.021(±0.63) V and current on-off ratio approaching 10^5. In addition to high performance, devices display remarkable stability under the effects of electrical stress and prolonged exposure to high humidity. Excellent performance and stability arise from the contributing factors of uniform surface morphology, high molecular order and superior interfacial conditions. Moreover, a noticeably long shelf life (more than 6 months) in the ambient environment is recorded for these devices. Thermal stress at high temperatures, however, deteriorates the device characteristics due to generation and propagation of cracks in the active semiconductor crystals. In addition, the realization of paper-based phototransistors is also accomplished with these devices.

6.2 FABRICATION OF PAPER DEVICES

OFETs were fabricated in top-contact bottom-gate architecture on PowerCoat™ HD 230 paper (thickness 220 µm, surface roughness < 20 nm as per manufacturer specifications) from Arjowiggins Creative Papers. All other materials used in the study were purchased from Sigma-Aldrich and used directly without further purification. The substrates with 1-inch × 1-inch size were pasted on the glass slides using Kapton tape and cleaned with a heavy blow of N_2 to remove the dust particles from the surface. A solution of 8 wt. % polyvinyl alcohol (PVA) is prepared in deionized water and stirred at 80 °C for 3 h. For smoothing the paper surface and depositing a barrier layer, the PVA solution was deposited on top of the paper substrate by spin coating at 1000 rpm for 60 s followed by annealing at 60 °C for 10 minutes.

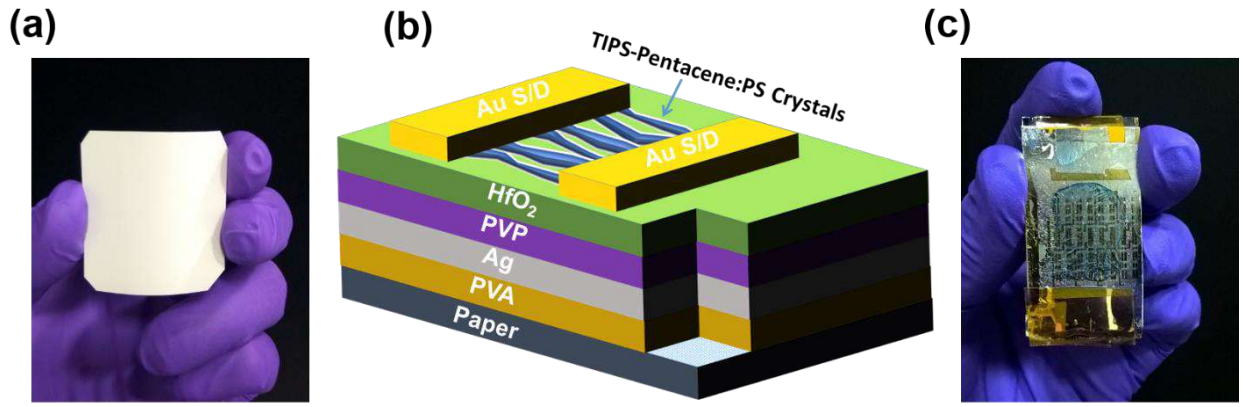

Figure 6.1 : (a) Digital image of the paper substrate, (b) Device structure of the top contact bottom gate TIPS-pentacene paper OFET and (c) Digital image of the fabricated device on paper substrate.

A 100 nm thick silver (Ag) layer is deposited using thermal evaporation to form the gate electrode. A solution of 3.4 wt. % Poly(4-vinylphenol) (PVP, MW ~ 25,000) and 1.1 wt. % poly(melamine-co-formaldihyde) which is a cross-linking agent, was prepared in propylene glycol monomethyl ether acetate (PGMEA) and stirred at room temperature for 24 h. The PVP solution was deposited on the top of the gate electrode by spin coating at 1500 rpm for 60 s to achieve a dielectric layer with a thickness of ~160 nm. Samples were then placed on a hot plate at 80 °C for a few minutes to evaporate the residual solvent, followed by annealing at 100 °C for 3 h to promote crosslinking. A 40 nm thick HfO_2 layer was deposited on the PVP layer, by atomic layer deposition at 100 °C using tetrakis(dimethylamido)hafnium (TDMAH) and H_2O as precursors in a savannah S-200 ALD system from Cambridge nanotech. To make the active organic semiconductor layer, solutions of 0.5 wt. % each of TIPS-pentacene and PS (MW~ 280,000), were stirred in toluene separately for 3 h. After 3 h, the blend solutions were prepared by mixing TIPS-pentacene and polymer stock solutions in a 1:1 ratio by volume, followed by vigorous shaking. The blend solution was dispensed on top of the HfO_2 layer and the substrates were then covered with glass petri-dish to provide a solvent rich environment to the drying film, and left overnight. Later a 200 nm thick Au layer was deposited by thermal evaporation under a high vacuum of 10^{-6} Torr to form Source-Drain electrodes using a shadow mask. Figure 6.1(a)-(c) shows the digital image of the bare paper, the schematic of the fabricated device and the digital image of fabricated devices respectively. All solution preparation and sample processing steps were performed in dark and ambient conditions. The exact channel length (L) and width (W) of the devices were obtained from the length and width of semiconductor crystals joining source and drain regions. Characterizing and analysis tools are similar as discussed in chapter 2. μ_{sat} and V_{TH} were extracted from the highest slope of the linear fit of $|I_{DS}|^{1/2}$ vs. V_{GS} plots using the saturation region drain current equation for standard transistors Eq. (2.1). Value of *Ci* (capacitance density of the gate dielectric layer) for devices has been measured through a metal-insulator-semiconductor (MIS) structure and found to have the value of 9.00(±1.16) nF/cm^2.

6.2.1 Reliability Characterization

To explore the operational stability 100 continuous transfer characteristics measurement cycles, DC bias stress measurement at $V_{DS} = V_{GS} = -10$ V for 3600 s, and transfer characteristics measurement with varying DC bias stress time were performed. To investigate the effect of humidity, the samples were placed inside a small chamber with the constant humid condition (95% RH) for various time intervals and then the electrical measurements were performed immediately after taking the samples out of the humidity chamber after each exposure. To study the effect of annealing temperatures, the devices were annealed at a particular temperature for 1800 s and then the devices were allowed to cool down in ambient and the electrical measurements were then carried out, a similar procedure was followed with increasing annealing temperature. UV irradiation study was performed by illuminating devices with a UV light source having a peak wavelength of 365 nm. The UV source used in the study was a 2 terminal UV LED, which was allowed to be irradiated from the top of the device with a maximum intensity of 1.8 mW/cm^2. To investigate the environmental stability of devices, samples were kept in a petri-dish under ambient conditions and electrical measurements were recorded at fixed intervals until 6 months.

6.3 RESULTS AND DISCUSSIONS

6.3.1 Modification of Paper Surface

Surface morphologies and associated interfacial conditions of each layer involved in OFET fabrication are very crucial factors, which influence the electrical performance of the OFETs very critically. Previous studies have suggested that devices with layers having uniform morphologies and high-quality interfaces tend to show ameliorated electrical performance mainly due to less-hindered charge transport in the improved-quality semiconducting film with fewer defects states[Steudel et al.,2004, Fritz et al.,2005, Yang et al.,2005, Huang et al.,2013]. Figure 6.2 (a) and (b) show the AFM images of the bare HD 230 paper surface and PVA layer (thickness ~800 nm)

deposited over the paper surfaces respectively. The bare paper surface was found to have an avg. surface roughness (Rq) of 11.9(±4.0) nm, which is quite uneven for the OFET fabrication process. To make the substrate viable for further processing, a thick film of PVA was deposited over the paper surface. The polymeric PVA layer was found to be amorphous hence suppressed the surface roughness to a value of 3.3 (±1.1) nm. Figure 6.2(c) and (d) show the AFM image of the PVP and HfO_2 surface which are the major dielectrics used in the study and found to have the surface roughness of 0.88(±0.05) and 0.81(±0.06) nm respectively. Thus, the HfO_2 surface over which the active layer is to be deposited was found suitable with a smooth and uniform surface for viable OFET fabrication. Figure 6.2(e) shows the general terracing structure of TIPS-pentacene crystallite obtained above the bilayer dielectric. Figure 6.2(f) shows the frequency-dependent C_i curve for the PVP/HfO_2 hybrid dielectric layer which demonstrates a very low change in capacitance in a broad frequency range. In addition, the bilayer structure has demonstrated low leakage current density, which is shown in Figure 6.2 (g).

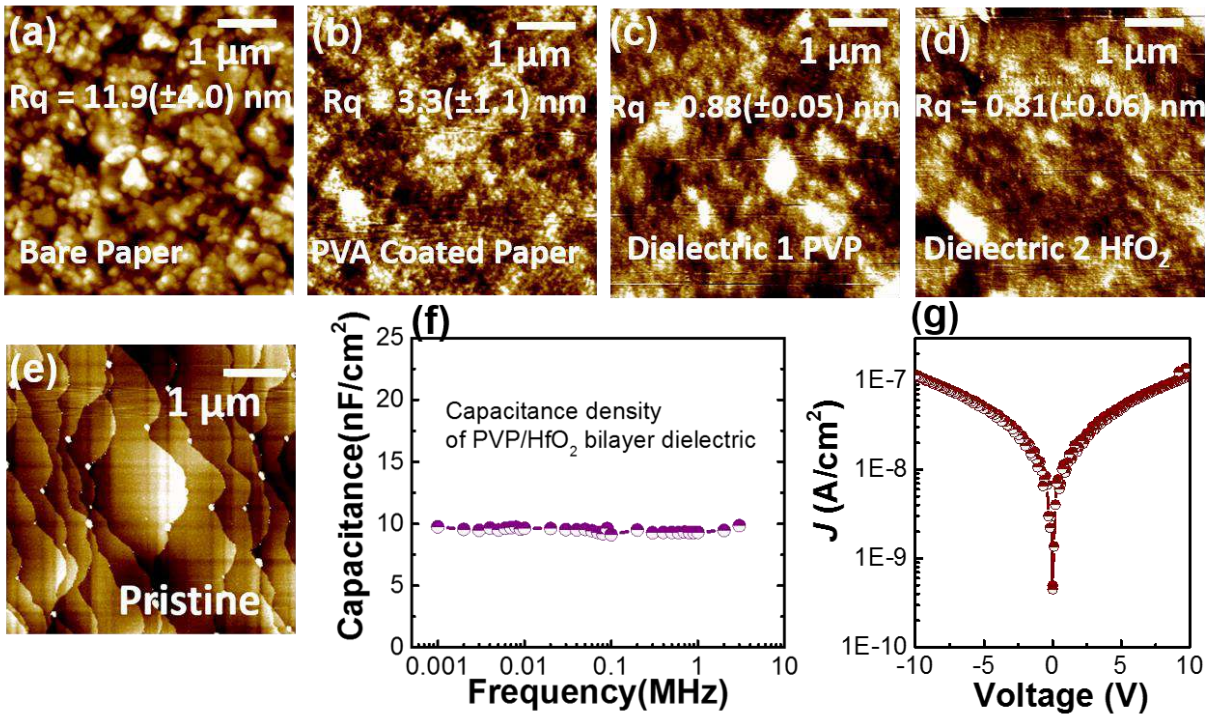

Figure 6.2 : Surface morphology of (a) Bare paper substrate, (b) PVA coated paper substrate, (c) PVP dielectric surface and (d) HfO_2 surface over which active layer was deposited. (e) Surface morphology of TIPS-pentacene crystal (f) *C-f* and (g) *J-V* characteristics for PVP/HfO_2 bilayer dielectric.

6.3.2 Electrical Characterization of Flexible Low-voltage Blend OFETs

Figure 6.3 shows the transfer and output characteristics for a representative device fabricated on PVA deposited paper substrates. The devices exhibited excellent p-channel characteristics with the maximum and average field-effect mobility of 0.44 and 0.22(±0.11) $cm^2 V^{-1} s^{-1}$ respectively, avg. threshold voltage (V_{TH}) of 0.021(±0.63) V, and current on-off ratio (I_{on}/I_{off}) approaching 10^5 with relatively lower operating voltage of -10 V. The summary of electrical parameters extracted from 23 devices is summarized in Table 1. The extracted parameters reveal that despite the uneven surface of the paper substrate, the performance of these paper-based devices is comparable to the many recently reported TIPS-pentacene OFETs on glass and plastic substrates. The high performance of these devices can be attributed to many possible reasons, which include surfaces with smooth morphologies, crystalline behavior of the active layer and high quality of dielectric: semiconductor interface.

The initial PVA layer on the paper substrates acts as a planarization layer and provides a smoother surface morphology for the deposition of subsequent layers. Further, the morphology is improved successively with the deposition of the PVP layer and HfO_2 layer (avg. roughness

0.81 nm), which is well supported by AFM, as discussed earlier. Thus, an ideal surface with very smooth and even morphology is obtained for active layer deposition. The second reason can be the improved degree of crystallinity of the TIPS-pentacene crystal, which is achieved due to enhanced molecular order in the retarded process of solvent evaporation in the drop cast procedure. Another major factor resulting in high device performance is the formation of a uniform dielectric-semiconductor interface in blends of small molecule organic semiconductors such as TIPS-pentacene with polymer binder like PS through the process of vertical phase separation [Smith et al.,2012, Lee et al.,2015]. Vertical phase separation in TIPS-pentacene: PS blends results into a tri-layer structure of TIPS-pentacene:PS:TIPS-pentacene [Madec et al.,2008, Li et al.,2011, Bharti and Tiwari,2016]. A uniform quality dielectric-semiconductor interface thus evolved in OFETs supports charge transport with fewer obstructions along the conduction pathway leading to superior electrical characteristics in the corresponding devices.

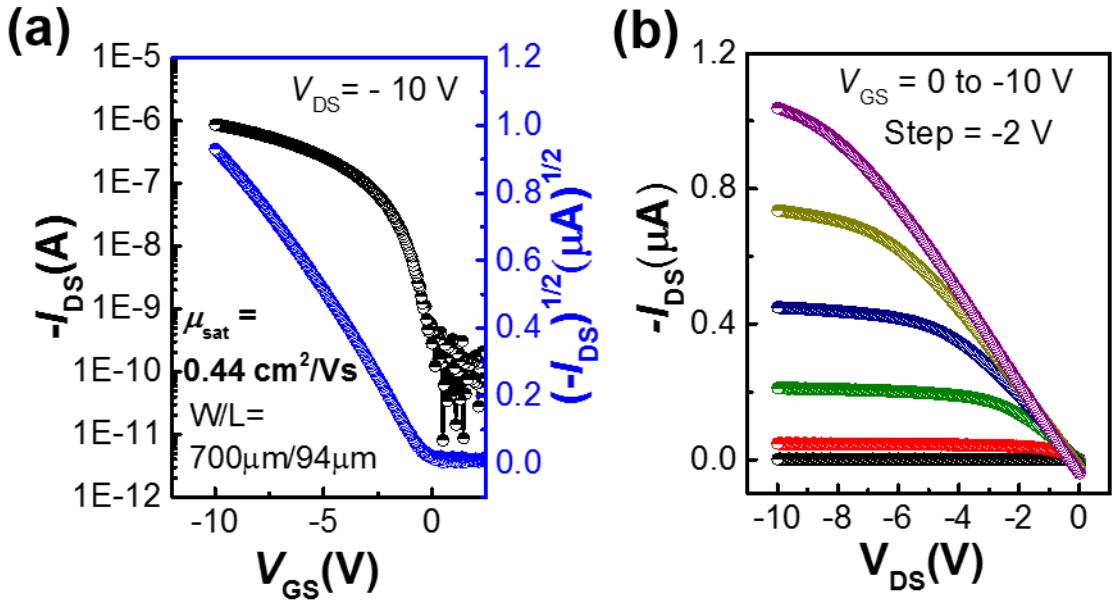

Figure 6.3 : (a) Transfer, and (b) Output characteristics of the representative paper device.

Table 6.1 : Summary of the electrical parameters for the fabricated paper OFETs.

Avg. for	*Capacitance Density (nF/cm²)*	μ_{sat} (cm²/Vs)	μ_{max} (cm²/Vs)	V_{TH}(V)	I_{on}/I_{off}
23 Devices	9.0(±1.16)	0.22(±0.11)	0.44	0.021(±0.63)	10^4-10^5

6.3.3 Operational Stability in Pristine State

The fabricated devices were then tested for operational stability with various tests. First, the bias stress test was performed where paper OFETs were subjected to electrical stress (V_{DS} = V_{GS} = -10 V) for time duration varying from 0 to 3600 s and transfer measurements were performed after each stress time. The effect of varying the bias-stress duration on the transfer characteristics is depicted in Figure 6.4(a). Small changes were observed in device characteristics when stress duration was gradually changed from 0 to 3600 s. This suggests that stress periods as large as 3600 s are also unable to effectively degrade the device characteristics. To investigate the bias stress stability of devices further, a particular device was subjected to electrical stress with the stress condition of V_{DS} = V_{GS} = -10 V for a period of 3600 s. Figure 6.4(b) shows the

normalized drain current decay characteristics for this particular device. Under stress conditions, the ON current decays as a stretched exponential function of time due to charge trapping in various locations including the bulk of the semiconductor, disordered areas of semiconductor, grain boundaries of semiconductor and dielectric-semiconductor interface. The device demonstrated a small decay of 8.5 % in the ON current indicating a smaller number of charge trapping sites and an operationally stable device, also inferred from Figure 6.4(a). Reasons similar to that for high electrical performance can be ascribed to bias stability also. Superior surface morphology, molecular order and interfacial conditions cause less number of trapping sites at various locations, which eventually reduces the charge trapping. This phenomenon is reflected through small decay in I_{DS}, indicating small magnitude of bias stress induced instabilities.

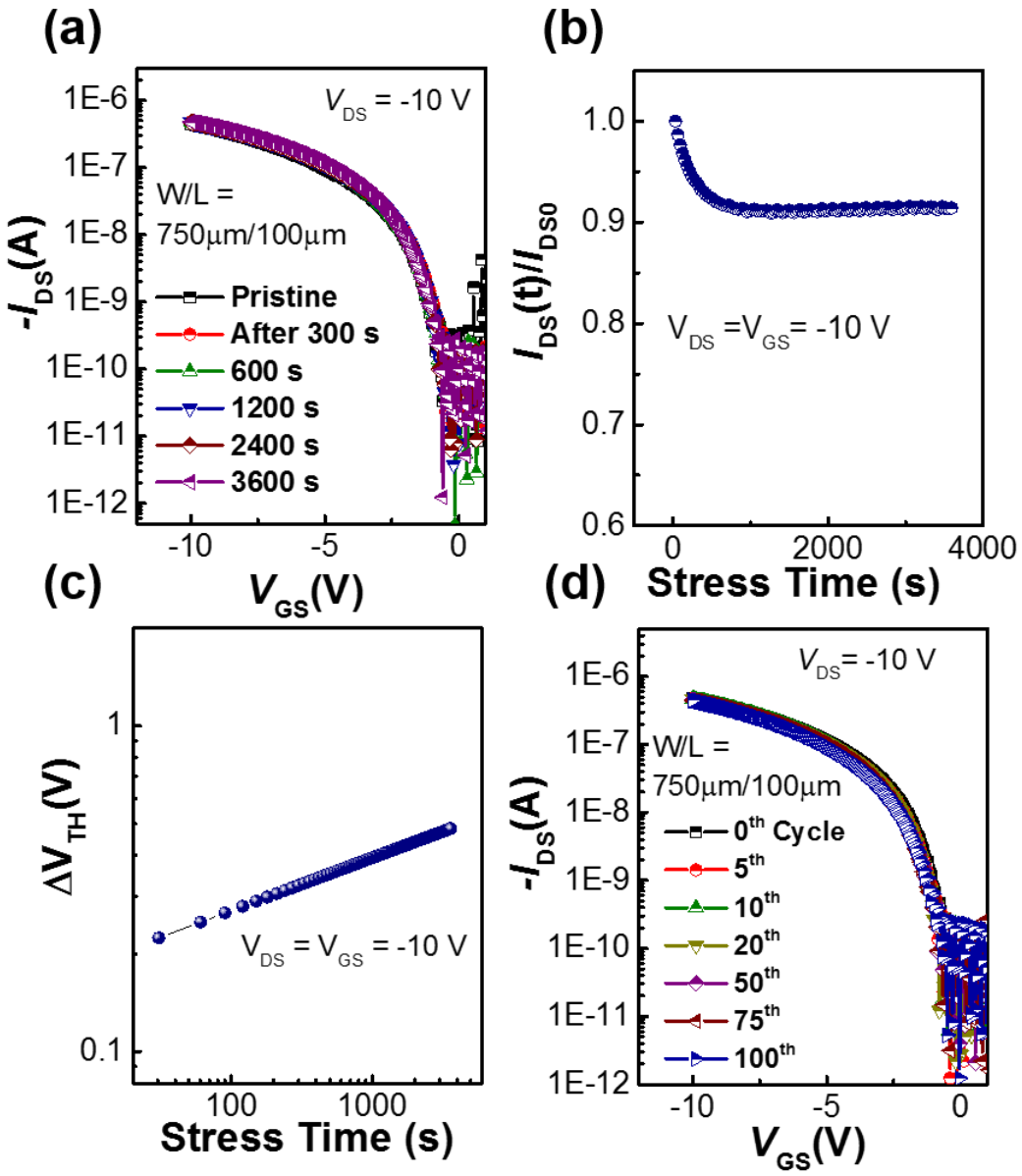

Figure 6.4 : (a) Measured transfer characteristics with increasing bias stress (V_{DS} = V_{GS} = -10 V) duration up to 3600 s, (b) Bias stress induced decay in normalized drain current, (c) Threshold voltage shift as a function of stress duration, and (d) Continuous transfer cycle measurement up to 100 scans.

Mathematically, the normalized decay in the drain current in the saturation regime can be expressed as the ratio of the I_{DS} at time t and 0 s, and can be given as Eq. (2.6). Time-dependent dispersion parameter β (which reflects the width of involved trap distribution) and τ is the relaxation time, a measure of typical trapping time of charge carriers were extracted by fitting Eq.

(2.6) in the experimental data and were found to have values of 2.7×10^{11} and 0.165 for τ and β respectively. Such a high value of τ further reflects less charge trapping leading to an operationally stable device behavior.

The stress-induced shift in threshold voltage can be represented mathematically as a stretched exponential function given as by Eq. (2.7) and is shown in Figure 6.4 (c). It can be deduced from Figure 6.4 (c) that devices experienced only a small shift of 0.4 V in the threshold voltage after undergoing fixed bias stress for 3600 s, again confirming the high stability of devices under large stress durations quantitatively. The electrical stability of these devices was also explored by an alternative route, by subjecting devices to 100 continuous transfer characteristic measurement cycles as shown in Figure 6.4 (d). The devices exhibited very less performance spread with minuscule changes in ON current and threshold voltage. All these outcomes indicate the minimal degree of charge trapping at various locations in the device due to the aforementioned reasons of improved morphology, crystalline order and interfacial conditions, which is reflected through high electrical stability in these devices.

6.3.4 Stability Analysis under Humidity

To test the reliability of devices under extreme environmental conditions investigations were performed under humidity. In this study, the devices were placed in a small chamber with a highly humid environment, and the electrical characterization of the devices was performed immediately after taking samples out in the ambient environment. The successive exposure and characterization process is continued with increased humidity exposure time. Figure 6.5 (a) shows the effect of increasing humidity exposure time on the transfer characteristics of the representative device. The devices exhibited negligible variation in electrical performance even after long exposure periods of 3600 s to extremely humid conditions (95% RH), demonstrating outstanding electrical stability of OFETs on unconventional paper substrate. The plot of variation of μ_{sat} and V_{TH} with humidity exposure time is presented in Figure 6.5 (b).

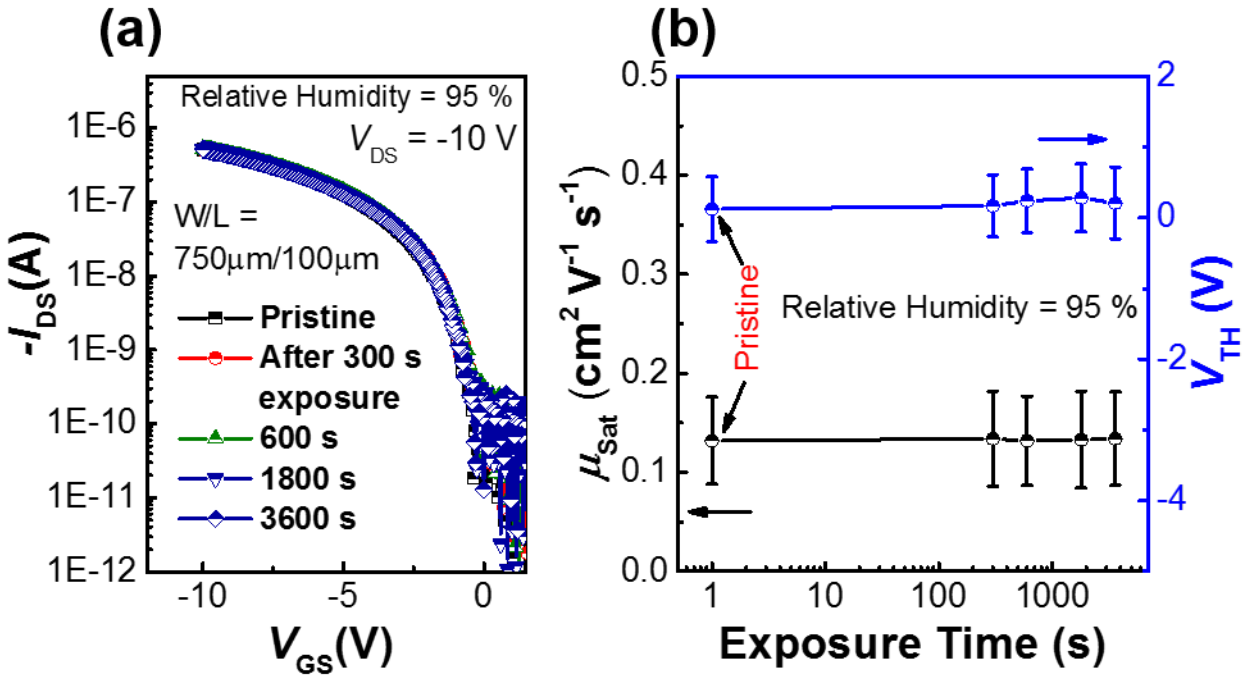

Figure 6.5 : (a) Transfer characteristics scans with varying device exposure time to humidity (Relative Humidity = 95%) and (b) Plot of variation in mobility and threshold voltage with varying humidity exposure time.

For a set of 6 devices considered for investigation, very little deterioration was observed in μ_{sat} and V_{TH} affirming high stability of performance parameters under humid conditions. This remarkable stability of OFETs under highly humid conditions can be associated with the hydrophobic nature of polymeric binder PS, which forms a uniform and high-quality dielectric-

semiconductor interface with TIPS-pentacene during the process of vertical phase separation. PS resists the dielectric-semiconductor interface degradation by repelling the moisture, which could have otherwise initiated severe charge trapping deteriorating the device performance.

6.3.5 Long term Environmental Stability OF Paper OFETs

Furthermore, to explore the long-term environmental stability, devices were exposed to ambient air with humidity values ranging from 20-30 % for a period as long as 180 days and electrical measurements were taken periodically under ambient conditions. Figure 6.6 (a) & (b) show the transfer characteristics of a representative device in logarithmic and linear scale, measured at different time intervals and the extracted mobility and threshold voltage values are shown in Figure 6.6 (c).

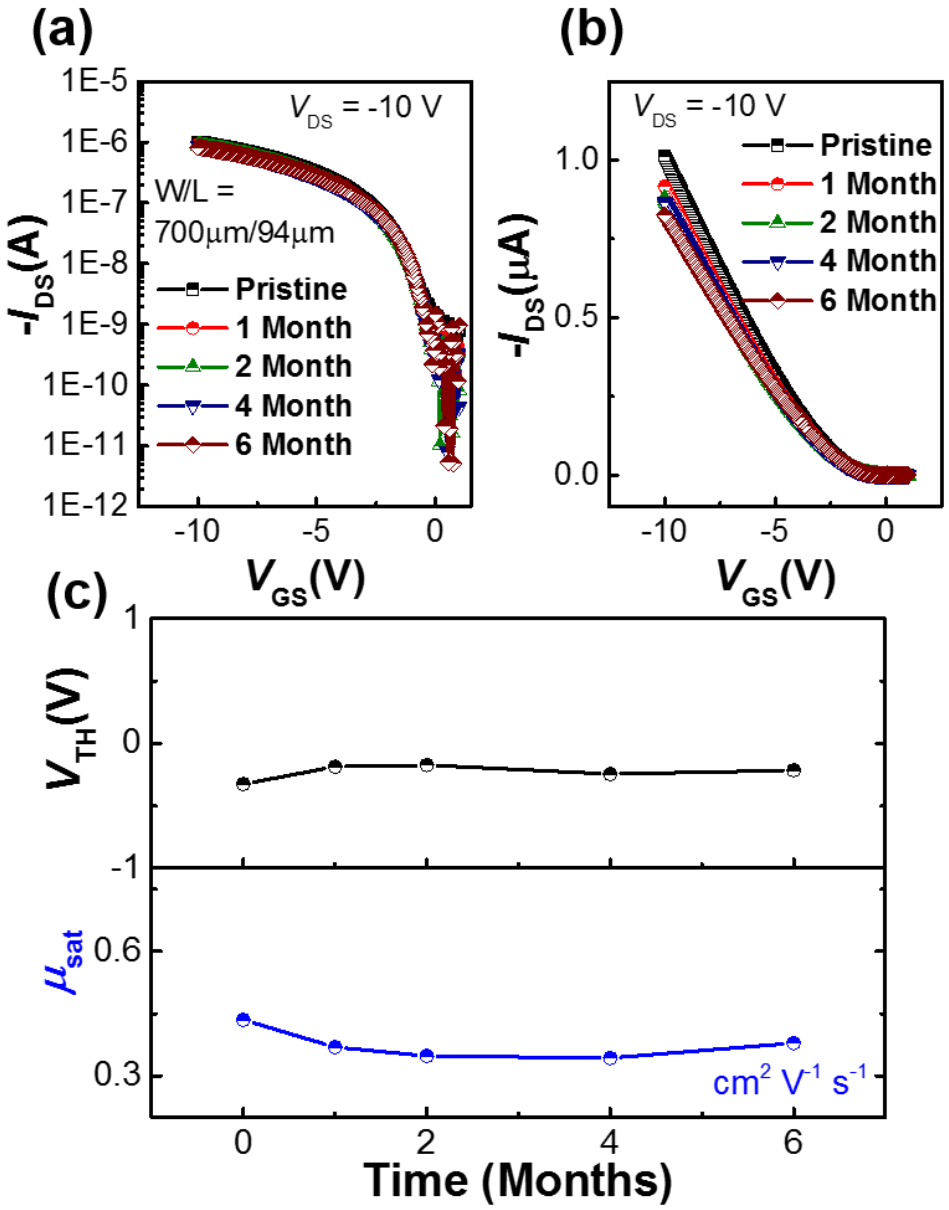

Figure 6.6 : Effect on transfer characteristics of the devices measured during storage in ambient environment for a period of 6 months in (a) logarithmic and (b) linear scale and (c) Plot of variation in mobility and threshold voltage as a function of time (months).

The surface morphologies of the active layer before and after 6-month of environmental exposure are shown in Figure 6.7 (a) and (b) respectively. Both obtained morphologies are the general terracing structure of TIPS-pentacene crystallite and remain unaffected. The invariability

in terracing structure before and after six months of environmental exposure suggests air-stable nature of TIPS-pentacene (further strengthened due to the addition of PS).

It can be observed that even after air-exposure for more than 6 months, there is little change in device performance (ΔI_{DS} = 18.5 %, $|\Delta V_{TH}|$ = 0.15 V, $\Delta\mu_{sat}$= 0.09 $cm^2\ V^{-1}\ s^{-1}$), which indicates outstanding air-stability and long shelf life of the devices under ambient conditions. To the best of authors' knowledge, this is one among the longest shelf life reported for OFETs on paper substrate. Such excellent air stability can be jointly attributed to the air-stable and water repellant nature of the TIPS-pentacene and PS film respectively. The functional groups available at 6 and 13 positions protect the TIPS-pentacene molecule from oxidation under ambient conditions, imparting the air-stable characteristics [Park et al.,2009, Feng et al.,2016]. In addition, the water-repellant nature of PS resists the moisture-induced degradation of TIPS-pentacene: PS interface. These factors lead to preserve the device characteristics for a long time making them suitable for reliable circuit and sensing applications.

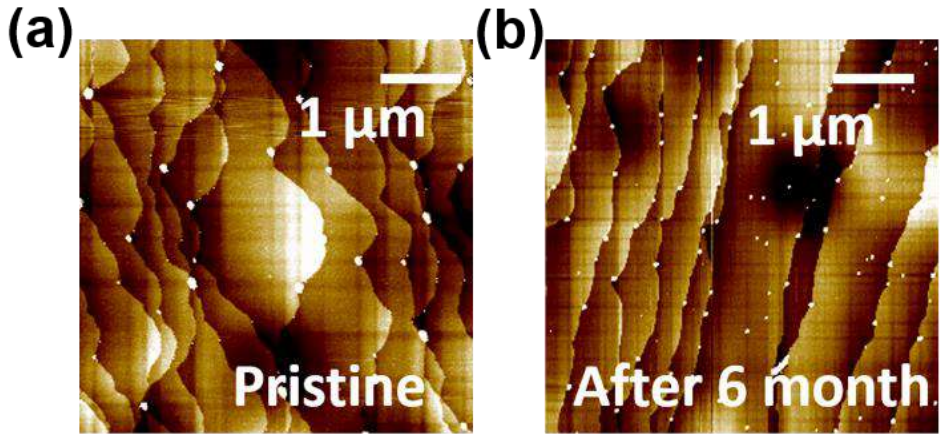

Figure 6.7 : Surface morphology of TIPS-pentacene crystals for (a) pristine and (b) after 6-month environmental exposure.

6.3.6 Effect of Annealing Temperature on Electrical Performance of Paper OFETs

In this study, an analysis of the effect of annealing temperature on paper device performance is demonstrated. To investigate this effect, the paper-based OFETs were annealed at different temperatures varying from 40 ˚C to 100 ˚C for the duration of the 1800s each. The annealing process was immediately followed by electrical characterization. All electrical measurements and annealing processes were carried out in ambient air.

Figure 6.8 (a) shows the variation in transfer characteristics of a representative device, which were acquired after annealing the device at different temperatures. It can be observed from the figure that the transfer curve is shifted a little towards the right for initial annealing temperatures of 40 ˚C and 60 ˚C. In addition, the characteristics of device annealed initially at 40 ˚C exhibits a slight improvement in ON current and threshold voltage (V_{TH}) in comparison to that recorded at room temperature. This initial improvement in the device performance can be attributed to the evaporation of residual solvent and release of any strain present in the active layer because of the redistribution of grains at low-temperature annealing, which eventually leads to improved crystallization and ordered TIPS-pentacene molecules [Bae et al.,2010]. These events thus enhance the molecular ordering and granular arrangements, leading to improved device performance. However, with further increase in annealing temperature, the ON current reduced monotonically with the shift in the transfer curve towards the negative V_{GS} direction that denotes the negative shift in V_{TH}. The plot of variation in various extracted electrical parameters with increasing annealing temperature is shown in Figure 6.8 (b). For a set of 4 devices considered for the experiment, the mobility values were reduced from 0.16(±0.09) $cm^2\ V^{-1}\ s^{-1}$ for pristine case to 0.06(±0.02) after 80 ˚C annealing, which further reduced to 0.03(±0.02) after annealing at 100 ˚C, with a cumulative degradation of 81% in mobility values. The threshold voltage values were

negatively shifted with the value of -0.65(±0.23) for pristine devices to -0.79(±0.03) after annealing the devices at 100 ˚C. The ON current, which was improved on initial low-temperature annealing, further deteriorated by more than two folds after the 100 ˚C annealing.

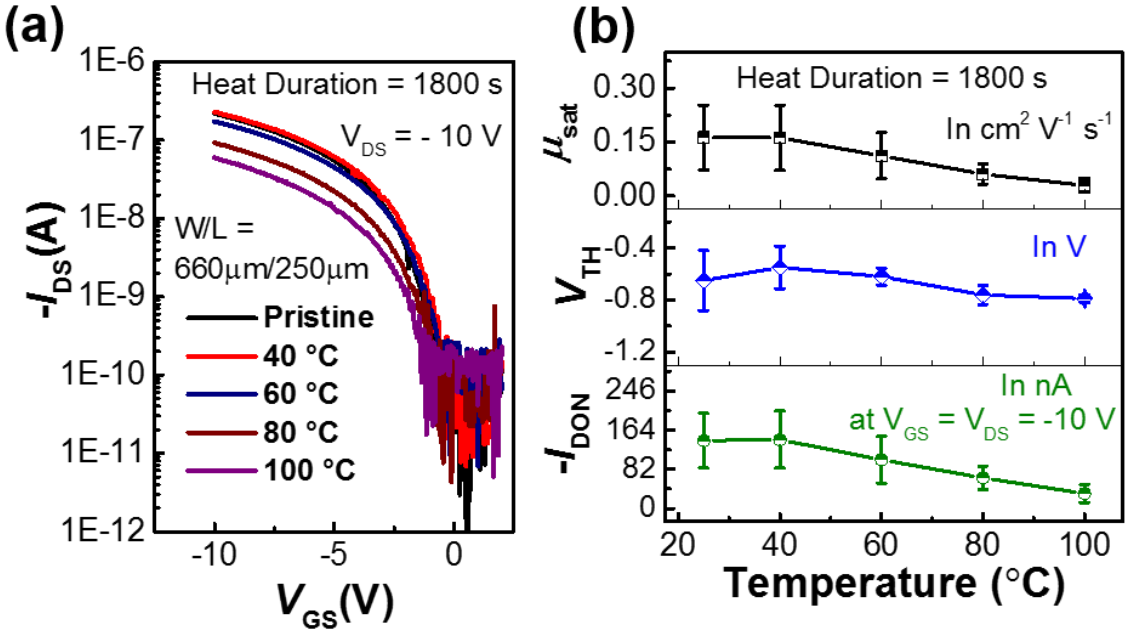

Figure 6.8 : Plot of variation in (a) Transfer characteristics, (b) Mobility, threshold voltage and I_{DON} (maximum ON current at V_{GS} = -10 V) with annealing temperatures.

The performance degradation at high annealing temperature occurs mainly due to the physical degradation of the active layer crystals because of the thermally generated cracks and their propagation. One of the probable reasons for these crack generation may be the inelastic stress developed during the thermal annealing above 60 ˚C [Bae et al.,2010]. These cracks and defects further function as charge trapping centers, leading to reduced device performance. Moreover, the device performance may also degrade due to permanent loss in the crystallinity of the active layer at higher annealing temperatures. To confirm the macroscopic deterioration of semiconducting crystals, optical micrographs of the crystals annealed at different temperatures were captured. It can be clearly observed from the Figure 6.9 (a, b & c) that no cracks were developed in crystals till initial annealing at 60 ˚C as the TIPS-pentacene crystals appear similar to that in the pristine case. However, with further increase in annealing temperature the cracks

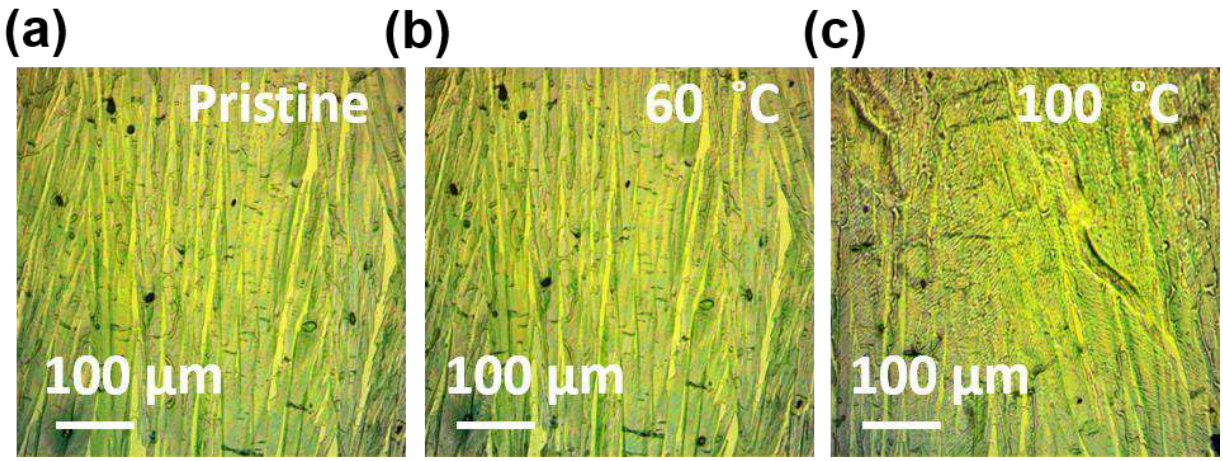

Figure 6.9 : Optical micrographs of semiconductor crystals for (a) Pristine, (b) 60 ˚C, and (c) 100 ˚C annealed devices.

were gradually developed and propagated. After annealing at 100 ˚C (Figure 6.9 (c)), crystals appeared brittle and rough with the evolution of large cracks on their top surface, indicating crystal rupture and concomitant degradation in electrical performance. The AFM images of active layer for pristine and annealed samples were also investigated and are shown in Figure 6.10 (a) and (b) respectively. It can be seen that pristine crystallite has a normal terrace structure, whereas in the annealed crystallite, terrace structure appears faded/flattened with the presence of crack-like features.

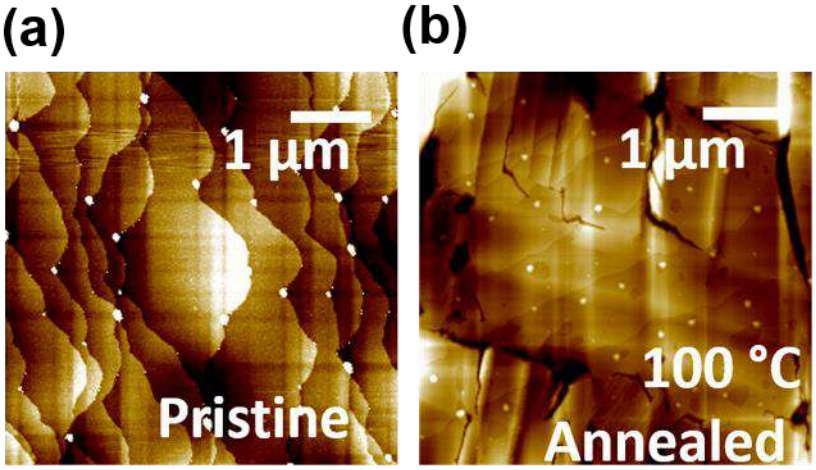

Figure 6.10 : Surface morphology of (a) pristine and (b) 100 ˚C annealed active layer, showing crystal rupture at high-temperature annealing leading to performance deterioration of devices.

Figure 6.11 shows the X-ray diffractogram of the active layer for pristine and annealed samples. It can be observed that the peak intensities were increased a little when the sample was annealed at 60 °C because of improved crystallization and ordering in TIPS-pentacene due to the evaporation of residual solvent and release of any strain present. However, the peak intensity drastically decreased when the active layer is annealed at 100 °C, which is due to the physical degradation of TIPS-pentacene crystals at a higher temperature with the generation of large cracks. Diffractogram results discussed above, are in very good agreement with those obtained from electrical characteristics and optical micrographs.

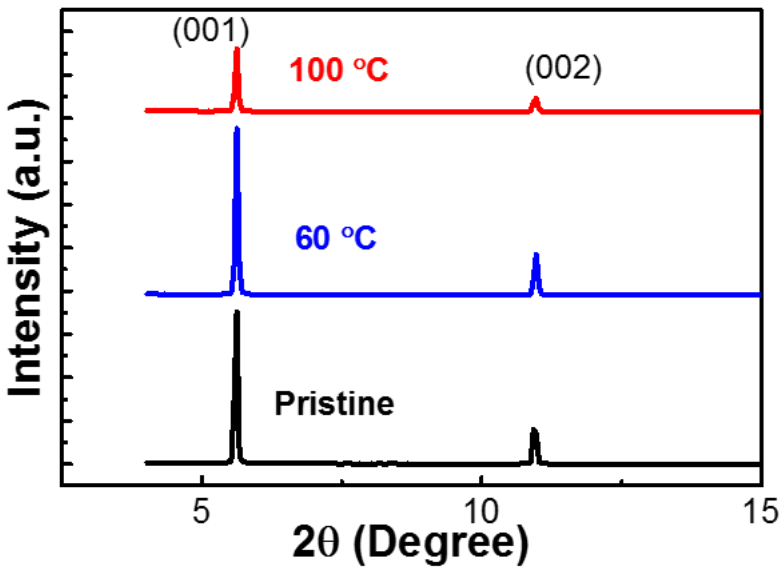

Figure 6.11 : X-ray diffractogram of the active layer for pristine and annealed samples.

6.3.7 UV Sensing with Paper OFETs

To check the utility of these paper OFETs in low-cost sensors they were tested for photo-sensing and was found that these paper-based OFETs can also function as phototransistors. To examine their photo-response, devices were exposed to UV irradiation. Figure 6.12 (a) and (b) show the variation in the transfer and output characteristics of a representative device under dark and UV illuminated conditions. Upon UV exposure, there is a significant change in the transfer curve, with a positive shift of 1.04(±0.53) V in V_{TH} for the four devices under consideration. Their photo-response is a combination of photoconductive and photovoltaic effects (visualized as an increase in the drain current and positive shift in V_{TH} respectively) and is due to widely accepted phenomena of UV photons stimulated exciton-generation in the active layer, their eventual dissociation into free electrons and holes, subsequent collection of holes at drain electrode and trapping of electrons at the interface [Dutta and Narayan,2004, Mas-Torrent et al.,2006].

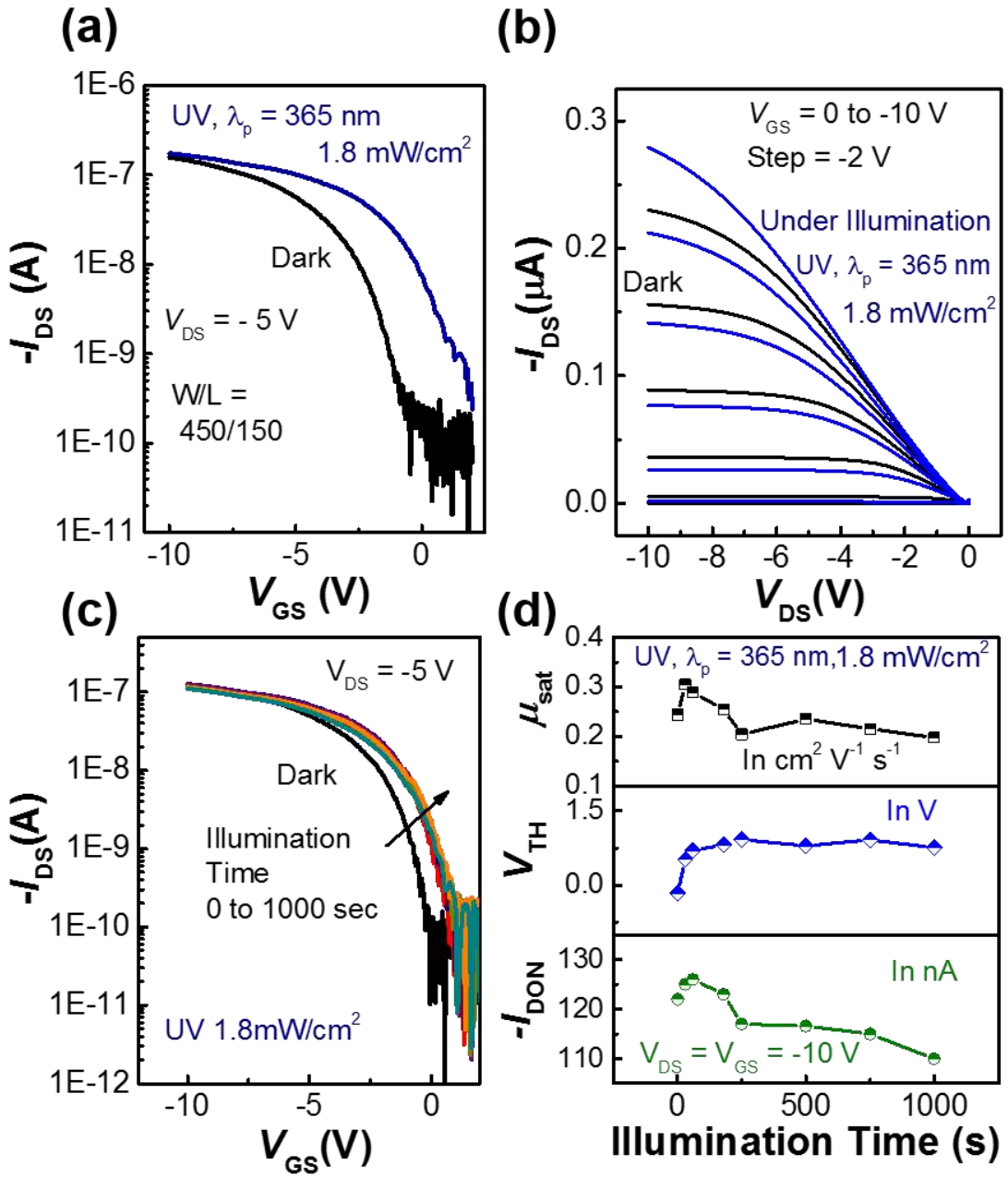

Figure 6.12 : (a) Transfer and (b) Output characteristics of paper OFET under UV illumination. (c) Effect of UV illumination time on the transfer characteristics of the OFET. (d) Plot of variation of mobility, threshold voltage and I_{DON} (maximum ON current at V_{GS} = -10 V) with increasing UV illumination time.

Figure 6.12 (c) shows the effect of increasing illumination time on a representative device, where the characteristics were measured in dark after the illumination for a particular time. As the illumination time increases from 0 to 1000 s, the transfer curve shifts towards positive V_{GS} direction, ultimately resulting in a positive shift in V_{TH}. The increased shift in V_{TH} can be attributed to the increased degree of exciton generation and subsequent minority charge trapping as discussed before. Plot of variation in μ_{sat}, V_{TH} and ON current (at V_{DS} = -5 V & V_{GS} = -10 V) with illumination time is shown in Figure 6.12 (d). The mobility values and ON current continues to degrade after a small initial increment, whereas the V_{TH} increases and saturates with increasing illumination time.

On the initial illumination drain current increases due to prevalent photoconductive effect, whereas at higher values of illumination time, drain current is reduced due to UV induced permanent deterioration (bond rupture and defect generation) of the active layer. It should be noted that this photo-response has been obtained from the solution-processed OFETs on the unconventional paper substrate while operating at lower voltages (5-10 V range). To the best of our knowledge, paper-based phototransistors have been demonstrated for the first time in this study. Such reasonably well performance of paper-based OFETs demonstrates that several other unconventional and highly biodegradable substrates like paper also have the potential to be viably used for various device applications like circuits and various kinds of sensors, despite their rare usage currently.

6.3.8 Paper OFETs with PVA/HfO_2 Bilayer Dielectric

Devices with similar architecture as discussed in section 6.2 were also fabricated using PVA/HfO_2 as a bilayer dielectric combination. The output and transfer characteristics of the typical paper-based representative OFET are shown in Figure 6.13 (a) and (b) respectively. The devices have shown excellent p-type characteristics with a clear linear and saturation region under -10 V operation. Despite having a high surface roughness of the paper substrate, the devices yielded high performance with maximum field-effect mobility of 0.78 $cm^2\ V^{-1}\ s^{-1}$ and average mobility of 0.52 $cm^2\ V^{-1}\ s^{-1}$ with a standard deviation of 0.16, the low threshold voltage of -0.56(±0.24) and an on-off current ratio approaching 10^4 was found for the set of 10 devices. The high-performance in these OFETs can be attributed to the smooth PVA planarization layer that made the paper surface viable for OFET fabrication, which is further planarized by the gate (Ag), PVA and HfO_2 dielectric layers, thus providing a smooth surface for active layer deposition

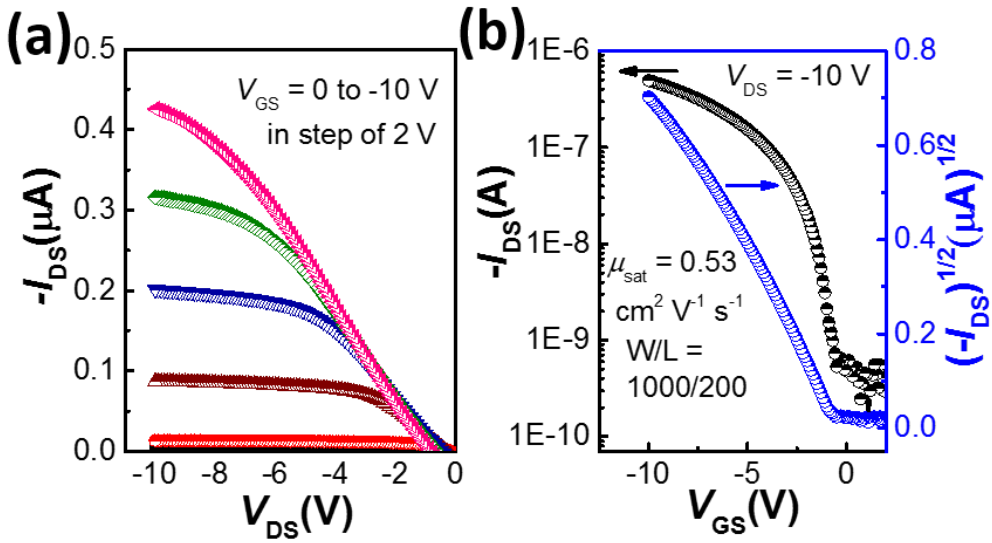

Figure 6.13: (a) Output and (b) Transfer characteristics of the representative paper OFET with PVA/HfO_2 bilayer dielectric.

To check the potential of these paper OFETs towards circuit application, we have demonstrated a resistive load inverter circuit by connecting external loads to paper OFET, with varying resistance. The inset of Figure 6.14 (a) shows the schematic of the external load inverter circuit. The circuit was operated well below -10 V. Figure 6.14 (a) shows the static transfer characteristic of the inverter circuit, it is observed from the graph that the circuit works correctly as an inverter with a clear output high or the logic 1 at low input voltage and a clear output low or logic 0 at high input voltage. However, with increasing the load resistance the transfer characteristics were found to improve because of the higher voltage drop across higher resistance. Figure 6.14 (b) shows the inverter static gain at different load resistance and was found to have the maximum value of 4 for 144 MΩ load.

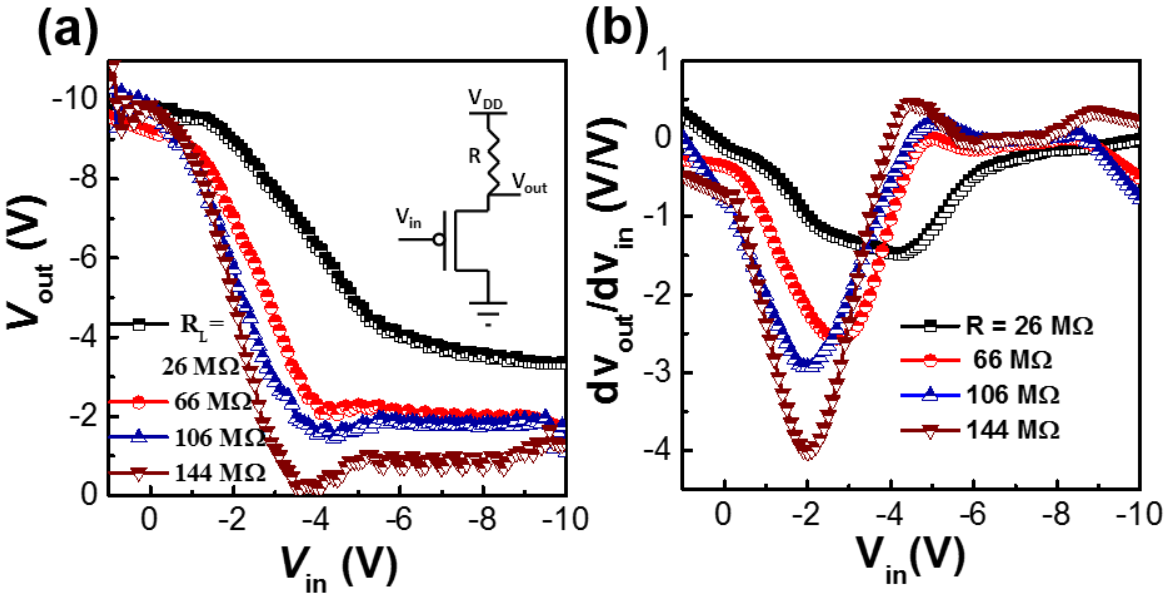

Figure 6.14 : (a) Voltage transfer characteristics of the resistive load inverter circuit with paper OFET. (b) Static gain with different resistive loads.

6.4 CONCLUSION

In this chapter, bottom gate top contact organic field-effect transistors with high performance and stability fabricated on PowerCoat™ HD 230 paper substrate have been demonstrated. The solution-processed paper-based devices with TIPS-pentacene: PS blend as active layer and HfO_2/PVP as hybrid gate dielectric exhibited maximum field-effect mobility of 0.44 $cm^2 V^{-1} s^{-1}$, near-zero threshold voltage and current on-off ratio approaching 10^5, while operating at a comparatively lower voltage of -10 V. These paper-based devices demonstrated highly stable behavior under gate bias stress, large number of repeated transfer measurement cycles and large duration exposure to high humidity, with negligible performance spread. In addition, a long ambient shelf life (more than 6 months) was observed. A slight improvement in the device performance was noticed when annealed at low temperatures, whereas high-temperature annealing deteriorated the device characteristics due to crack generation and propagation in the active layer. Furthermore, these devices were successfully demonstrated as viable phototransistors on the paper substrate. In addition, paper OFETs with HfO_2/PVA bilayer dielectric were also fabricated and have shown avg. and max. field-effect mobility of 0.52(±0.16) and 0.78 $cm^2 V^{-1} s^{-1}$ respectively. The fabricated Paper OFETs were also demonstrated in a resistive load inverter circuit with varying resistive load.

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