2
Device Fabrication and Analytical Techniques

The selection of appropriate processing methods, experimental and analytical techniques is very important in the fabrication of devices to obtain the desired results. The chosen experimental techniques decide the cost and performance of the devices. To make the devices cost-effective, the chosen experimental strategies must be cost-effective. Another important factor is the characterization techniques used for the material and devices during and after the fabrication of these devices. To draw appropriate conclusions and to understand the science behind the obtained device performance they must be carefully characterized. The first part of the chapter will give a brief overview of the fabrication of the studied devices, later various fabrication tools and the parameter extraction techniques used in the present work are discussed.

2.1 OVERVIEW OF DEVICE FABRICATION

For organic device fabrication, cleanliness is one the most vital factor that needs to be considered, also the environment in which the devices are being fabricated must have constant conditions as these devices are very much prone to changing environmental conditions like humidity, temperature, etc. In this thesis work, the devices are fabricated on rigid (silicon (Si)) and flexible (Polyethylene terephthalate (PET), Polyamide and Paper) substrates. All the materials were purchased from Sigma-Aldrich and used directly without further purification The fabrication of devices started with cleaning substrates. Silicon, PET, and Polyamide substrates were clean by a heated ultrasonic bath in 2-propanol (IPA), acetone, de-ionized water, and methanol for 10 minutes each in an ultra sonicator. Later followed by a heavy N_2 blow to dry the substrate. The digital image of the sonicator system used is shown in Figure 2.1. The temperature in the cleaning process was not exceeded above 60 °C to maintain the substrate integrity. For the unconventional paper substrate, the cleaning step was missed to avoid any damage to the substrate and they were only clean by heavy nitrogen blow to remove the dust particles from the surface. In all our studies, the devices were fabricated in the bottom gate and top contact architecture, where the bottom gate electrode is fabricated first and the top source and drain electrodes are fabricated in the last step. The Device schematic of the bottom gate top contact OFET is shown in Figure 2.2 (a).

After the appropriate cleaning of the substrate, the gate electrode was deposited using a thermal evaporation system under a high vacuum. In the case of the rigid silicon substrate, the highly doped n+ silicon was used as the gate electrode, whereas for the flexible substrate ITO coated PET, ITO was used as the gate electrode. For the polyamide and paper substrate, the gate electrode is deposited using a thermal evaporation system. This is followed by the deposition of the dielectric stack. The dielectric layer can be either of organic, inorganic or a combination of organic and inorganic layer. For the deposition of the organic dielectric layer, the spin coating technique was used, whereas the inorganic dielectric layers were deposited by Atomic Layer Deposition (ALD) and RF-magnetron sputtering system. For the rigid silicon substrate, 300 nm thermally grown SiO_2 was used as a dielectric layer. Over the dielectric layer, the next layer deposited is the active semiconductor layer. TIPS-pentacene was used as an active layer in all our studies, which was used either neat or in mixture with polymer binder polystyrene (PS). For the preparation of Neat/blend active layer solutions, TIPS-pentacene and polystyrene (PS) was

dissolved in toluene (with particular concentration depending on the need of the study) and stirred for 3 h at 70 °C to allow a perfect mix of semiconductor in the solvent.

Figure 2.1 : An ultrasonic cleaner from Rivotek.

The neat solution of TIPS-pentacene was used as it is. However, to make the blend solutions the TIPS-pentacene and PS solutions were mixed in the desired volume ratio. To make the active organic semiconductor layer, neat/blend solutions were dispensed above the dielectric layer. Just after drop cast, the substrates were covered with a glass petri dish to provide a solvent rich environment to the drying film. All solution preparations and sample processing steps were done in dark and ambient conditions. After the complete evaporation of the solvent, the active layer film is achieved. Further, the source/drain electrodes were patterned using a shadow mask in a thermal evaporation system under a high vacuum. The shadow mask used in the study is shown in Figure 2.2 (b). The mask is pasted on the substrate above the active layer, the metal is only allowed to pass throw openings in the mask and thus the desired patterns are obtained. For the measurements of capacitance separate capacitors were fabricated. The fabrication techniques and the device structure used were similar except the active layer is not considered in the fabrication process. The use of these capacitors is to know the capacitance density of the used dielectric stack.

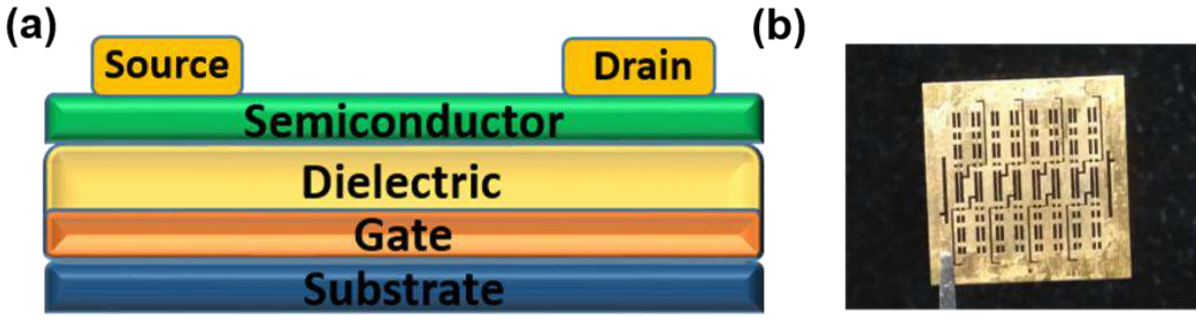

Figure 2.2 : (a) Bottom gate top contact OFET architecture. (b) Shadow mask for Source/Drain.

During and after the fabrication of these devices various characterization techniques were used. The Surface morphologies of crystals were captured by atomic force microscopy (AFM) using SPM XE-70 from Park Systems. X-Ray Diffraction (XRD) measurements were done using D8 advanced system from Bruker. Electrical measurements were performed using Keithley 4200 SCS analyzer in combination with the probe station. The various other fabrication tools and analytical schemes used are discussed in the next section.

2.2 Physical Vapor Deposition

In the OFET fabrication, the metal electrodes need to be deposited. The deposition of these electrodes must be controlled carefully to obtain smooth surface morphology. E-beam and thermal evaporation techniques are the physical vapor evaporation techniques and are generally used for metal electrode deposition. The two systems are used for almost similar work but have different working principles.

2.2.1 E-beam (Electron-beam) Evaporation

The electron beam (e-beam) evaporation system by its name suggest is a system that uses a high energy electron beam to be bombarded on the material that needs to be deposited. The high voltage (kV) electron beam when bombarded on the metal target which is placed in the high vacuum of the order of ~ 10^{-6}, the metal is heated up to its melting point. The electron beam causes the metal atom to transform into the gaseous phase. The gaseous phase atom travel in the vacuum chamber and get condensed on the substrate through the shadow mask to deposit the desired film pattern. The electron beam is generated by the thermionic emission of electrons produced from the incandescent filament. The deflection of this electron beam is done through a magnetic field. The metal on the target is only affected where the e-beam is bombarded, thus regional heating of material takes place and remaining material remains intact. The e-beam method can be used for metals that have a high melting point and it creates less contamination which are some of the advantages. In addition, the deposition rate which is a very crucial parameter in film deposition can be controlled to a large extent from as low as 1nm/minute to as high as few micrometers/minute. Also, the material utilization capability of the e-beam system is better than other physical vapor deposition system. However, the X-rays generated in the process may also damage the device thus can only be used before organic semiconductor deposition, i.e. for a bottom gate and top contact OFET it can be used for only depositing gate electrode. Figure 2.3 shows the schematic of the e-beam evaporation system.

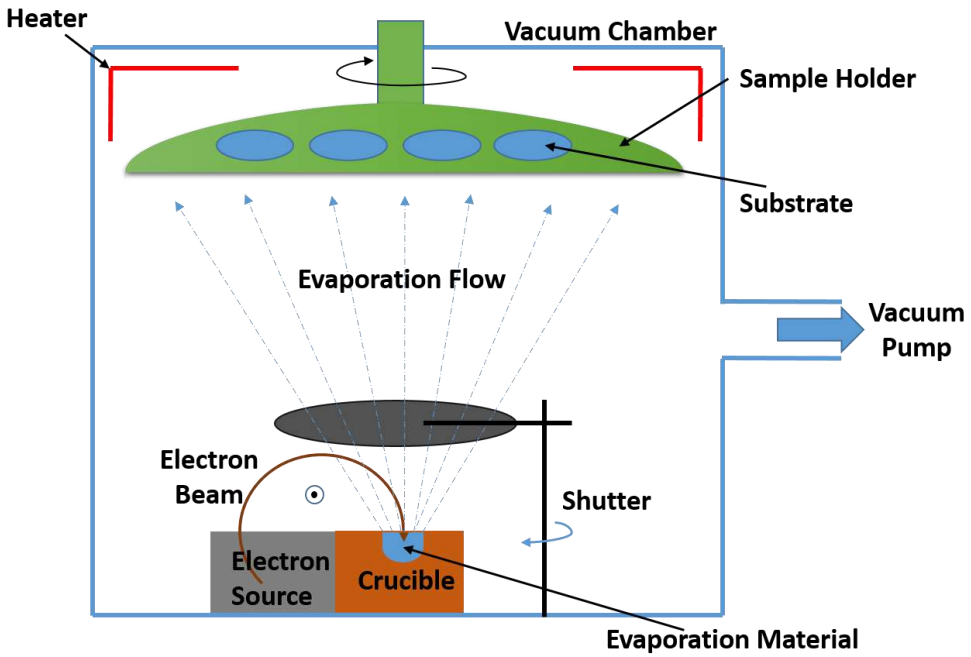

Figure 2.3 : Schematic representation of the e-beam evaporation system.

2.2.2 Thermal Evaporation

The thermal evaporation system is one of the simplest deposition techniques used for depositing metal electrodes. The thermal evaporation system involves resistive heating of the source material that when reaches its melting point converted to a gaseous phase, the gaseous

atom of the target material travel in a vacuum and condenses on the cool substrate to provide a thin film for the metal electrode. The source container is generally a tungsten boat, which is heated when a high current is passed through it. The deposition is done in a high vacuum condition, thus before using the system high level of vacuum (> 10^{-6} Torr) is achieved using vacuum pumps. The high vacuum thus increases the mean free path of the source material traveling from source to the substrate and thus the evaporated particle does not collide with other gas particles in the path. In addition, more the vacuum level in the system more will be the purity of deposited film. In the thermal evaporation system, less complex circuitry is involved compared to the e-beam system. The tungsten boat connected to a power supply is placed in the bottom and the samples on which the film is to be deposited are pasted on top of the chamber facing the source material. Figure 2.4 (a) shows the schematic illustration of the thermal evaporation process and the digital image of SC-Triaxis-e-beam and thermal evaporation system from Semicore is shown in Figure 2.4 (b). The system is used for depositing silver (Ag) gate electrode and gold (Au) source/drain electrode in our studies. In the system, the source to substrate distance was varied from 20-60 cm and a vacuum level below 10^{-6} Torr was used. The source material was heated in a tungsten boat at a power of 600 W and the deposition rate was controlled to 1 Å/s. The in situ thickness monitor was used to measure the thickness, also the thickness was later verified by stylus-based profilometer measurement. The general gate thickness in our studies was 100 nm and source/drain electrodes thickness was considered to be 200 nm.

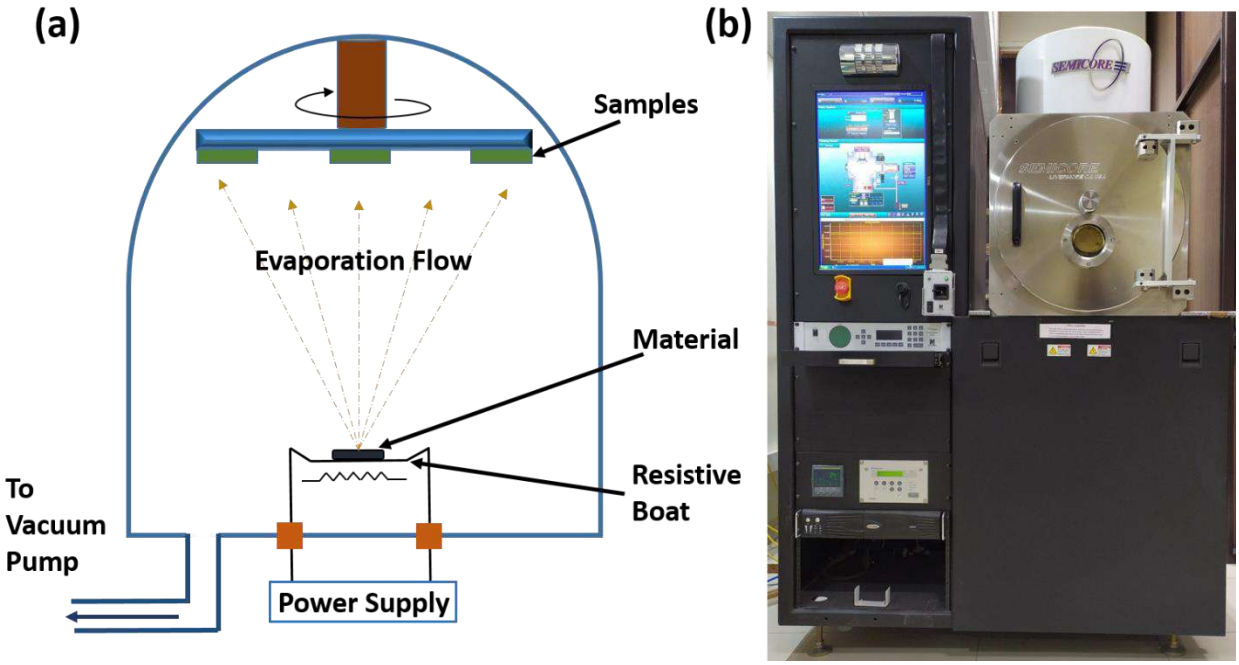

Figure 2.4 : (a) Schematic representation of the thermal evaporation system and (b) digital image of SC-Triaxis-e-beam and thermal evaporation system from Semicore used in experiments.

2.3 ATOMIC LAYER DEPOSITION

Atomic layer deposition (ALD) is a thin film deposition technology, which uses gas-phase chemical reaction step by step to form a thin film. This technology is a class of chemical vapor deposition techniques. The materials that can be deposited using ALD involve oxides, nitrides, metals, fluorides, sulfides, etc. In most of the atomic layer deposition system, two types of precursors also known as reactants are used and the reaction between the chosen materials allow a film to grow. The samples are placed in a closed chamber which is equipped with a heater to heat the samples during the process, depending on the need of the deposited film. The precursor's valves are open alternatively for a small amount of time to let the reactants reach the chamber and the reactants or the material to be deposited reach the reaction chamber with the help of inert carrier gas. When both the reactants reach the chamber, the vapor of the reactants takes some

time to react and form a layer of the film. After some time, the by-products left from the reaction and the residual reactants are pumps out from the chamber and the system is ready for the next cycle. With the continuous exposure of reactants to the chamber, a thin film of the desired material is obtained. The schematic representation of thin-film formation in the ALD system is represented in Figure 2.5 (a). As the film is deposited atom by atom thus a good quality thin film is achieved and the thickness of the film is precisely controlled. In our studies, the HfO_2 dielectric layer was deposited using a savannah S-200 thermal ALD system from Cambridge nanotech. The film was deposited at 100 °C with tetrakis-dimethyl-amidohafnium (TDMAH) and water as the precursors. The thickness of 40 nm was achieved by operating the ALD system for 400 cycles. Figure 2.5 (b) shows the ALD system used in the study.

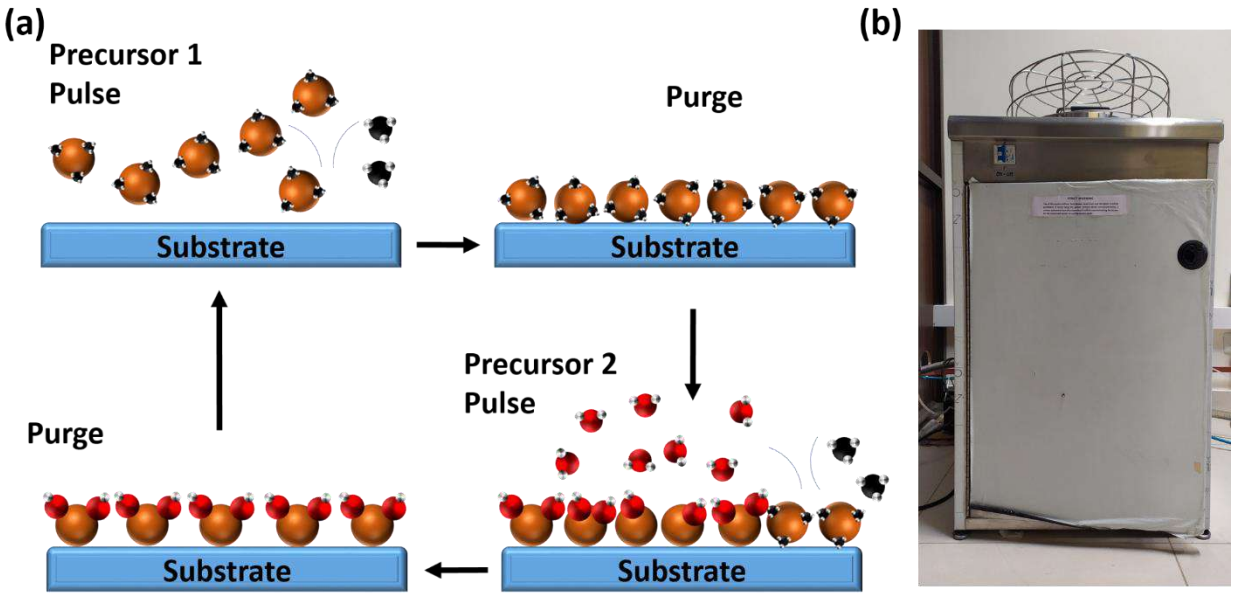

Figure 2.5 : (a) Schematic representation of film formation with ALD system, and (b) digital image of savannah S-200 thermal ALD system from Cambridge nanotech used in the experiments.

2.4 SPUTTERING

Sputtering is a Physical Vapor Deposition (PVD) technique that is used to deposit metals and dielectric materials. The basic working principle is when high energy ions are bombarded to the target material or the source material, the material atoms get ejected from its surface and travel towards the substrate on which the film is to be deposited and impact on the substrate with sufficient energy to provide a thin film. The ejected atoms from the target have a very wide range of energy. The ejected target atoms can freely move towards the substrate in a straight line and there is a possibility of re-sputtering from the substrate itself. However, if the gas pressure is high than the ejected atoms will have a collision with the background gas atoms and it reaches the substrate with moderate speed. Thus the deposition is widely controlled with the background gas pressure. The background gas which plays a vital role in the deposition of the film is generally an inert gas like argon. The gas is selected in such a way that the atomic weight of the target material should be close to the atomic weight of the gas used which ensures efficient momentum transfer. The sputtering techniques are classified as DC sputtering and RF sputtering. The major difference in both is the kind of power supply used. As suggested by their names the DC sputtering uses DC power whereas in the RF sputtering AC power is used. In DC sputtering when the working gas is ionized, which will result in positive ions and the generated positive ions will move towards the negative cathode and if the conductivity of the target material is not good those ions will get accumulated at the target material. Thus the DC sputtering is not preferred for dielectric material depositions. To eliminate the problem, RF sputtering is used where the alternating potential helps to remove the charge build-up at the target material and thus cleans the target. RF sputtering can be used to deposit metals and dielectric materials both

efficiently. A schematic representation of the sputtering technique is shown in Figure 2.6 (a). In one of our studies, barium strontium titanate (BST) is used as a high–k dielectric material and was deposited using RF sputtering. For deposition of BST film, samples were loaded into the vacuum chamber and the base pressure as high as 4×10^{-7} was achieved. BST films were deposited where the RF power was kept to 100 W, the substrate to target distance was fix to 5 cm, the working pressure and Ar flow rate was 2×10^{-2} mbar and 65 SSCM respectively. The thickness of the BST films was controlled by the growth time with the deposition rate of 0.1µm/hr. The digital image of the RF sputtering system used in the study is shown in Figure 2.6 (b).

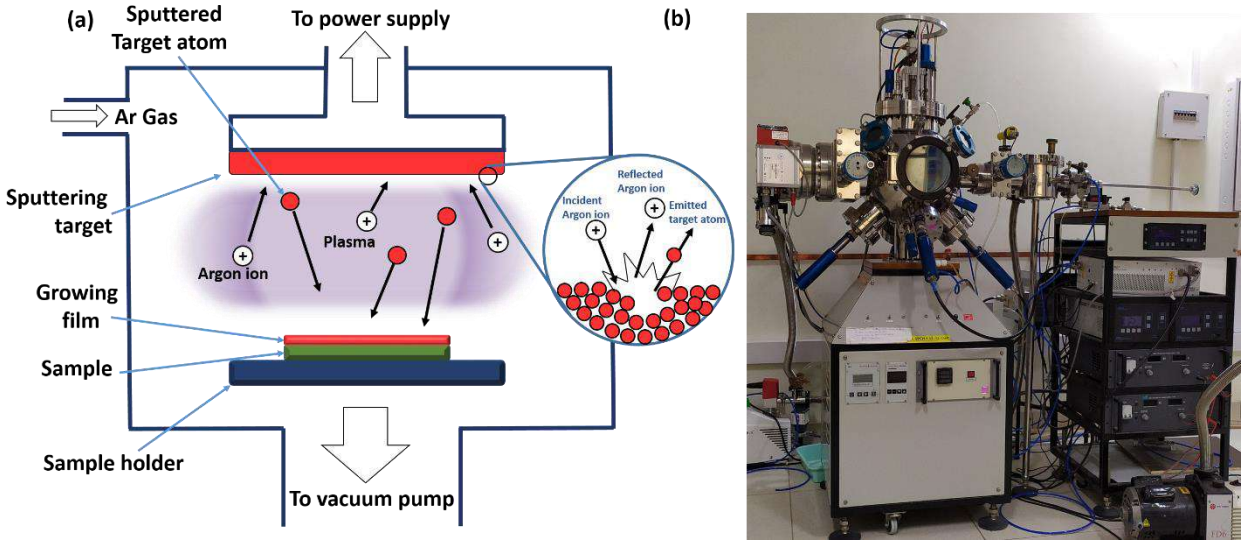

Figure 2.6 : (a) Schematic representation of the sputtering system and (b) digital image of the sputtering system used in experiments.

2.5 SPIN COATING

Spin coating is one of the simplest and widely used thin film deposition techniques. It is used to deposit various dielectric and semiconducting films and provide thickness ranging from few nanometres to few micrometers uniformly over the substrate. This method involves dispensing an adequate amount of solution of a material (made by dissolving a particular material to be deposited in a specific solvent), whose film is to be deposited on the substrate. The substrate is then given rotation to spread the solution to the entire substrate due to centrifugal force and provide a thin film with solvent evaporation. The machine that is used for spin coating is termed as Spin coater. Figure 2.7 (a) shows the schematic of the spin coating procedure. Spin coating is generally preferred for providing uniform films all over the substrate. The quality and thickness of the deposited film depend on various factors like the concentration of the solution, boiling point, viscosity of the solvent and materials solubility in the solvent. Other factors that affect the film thickness are the rotating speed and the time of rotation. If the spinning speed is very high, the film thickness will be low due to fast solvent evaporation and higher centrifugal force to the solution and vice versa. Also, the higher the concentration of the solute, the thicker will be the obtained film.

In our study Spin coating was used to deposit the planarizing layer over the paper substrate. In addition, the technique is used to deposit polymer dielectric layers. WS-650 MHz-BNPP/LITE spin coating system from Laurell was used in the study. Figure 2.7 (b) shows the digital image of the spin coater used. The rotation speed was varied from 1000-2000 rpm and the rotation time was varied from 30-60 s. The deposited films were annealed post-deposition to remove the residual solvent.

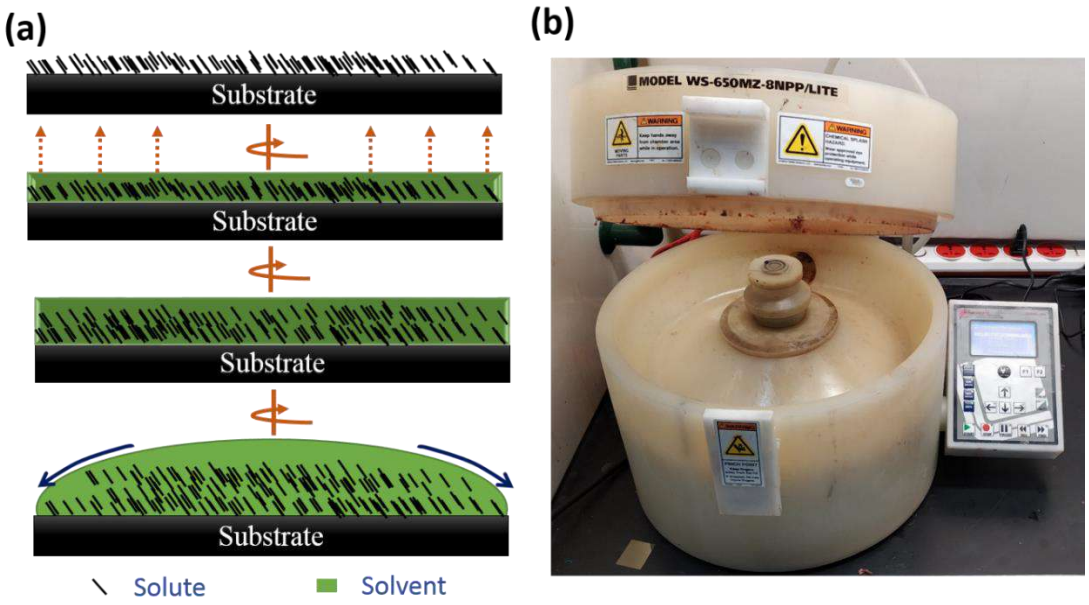

Figure 2.7 : (a) Schematic representation of film formation with the spin coating method and (b) digital image of WS-650 MHz-BNPP/LITE spin coating system from Laurell.

2.6 DROP CASTING

Drop casting is another simple film deposition technique in which the solution is simply poured over the substrate. The solution gets spread over the substrate and solvent evaporation will result in the desired film deposition. Simple to use and no instrument involvement are the key advantages of the techniques. But less control over the thickness and non-uniformity in the deposited films are some of the demerits. A schematic illustration of the drop-casting procedure is shown in Figure 2.8 (a).

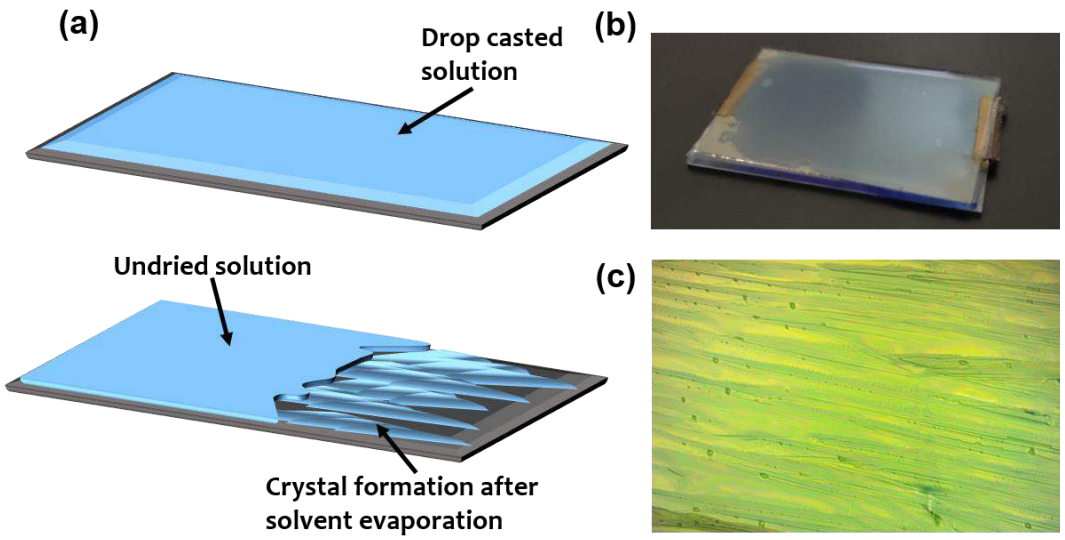

Figure 2.8 : (a) Schematic representation of semiconductor deposition through drop-casting method, and the digital image of the (b) semiconductor solution drop cast over a flexible sample, (c) semiconductor crystals formed after solvent evaporation.

Despite the demerits, the method is used in films where slow solvent evaporation is required. The decelerated solvent evaporation will lead to higher crystalline films because of the higher molecular arrangement times. The thickness of the film in the drop-casting procedure depends on various factors like the boiling point of the solvent used, the concentration of the solute in the solution, etc. The thickness, quality and orientation of the film can also be controlled by providing external temperature to the substrate by increasing the evaporation rate. In our

studies, drop-casting is adopted to deposit semiconductor films. The semiconductor solution was dispensed over the substrate and immediately after that, the substrate was cover with a glass petri dish to give solvent rich environment to the drying film. The slow solvent evaporation resulted in highly crystalline semiconducting films. The digital image of the solution dispensed on the flexible substrate and the microscopic image of the obtained semiconductor crystals are shown in Figure 2.8 (b).

2.7 PHOTO LITHOGRAPHY

Photo Lithography which is also termed as optical lithography is a technique used to pattern thin films in device fabrication. The optical lithography process uses UV light, which is allowed to fall on the photosensitive polymer also known as photoresist, through the photomask. The photomask consists of patterns that are desired in the film. Light is allowed to pass through the transparent regions and will be stopped by the opaque regions. With the interaction of light to the photoresist, it either softens or hardens depending on the type of photoresist. The photoresists are classified into two types, positive and negative photoresists. Those photoresists which become insoluble in developer after exposure to light are termed as positive photoresist and those which become soluble in the developer are termed as negative photoresist. After exposure to light, the photoresist is then developed to get desired patterns and the films beneath the photoresist can thus be selectively etched. The process has very high precision and can be used to draw patterns with the spacing of few nanometres. The schematic illustration of the lithography process is shown in Figure 2.9 (a) and the digital image of the photolithography setup is shown in Figure 2.9 (b).

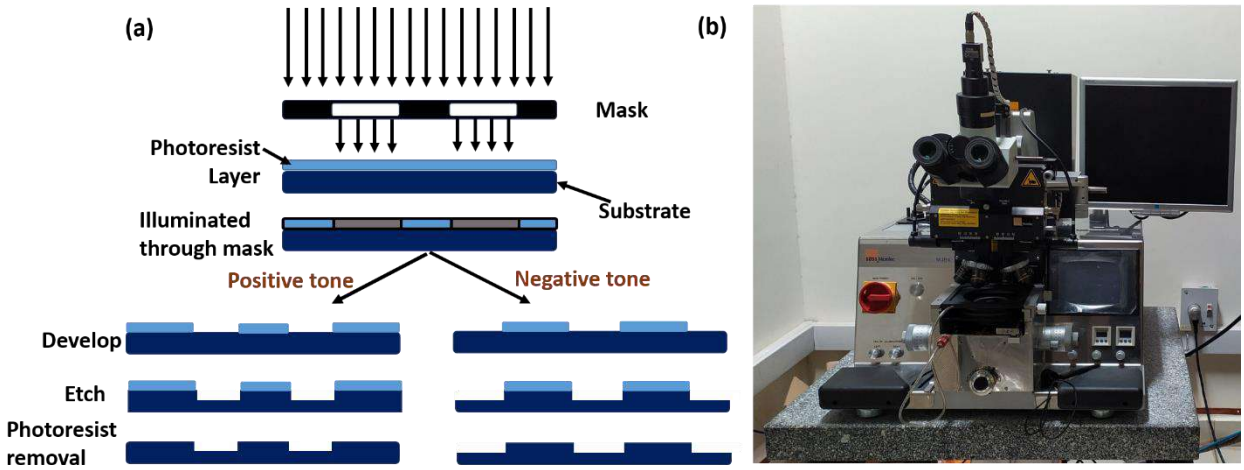

Figure 2.9 : (a) Schematic illustration of the photo-lithography process and (b) digital image of the photolithography machine.

2.8 SURFACE PROFILING

Surface profiling is necessary to obtain the thickness of various deposited films in device fabrication. Linear surface profiling of a thin film can be done using a simple profilometer and is one of the easiest techniques to record the surface profile. The surface profilometer consist of a sharp tip also termed as a stylus. The stylus continuously exerts a constant force to the surface under examination. And this constant force is monitored by a feedback system through a computer. The stylus is attached to the profiler which can move in an upward and downward direction. To examine the film thickness, the stylus is scanned from one point to another and when the stylus moves in hills and valleys of the film the exerted force on the stylus is replicated to the profiler and the constant force applied changes due to its movement and that deviation is recorded by the closed feedback loop. The schematic representation of the profiling technique is shown in Figure 2.10 (a). The surface profiling technique using the stylus is also termed as contact

type surface profiling. However, when surface profiling is done using light where there is no direct contact with the measuring film it is termed as non-contact surface profiling. The contact type profilometry has a major disadvantage of more chances for the tip to damage with the rough films as the tip is in direct contact with the film. Also, the scan speed will be limited due to direct contact. Contrary to that non-contact surface profiling is fast and has less damage possibility. Contact type profilometry system DekTak-XT surface profiler from Bruker was used for various thickness measurements in our studies. The digital image of the profile-meter is shown in Figure 2.10 (b). The radius of the stylus used was 2 μm and the scan time was 30 s to 60 s.

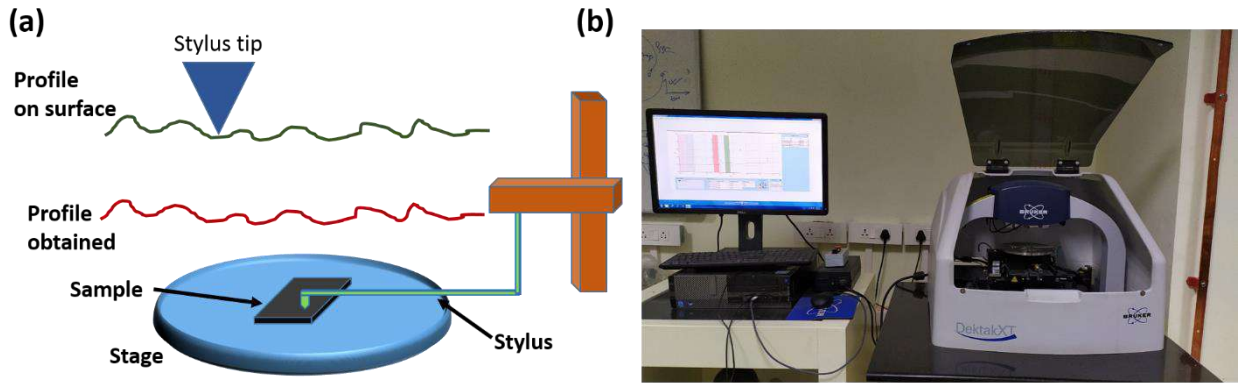

Figure 2.10 : (a) Schematic illustration of stylus profilometer and **(b)** digital image of DekTak-XT surface profiler system from Bruker that was used in experiments.

2.9 X-RAY DIFFRACTION

X-ray diffraction techniques are the most fundamental analytical techniques and have been used for long to understand the crystal structure, recognizing unknown materials, dimensions of the unit cell, knowing the preferred orientation in a polycrystalline material, orientation in the crystalline material and calculating the stress and defects in the material. The X-ray diffractometer basically consists of three parts namely X-ray source, sample holder and a detector. The generation of X-rays is performed in a cathode ray tube by heating a filament with the application of high voltage. The filament emits electrons, which are accelerated by applying high voltage, the accelerated electrons move towards the sample and bombarded to it with high energy. When the bombarded electrons have sufficient energy to knock out electrons from the inner shell the characteristics X-rays are emitted. The emitted spectra consist of many components among which the most common are k_{α} and k_{β} radiation. k_{α} corresponds to transition from n = 2 to n = 1 and k_{β} corresponds to n = 3 to n = 1 transition. The characteristics X-rays are specific to the target material (Cu, Fe, Mo, and Cr). Monochromatic X-rays are generated by filtering the emitted X-rays through filter foils or crystal monochromators. Cu is the most common target material used in the X-ray diffractometer with Cuk_{α} radiation of 1.5418 Å. The monochromatic X-rays are collimated and directed towards the sample under consideration. When the incident X-ray on the material satisfies the Bragg's Equation $(n\lambda = 2dsin\theta)$ constructive interference results and there observed a peak in the collected intensity. The rotating detector records the intensity of the reflected X-rays. The collected intensity is processed by the detector and converted to count rate which is then produced as output by the system. X-ray analysis generally required thick films for analysis. Non-destructive nature and no need for complicated sample preparation are some of the merits of these methods. The basic illustration of an X-ray diffractometer is shown through a schematic in Figure 2.11 (a). In our studies, X-ray diffraction measurements were performed using D8 advanced from Bruker, which uses Copper as the target material with CuK_{α} radiation = 1.5418Å. The digital image of the used diffractometer is shown in Figure 2.11 (b).

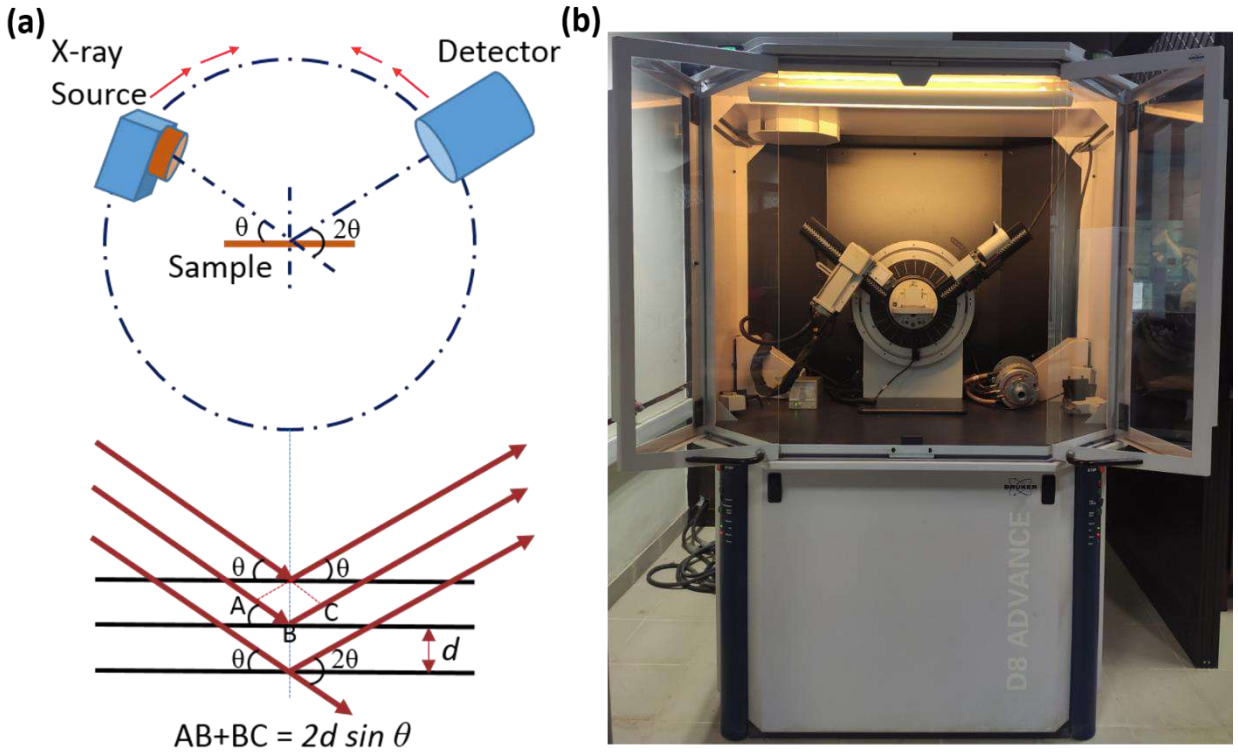

Figure 2.11 : (a) Illustration of the working principle of X-ray diffraction measurement. (b) D8 advanced X-ray diffraction system from Bruker that is used in experiments.

2.10 ATOMIC FORCE MICROSCOPY

In OFET fabrication various interfaces such as dielectric: semiconductor or the semiconductor: electrode interface plays a vital role in defining the device performance. To get high performing devices analyzing the surface morphologies are very important. Atomic force microscopy is certainly among the most advance microscopic techniques that are used to analyze the surface morphologies with its resolution in nanoscale. Atomic force microscopy analysis not only provides the three-dimensional morphology of the film under consideration but also provide various surface related parameters. The basic principle of AFM is the deflection of cantilever on the surface of the sample, which reflects the incident laser beam which is irradiated over the cantilever and the deflection in the reflected laser is then collected and patterned by the photodetector. The cantilever consists of a sharp tip at the front end, which is used to scan the sample under consideration. When the tip slowly moves downwards it is attracted to the sample, when it reaches considerable closer the repulsive forces start dominating and the tip is deflected away from the sample. A laser beam is continuously shining over the tip-top and after reflection, it is getting collected by a photodetector. When the tip moves to and fro in the selective area under consideration, the tips move in the hills and valleys and thus there is upward and downward motion in the cantilever. The reflected laser beam is deflected and its motion is tracked by a position-sensitive photodetector. A reference point is set, which is a constant separation between the sample and the tip and is continuously monitored and kept constant through a closed feedback loop. The deflection in cantilever is monitored, processed and is presented in the form of a 3D image of the surface which represent the surface morphology and present various surface parameters. A schematic illustration of the AFM technique is shown in Figure 2.12 (a). In the present study SPM XE-70 from Park Systems was used for Atomic force microscopy analyses of various dielectric and semiconductor films. The digital image of the system used is shown in Figure 2.12 (b).

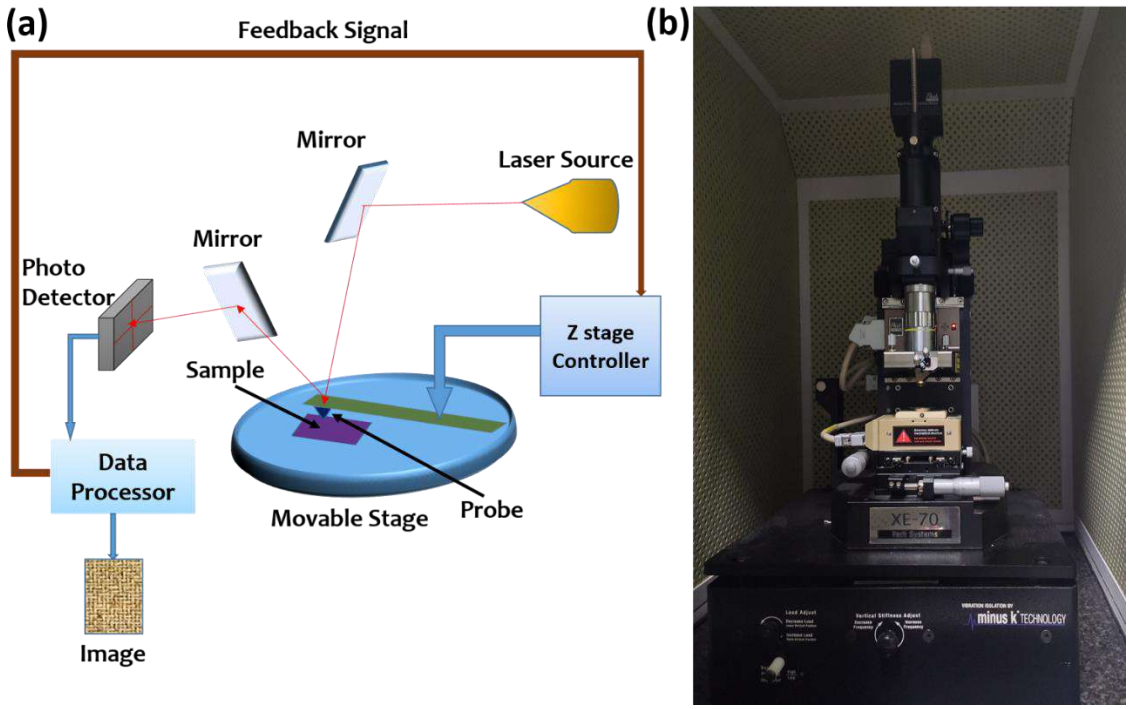

Figure 2.12 : (a) Surface roughness analysis through the atomic force microscopy system. (b) SPM XE-70 AFM system from Park Systems.

2.11 OPTICAL MICROSCOPE

The optical microscope also termed as light microscope are the most commonly used microscopes. They use visible light and a combination of lenses to produce a magnified image of the small object. An optical microscope can either be simple (uses only one lens) or a compound microscope (uses more than one lens). Most of the optical mirrors are compound in nature that enlarges image in two-stage. Light from the mirror is allowed to shine on the object under consideration, a lens (objective lens) near the object is used to collect light and focus the real image of the object inside the microscope. The captured image is then magnified by a series of second stage curved lenses (eyepiece lens) to produce the enlarged image to the viewer.

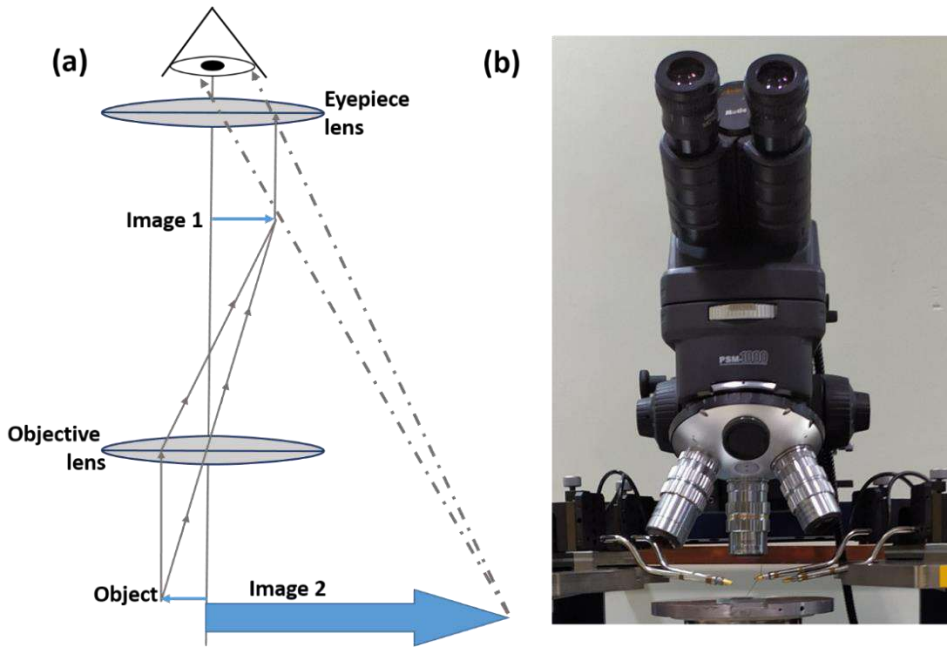

Figure 2.13 : (a) Image capturing using an optical microscope. (b) The optical microscope used in the experiments.

The enlarged image can be seen by looking into the eyepiece and images can be captured by using photosensitive cameras to produce a micrograph. The schematic representation of the optical microscope is shown in Figure 2.13 (a). In the current study, optical microscopy was used to capture the top view of the semiconducting crystal. The digital image of the microscope used in the study is shown in Figure 2.13 (b).

2.12 SCANNING ELECTRON MICROSCOPY

The human eye can detect two points that are separated by 0.2 mm if sufficient light shines on them without using additional lenses. This separation is termed as the resolving power or resolution of the human eye. The resolution of a commonly used optical microscope depends on the quality and quantity of lenses use and also on the wavelength of the light source. The optical microscope has a resolving power of around 1000x. The average wavelength of the white light is about 550 nm, which limits the resolution of the optical microscope to about 200-250 nm. To overcome the limitation and imaging even smaller features, electron microscopy is used because an electron has a much shorter wavelength which enables better resolution. Scanning electron microscopy uses a focussed beam of electron scanned above the surface which produces various signals that are used to produce surface morphology of micro and nano-scale samples.

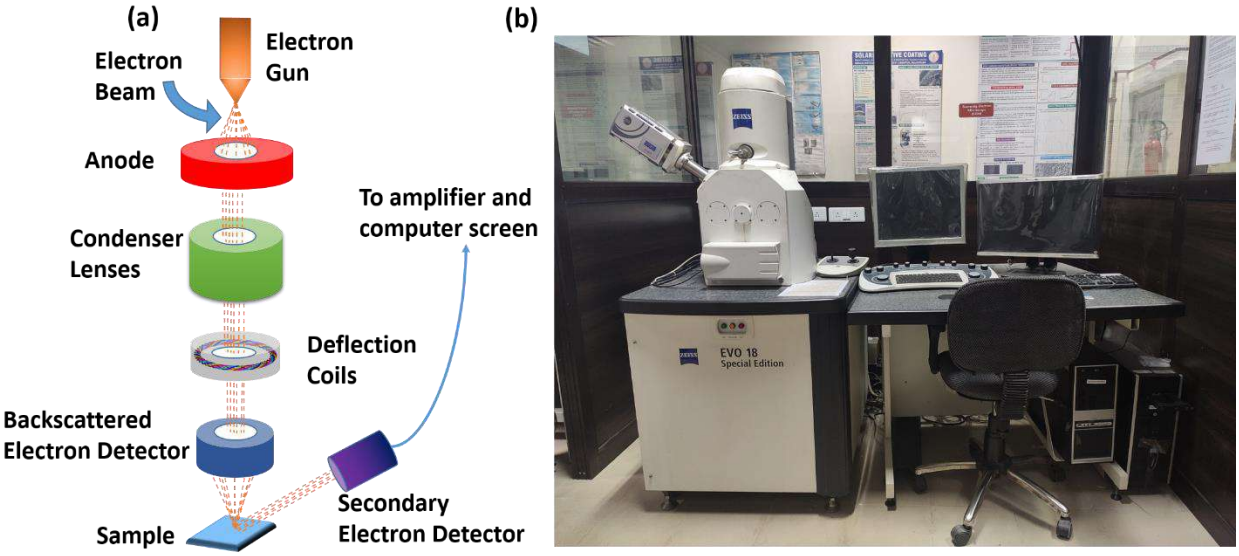

Figure 2.14 : (a) Surface imaging using scanning electron microscopy. (b) SEM EVO-18 special edition system from Carl-Zeiss.

The major constituents of SEM are the electron beam source, series of electromagnetic lenses to direct the beam to the surface of the sample, an electron collector, a sample holder and a work station to process the obtained signal and produce images. The samples are mounted inside the chamber and with a combination of pumps, the chamber is evacuated. Electrons are emitted by an electron source at the top of the vertical column and are accelerated towards the samples by passing through a series of electromagnetic lenses. The electron beam performs a raster scan at a specified area for imaging. The position of the electron beam is controlled by scan coils situated above the objective lens. When the high energy electron beam interacts with the surface it penetrated to few microns in the sample depending on the applied voltage and density of the sample and it produces secondary electrons, backscattered electrons, diffracted backscattered electron, heat and characteristics X-rays. Secondary electrons play a key role in SEM imaging. The position and intensity of these emitted secondary electrons are collected by one or more detectors and the information is processed to provide the surface morphology. Backscattered electrons and characteristics X-rays can further be used to obtain contrast and crystal properties. The schematic illustration of SEM is shown in Figure 2.14 (a). In the current

study cross-sectional imaging of semiconductors, crystals are captured by SEM using EVO-18 special edition from Carl-Zeiss. The digital image of the instrument is shown in Figure 2.14 (b).

2.13 ULTRA-VIOLET AND VISIBLE SPECTROSCOPY

Ultra-violet and visible Spectroscopy refers to either absorption or reflectance spectroscopy in part of UV and full visible spectral range. It is a widely used analysis technique in analytical chemistry. It uses visible and adjacent ranges and the interaction between the light and the matter in this particular range is studied. Upon interaction with the light, the atom and molecules undergo electronic transition. In the UV and visible absorption spectroscopy transition from the ground state to excited state is measured. The said spectroscopy is based on Beer-Lambert's law, which states that the absorbance depends on the intensity of incident radiation, the thickness of the absorbing solution and concentration of the solution. The general spectroscopy setup uses a light source that emits radiation in the UV and visible region of the electromagnetic spectrum. With numerous rotating prism, the emitted light is dispersed in the form of increasing monochromatic wavelengths. Each of these wavelengths is separated through slits and are further separated by a prism into two beams. The two beams are allowed to pass through the reference and the actual sample solution, which are placed in quartz cuvettes. The light coming out from the two cuvettes of the reference and the actual sample is monitored through photocells, the light induces an alternating current in the photocell. The alternating current is then analyzed and pass through an amplifier to produce results in the form of the absorbance spectrum. A schematic illustration of the technique is shown in Figure 2.15 (a). In the current study, the technique was used to analyze the absorption spectrum of semiconductor material and UV-visible spectroscopy was performed in a wavelength range of 250-800 nm using UV1800 spectrophotometer from Shimadzu. The digital image of the same is shown in Figure 2.15 (b).

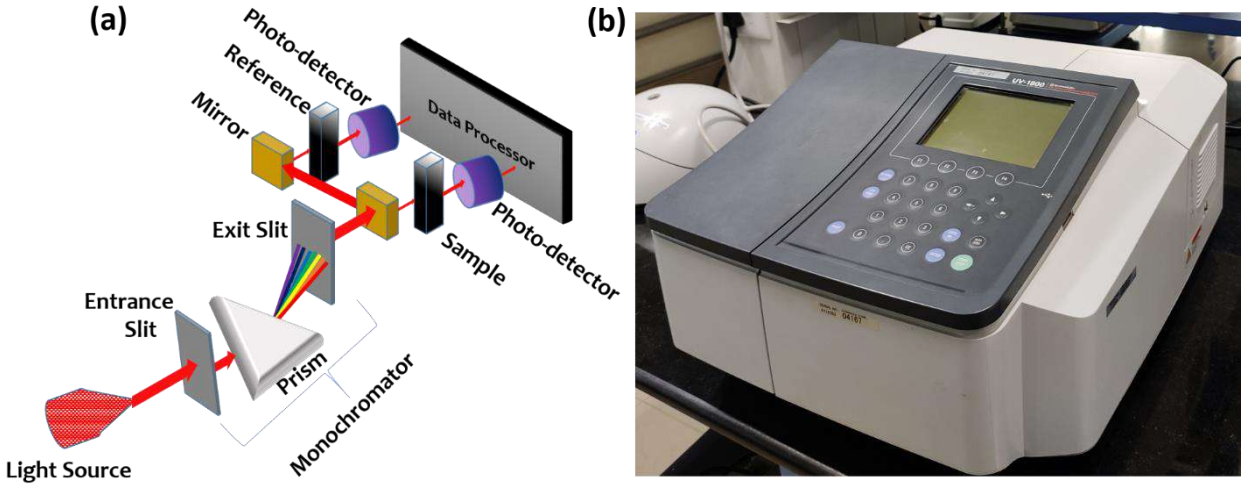

Figure 2.15 : (a) Schematic illustration of UV-visible spectroscopy process. (b) UV-1800 UV-visible spectrophotometer from Shimadzu used for characterization.

2.14 ELECTRICAL CHARACTERIZATION

Precise electrical characterization of the fabricated devices is important in analyzing device characteristics. The fabricated devices were analyzed using a 4200-semiconductor characterization system form Keithley. The system is a fully integrated parameter analyzer that is capable to deliver synchronizing current-voltage (I-V) and capacitance-voltage (C-V) measurements. Keithley interactive test environment (KITE) was used to feed the characterization parameter and analyze the fabricated device. The 4200 SCS analyzer was used in combination with the Cascade Microtech PM5 probe station where the devices were positioned and probed.

The probed devices were connected to the measuring unit with the help of the coaxial cables. All the measurements were done in the dark and ambient conditions in a normal lab environment. Relatively constant environmental conditions were maintained near the characterizing unit to avoid any effect from the external stimuli. The digital images of the parameter analyser and probe station are shown in Figure 2.16 (a) and (b) respectively.

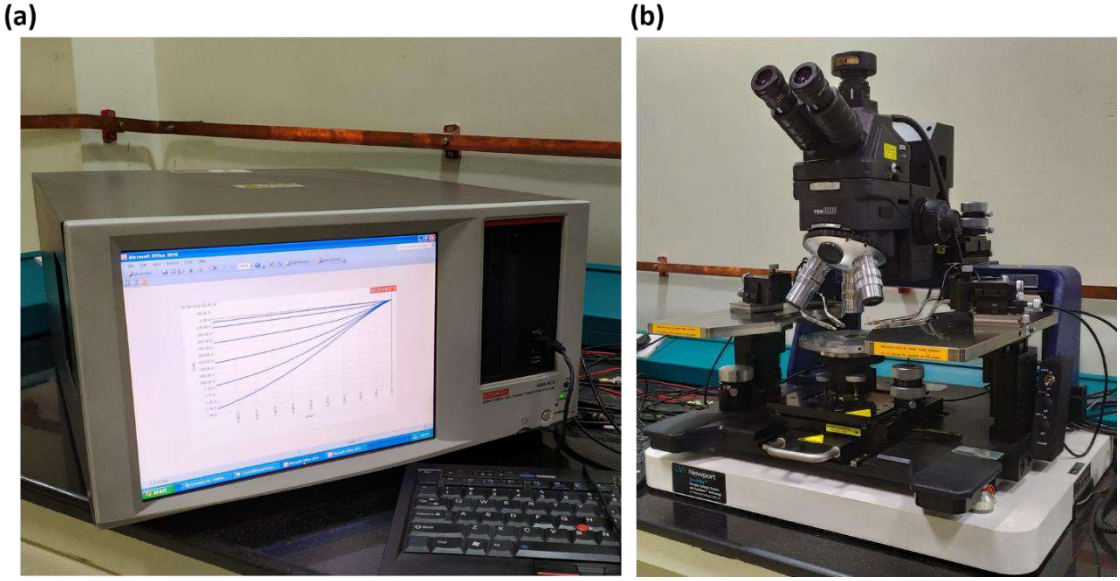

Figure 2.16 : (a) 4200-semiconductor characterization system from Keithley. (b) Cascade Microtech PM5 probe station used for characterization.

2.14.1 Parameter Extraction

The performance of any device is analyzed through its characteristic electrical parameters. Each device has its critical characteristic parameters that define its superiority and they depend on various factors such as the material and processing techniques. Depending on a particular parameter and its importance through the device perspective, we can conclude whether the device is performing good or bad. The performance of OFETs is also evaluated by these critical parameters. Some of these parameters are field-effect mobility (μ), the threshold voltage (V_{TH}), current on-off ratio (I_{ON}/I_{OFF}), sub-threshold slope (SS), and interface trap density (D_{it}). These critical parameters depend on various factors such as type of semiconductor, the material used for dielectrics, nature of the electrodes, processing techniques used for deposition of dielectric, semiconductor and electrodes. In the organic devices, environmental conditions also play an important role in defining device parameters as these devices are very much prone to the environment. All the discussed factors strongly affect the device parameters.

The mentioned device parameters are extracted from the electrical characteristics of the fabricated device. To obtain these parameters, first, the variation in drain current (I_{DS}) with applied gate voltage (V_{GS}) and drain voltage (I_{DS}) is recorded. The variation of drain current with varying gate voltage (I_{DS} vs. V_{GS}) with the drain to source voltage held constant is called as the transfer characteristics of the OFET and the variation in drain current with the varying drain to source voltage (I_{DS} vs. V_{DS}) is called as the output characteristics of OFETs. The transfer and output characteristics of a p-type OFET are shown in Figure 2.17 (a) and (b) respectively.

OFETs operate in accumulation region, thus when a gate bias is applied charges of opposite polarity get accumulated at the dielectric semiconductor interface and a channel is formed between the source and the drain electrode and current conducts. This can be observed in the reference transfer characteristics in Figure 2.17 when a small positive gate bias is applied in a p-channel OFET, there are only a few holes available at the semiconductor dielectric interface and a small amount of leakage current exists (the device is said to be in OFF state). When the gate

voltage starts increasing towards negative values, charges (holes) start getting accumulating at the interface and the drain current started increasing slowly. The applied gate voltage reaches a point where a substantial amount of charges accumulated at the interface and current increases sharply due to the conduction path between source and drain through the channel (the device is said to be in ON state). When the drain to source voltage is low the device is said to be operated in the linear regime and at the high drain to source voltage, it operates in a saturation regime. The two regions are separated by the dotted line in the output characteristics. Drain current equations in linear and saturation regimes are given similar to the equation for standard MOSFETs. Drain current equation in linear regime is given by the following Eq.,

$$I_{DS} = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (2.1)$$

And the equation in the saturation regime is given by,

$$I_{DS} = \mu C_{ox} \frac{W}{L}\frac{(V_{GS} - V_{TH})^2}{2} \qquad (2.2)$$

Where μ is the field-effect mobility, C_{ox} is the capacitance density, V_{TH} is the threshold voltage of the device and W and L are channel width and length respectively.

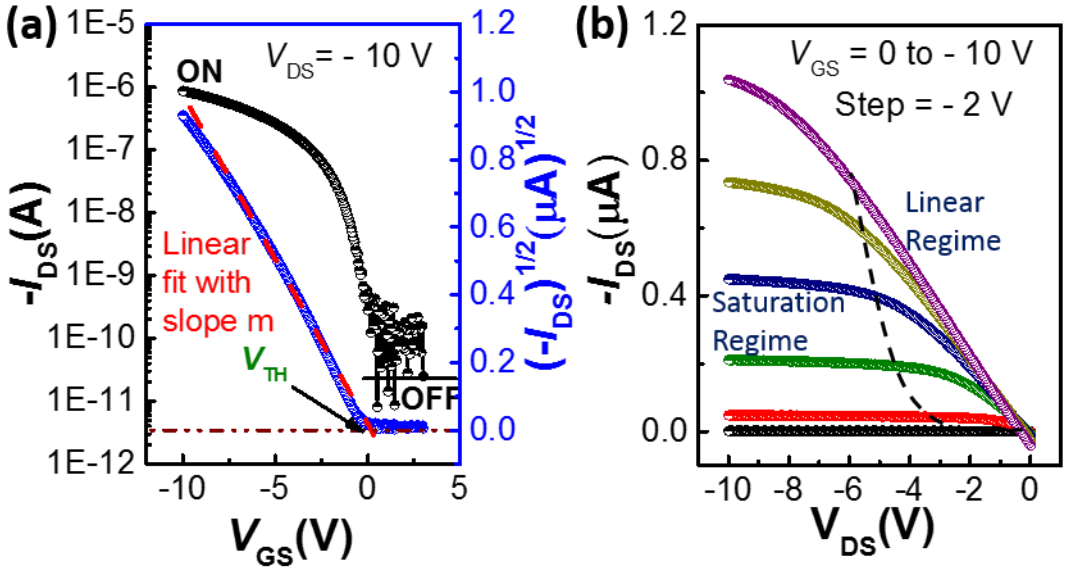

Figure 2.17 : Typical (a) transfer and (b) output characteristics of a p-type OFET.

Most of the device parameters can be extracted from the transfer characteristic. The most important parameter in OFETs is the field-effect mobility of the device. The field-effect mobility defines how easily charge carriers can move in semiconductor and it can be extracted from the transfer characteristics by plotting the square root of drain current vs. gate voltage. The slope of the square root of drain current vs. gate characteristics can be obtained by applying a linear fit to the obtained curve and the slope is defined mathematically as,

$$m = \frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}} \qquad (2.3)$$

By substituting the value of slope in the derivative of Eq. (2.2) it can be rewritten as,

$$\mu = \frac{2L}{WC_{ox}}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 = \frac{2L}{WC_{ox}}m^2 \qquad (2.4)$$

The obtained equation gives the mobility of the device and is the most standard way for finding the said parameter and in the current study, the mobility's were extracted through this method. The mobility calculation from this method has two limitations, first it does not account for the contact resistance and second it is highly geometry dependent, and specially more prominent errors can be seen for short channel devices. The equation may lead to over or underestimation of mobility values. Contact resistance effects are more dominant on short-channel OFETs. Since, most of our devices have the long channel lengths (> 100 μm), thus we assume the mobility values may not be much deviated from the values calculated from other more accurate mobility calculation methods like gated four-point probe or transmission line method. Furthermore, in this thesis the average and standard deviation of the characteristics parameters have been calculated to show the operational stability by selecting multiple devices from different location of the sample, which certainly compensate obvious effects arising due to inherent over/under-estimation of mobility values. Moreover, the idea of the research was not to focus on the high values of characteristics parameters, rather we wanted to demonstrate the possibility of fabricating high performance devices on unconventional substrate. Thus the commonly used parameter extraction technique has been used. The next important parameter in OFETs is the threshold voltage (V_{TH}), which is defined as the minimum value of the gate voltage at which conduction starts to take place in the device. V_{th} can also be obtained from the square root of the drain current vs. gate voltage curve. The intercept and slope of the linear fit in this curve are first obtained and the V_{TH} of the device can thus be obtained as the negative ratio of intercept and the slope of the linear fit. On to off current ratio is defined as the ratio of device current ON state to OFF state respectively. In the current study, at a particular operating voltage, the maximum drain current value achieved is considered as ON current and where the device current is constant at a low gate voltage that constant level is considered as OFF current. If the drain current is not constant in the off region than the minimum current level in that region is considered as off current. Subthreshold slope (SS) is related to the switching speed of the transistor and is defined as the minimum change in gate voltage required to obtained per decade change in drain current. Transfer characteristics with steeper slope represent faster devices with the fast transition from OFF to ON state. Another important OFET parameter that is related to the quality of semiconductor: the dielectric interface is the interfacial trap density (D_{it}). D_{it} can directly be obtained from the SS values by using the following equation,

$$D_{it} = \frac{C_i}{q}\left[SS\frac{\log(e)}{kT/q} - 1\right] \qquad (2.5)$$

2.14.2 Operational Stability Test

Operational stability is one of the major concerns in OFETs. During the operation, devices are subjected to various external stimuli including electrical, mechanical and thermal. To utilize these devices in circuit and sensing applications their operational stability is a must. Operational stability represents the invariant nature of device performance during operation. Operational stability of the device depends on various factors like the kind of semiconductor material used, processing techniques, device structure, etc., and can be tested by subjecting the devices to various electrical and mechanical stress. A device is said to be operationally stable if there is no significant change in its electrical parameters even when subject to various electrical or mechanical stress or with time. In the current study, the electromechanical stability of the fabricated devices is tested by a series of experiments.

2.14.2.1 Electrical Stability

To test the electrical stability, devices were first tested through multiple scan cycle scheme. In this test transfer characteristics (I_{DS} vs. V_{GS}) of the devices were captured multiple times continuously and the shift in electrical parameters like mobility, threshold voltage, ON current, etc. was observed. Another test for electrical stability is the bias stress stability test in which the device is subjected to a fix bias voltage at the gate and drain terminal. With the constant voltage applied to drain current (I_{DS}) should remain constant for an operationally stable device. However, due to trapping of charges at various regions in the device such as in the bulk of the semiconductor, at the grain boundaries, at various interfaces like dielectric: semiconductor or the electrode: semiconductor interface, the current show's deviation with time. In the current study. The bias stress study was carried out by applying a constant bias to the device for different time intervals followed by capturing the transfer characteristics after each bias stress time. Also, the variation in normalized drain current was analyzed with time with the applied stress. Mathematically, the decay in normalized drain current (ratio of I_{DS} at time t to I_{DS} at time 0 s.) is given by the following equation,

$$\frac{I_{DS}(t)}{I_{DS}(0)} = \exp\left(-2\left\{\frac{t}{\tau}\right\}^{\beta}\right) \qquad (2.6)$$

Where, β is a temperature-dependent dispersion parameter and reflects the width of involved trap distribution and τ is the relation time, a measure of typical charge trapping time.

The obtained experimental data is fitted in Eq. (2.6) and the value of τ and β were extracted. The corresponding shift in threshold voltage of the device can be obtained through the extracted τ and β values by using the following equation,

$$|\Delta V_{TH}(t)| = |V_{GS} - V_{TH0}|\left[1 - exp\left\{-\left(\frac{t}{\tau}\right)^{\beta}\right\}\right] \qquad (2.7)$$

Where ΔV_{TH} (t) is the shift in threshold voltage with time under bias stress, V_{TH0} is the threshold voltage before applying bias stress. With the obtained parameters the device electrical stability was observed.

2.14.2.2 Mechanical stability

To explore the feasibility of fabricated devices in flexible applications, mechanical stability needs to be explored. In this test, the devices were subjected to mechanical stress with varying the bending radius and the variation in device electrical performance was observed. The applied strain to the devices is measured by the following equation,

$$\text{Strain (\%)} = \frac{t_{sub}}{2R_{bend}} \times 100 \qquad (2.8)$$

Where t_{sub} is the thickness of the substrate and R_{bend} is the bending radius. In the current study, device transfer characteristics were captured with the increasing strain (decreasing bending radii) and the variation in mobility, threshold voltage and current ON-OFF ratio were extracted. In addition, the devices were subjected to bending cycles, where in each bending cycle the devices were given both the compressive and tensile strain to particular bending radii and the device characteristics were captured by taking it back to the unstrained situation. Device characteristics were captured by bending the devices for as large as 500 such cycles. Electrical characteristics like multiple transfer scans, bias stress stability test were performed before and after bending the devices to check the deterioration in device performance with mechanical stress. The bending angle corresponding to bending radii were calculated by (θ= arc/R_{bend}), where arc is the distance between source edge to drain edge. The angles correspond to 12mm, 10mm, 8mm and 5 mm bending radii are 5.73°, 6.89°, 8.60° and 13.76° respectively.

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