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Effect of Semiconductor: Polymer Blend

Performance and operational stability of OFETs can be improved by various factors like changing the active and dielectric layer deposition strategies, improving the quality of the deposited films to get a smooth dielectric: semiconductor interface. Dielectric: semiconductor interface is the most crucial interface in the OFET system as the charge carries get accumulated in the first few angstroms at the interface. Smoother the interface lesser will be the trap quantity and which in turn leads to better device performance. Various strategies are investigated to improve this interface such as incorporating an organic polymer insulating layer between the inorganic dielectric and semiconductor film. However, with the use of such buffer layer solution processing of semiconductor over it creates several challenges. Another important technique used is the use of semiconductors and insulating polymer together in the active layer. The self-governed vertical phase-separated dielectric: semiconductor interface results in an interface with lesser traps and thus leads to better performance of the device compared to devices with a neat semiconductor. In this chapter, the improvement in device performance with the use of semiconductor: polymer blend and the critical role of the mixing ratio of the semiconductor and polymer solutions on the electro-mechanical stability of the flexible blend OFETs are discussed [Raghuwanshi et al.,2018].

3.1 INTRODUCTION

The aftermath of extensive research interest and accompanying advancement in the device performance have made the solution-processed OFETs comparable to high mobility organic single-crystal field-effect transistors [Briseno et al.,2006, Hasegawa and Takeya,2009, Minemawari et al.,2011, Chen et al.,2012, He et al.,2015, Lim et al.,2017]. Along with achieving superior performance in devices, however, performance reliability is also a major concern in several standard applications of flexible electronics where a high degree of performance invariability is expected from devices under strained situations [Lin and Yan,2012, Ryu et al.,2015, Wu et al.,2015]. When the high performance and high degree of electro-mechanical stability are the prime objectives for a solution-processed flexible OFETs, blending organic semiconductor with an insulating polymer binder is certainly one of the best possible and conventional choice to achieve both aforementioned features together [Smith et al.,2010, James et al.,2011, Hwang et al.,2012]. Semiconductor: polymer blend OFETs derive their remarkable electrical performance due to the occurrence of vertical phase separation between semiconductor and polymer films [Smith et al.,2012, Bharti et al.,2016, Bharti and Tiwari,2016]. Numerous factors influence the electrical performance of blend OFETs which include deposition strategy, material properties of the polymer binder (molecular weight, crystallinity etc.), the solvent used, and mixing proportion of the semiconductor and the polymer solutions [Kang et al.,2008, Hwang et al.,2012, Diao et al.,2013, Shao et al.,2013, Pitsalidis et al.,2014]. The mixing ratio of semiconductor and polymer solutions is one of the crucial parameters, which has been given its due consideration while exploring its effects on the electrical performance of blend OFETs. Semiconductor: polymer mixing ratio, which has the potential to alter the device performance by several orders of magnitude by affecting overall film formation, also impacts the operational stability of devices. However, the relation between the mixing ratio and the electrical stability of semiconductor: polymer blend OFETs is scarcely explored [Madec et al.,2008].

In this chapter, the dependency between the mixing ratio of the semiconductor and polymer solutions and the electro-mechanical stability of the blend OFETs is systematically explored. Rigorously explored semiconductor material TIPS-pentacene has been used with insulating polymer polystyrene as the semiconductor-polymer pair. Polystyrene which is one among the few insulating polymeric binders reported, capable of forming phase-separated structures with small-molecule organic semiconductors was chosen to form a blend with the semiconductor. As per the literature available, polystyrene does not interrupt the π–π stacking of the TIPS-pentacene molecules and improves the uniformity in the molecular morphology and the active layer coverage within the device[James et al.,2011, Feng et al.,2016]. Polystyrene also has a good degree of solubility in common organic solvents. The electrical performance of OFETs was observed to improve with increasing polymer content in the solution. The maximum field-effect mobility improved from 0.08 for neat TIPS-pentacene OFETs to 0.24, 0.25 and 0.57 $cm^2 V^{-1} s^{-1}$ for semiconductor: polymer blend with mixing ratio of 3:1, 1:1 and 1:3 respectively. The 1:3 semiconductor: polymer blend OFETs exhibited much lesser drain current decay (~2 %) under the gate bias stress in comparison to 1:1, 3:1 blend and neat OFETs with drain current decay of 11.2 %, 17.8 %, and 41 %, which resulted in threshold voltage shifts of 0.05 V, 0.3 V, 0.48 V and 1.1 V respectively. All types of devices were recovered almost completely from the degrading effects of gate bias stress. OFETs with 1:3 semiconductor: polymer blend ratio showed an unchanged electrical behavior after undergoing 100 continuous characteristics measurement cycles with respect to all other types of OFETs, which demonstrated a large spread in their electrical characteristics.

3.2 EFFECT OF POLYMER ADDITIVES

Solution processing of organic semiconductors is an aid towards low cost and large area processability and is a step towards developing the printed electronic technology. Small molecule organic semiconductors are widely used in OFET technology but they suffer from various solubility issues and thus a lot of research is carried out in past few decades for the addition of soluble side groups in conjugated cores which have increased the solubility of small molecule organic semiconductors to a great extent in common organic solvents [Anthony et al.,2001, Sheraw et al.,2003]. Another issue with these semiconductors is the formation of uniform and large-area reproducible films. Due to the low viscosity of small molecule-based solutions, dewetting is a major issue that results in non-homogeneous and discontinuous films. One of the simplest and effective solutions to the above-mentioned problems is the use of semiconductor: polymer blends in the active layer [Smith et al.,2010, Lee and Park,2014, Riera-Galindo et al.,2018, Riera-Galindo et al.,2019]. The strategy also helps in improving the device performance with an increase in the crystallinity of the drying film and also provide a high-quality dielectric: semiconductor interface, due to slow solvent evaporation [Richter et al.,2017]. If the polymers binder used is chosen carefully is can also be used to reduce the surface defects of the inorganic dielectric and can act as a barrier layer that does not allow moisture to reach the inorganic layer surface. The advantages can further be increased if the dielectric: semiconductor interface is obtained by proper phase separation, which further results in a better quality interface due to surface energy-driven phase-separated interface between the polymer and organic semiconductor film.

In small-molecule conjugated systems with the use of polymer binder, the benefits were first seen with rubrene based OFETs [Stingelin-Stutzmann et al.,2005]. Obtaining good quality rubrene layer was always a difficult task because of its poor film-forming capability and its tendency to oxidation. Using polymer binder with rubrene not only improve the thin film formation but also improved the device performance with controlled organic semiconductor crystallization. It was seen that changing the polymer binder drastically change the device performance due to phase separation and has effected the electronic properties of OFETs. Since then a range of polymer binder has been used with various semiconductors, for instance, 6,13-bis (triisopropylsilylethynyl)pentacene (TIPS-PEN) which is considered as a high mobility OSC and

is also used in our study is extensively used with various polymer binders like polystyrene (PS), poly(α-methylstyrene) (PάMS) etc. The improve quality of films and high-quality dielectric: semiconductor interface also allow researchers to use blend in various coating techniques like drop-casting, bar coating spray coating etc. Similar to TIPS-pentacene various other semiconductors like 5,11-bis(triethylsilylethynyl) anthradithiophene (TES-ADT), 2,7-Dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT), 2,8-difluoro5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TESADT) etc. have been widely used with various polymer bidders in high performance OFETs. Some of these blend systems with their obtained mobilities are listed in Table. 3.1. With the aim of achieving high performance in flexible OFET devices and to improve the electromechanical stability, the study on the effect of mixing ration on device performance is illustrated in this chapter.

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Table 3.1 : Summary of some high performance semiconductor: polymer blend OFETs with their deposition strategy.

OSC.	**Insulating Binder**	**Deposition Method**	**μ ($cm^2 V^{-1}s^{-1}$)**	**Op. Vol. (V)**	**Reference**
P3HT	PS	Drop Casting	0.24	80	[Bu et al.,2018]
C_{10}–DNBDT–NW	PMMA	Blade Coating	10.6	30	[Soeda et al.,2016]
QBS	PVN	Spin Coating	0.12	100	[Kang et al.,2017]
Rubrene	PS	Drop Casting	0.7	20	[Stingelin-Stutzmann et al.,2005]
C8-BTBT	PS	Blade Coated	12	80	[Haase et al.,2018]
C5-BTBT	PS	Spin Coating	0.46	60	[Ljubic et al.,2016]
TES-ADT	PMMA	Spin Coating	0.47	20	[Lee et al.,2009]
TIPS-Pen.	PS	Blade Coating	8.3	1	[Teixeira da Rocha et al.,2018]
DPP-CN	PαMS	Spin Coating	0.5	60	[Zhong et al.,2012]
DPTTA	PS	BAMS	1	20	[Campos et al.,2018]
PDI-RN2	PS	Spin Coating	0.16	60	[Amegadze and Noh,2014]
PDI8CN2	PS	BAMS	0.028	20	[Campos et al.,2018]
DNTT	PS	Spin Coating	3.35	50	[Hamaguchi et al.,2015]
DPP6T	PMMA	DIP Coating	0.55	80	[Zhang et al.,2018]

3.3 EXPERIMENTAL

In the study, OFETs were fabricated in top-contact bottom-gate architecture on indium tin oxide (ITO) coated flexible polyethylene terephthalate (PET) substrates (thickness = 127 µm, surface resistivity 60 Ω/sq.). The schematic of devices fabricated in the study is shown in Figure 3.1. Prior to device fabrication, the substrates were cleaned with a similar procedure as discussed in section 2.1. Over the cleaned substrates a 40 nm thick dielectric layer of HfO_2 was deposited on these substrates by atomic layer deposition at 100 °C using tetrakis(dimethylamido)hafnium (TDMAH) and H_2O as precursors. 0.5 wt. % solution of TIPS-pentacene and poly(styrene) (M_W ~ 280,000) were prepared separately in toluene by stirring at 70 °C for 3 hours. Various blend solutions were then prepared by mixing TIPS-pentacene and polymer stock solutions in 3:1, 1:1 and 1:3 ratios by volume, followed by stirring for 30 minutes. To make the active organic semiconductor layer, neat/blend solutions were dispensed on HfO_2 deposited substrates. Just after drop cast, the substrates were covered with a glass petri dish to provide a solvent rich environment to the drying film. All solution preparations and sample processing steps were done in dark and ambient conditions. An Au layer (thickness of 200 nm) was thermally deposited through shadow masks under a high vacuum of 10^{-6} Torr to form Source-Drain contacts. Characterization and analyzing tools are similar as discussed in chapter 2. All measurements were performed in ambient conditions with the relative humidity ~20%. After characterization, the devices were stored in a vacuum. Device performance is definite to vary with the oxygen content of the air. However, relatively constant environmental conditions were maintained near the measurement setup. μ_{sat} and V_{TH} were extracted from the highest slope of the linear fit of $|I_{DS}|^{1/2}$ vs. V_{GS} plots using the saturation region drain current Eq. (2.4). Four types of devices namely neat, 3:1, 1:1 and 1:3 blend were fabricated and the values of C_i for neat and blend devices have been measured from metal-insulator-metal (MIM) capacitors and metal-insulator-semiconductor (MIS) structure respectively and found to have values of 200, 31(±5.9) , 27.4(±1.94), and 21.11(±1.84) nF/cm² at 1 KHz for neat, 3:1, 1:1 and 1:3 blend films.

To explore the bending stability, devices were subjected to tensile strain along the channel direction by bending the substrate with radius R_{bend} of 5.0 mm. The strain on the device was calculated using Eq. (2.8).

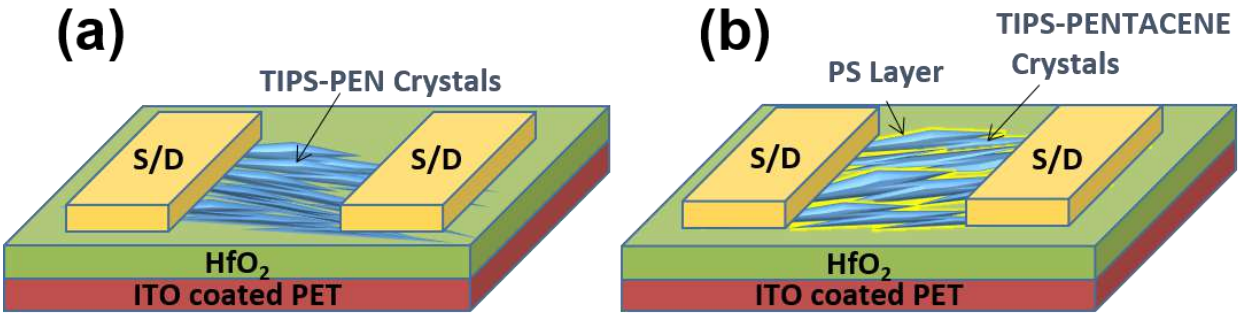

Figure 3.1 : Schematic representation of bottom gate top contact OFETs fabricated with (a) Neat and (b) Blended active layer.

3.4 RESULTS AND DISCUSSION

3.4.1 Effect on Crystallinity and Surface Morphology

Figure 3.2 (a-d) shows the surface morphologies of the TIPS-pentacene crystals obtained from four kinds of solutions. Surface morphologies for all four types of crystals were found to be identical, which suggests that the terracing structure of the TIPS-pentacene crystal does not vary with the proportion of TIPS-pentacene in the solution.

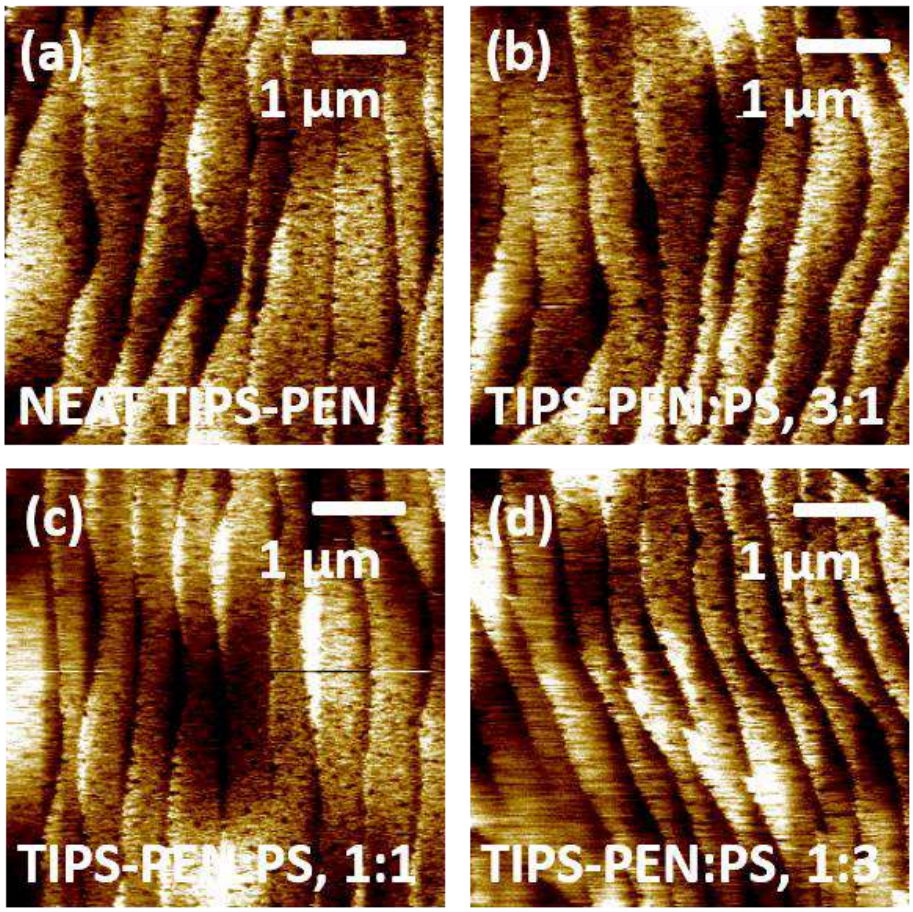

Figure 3.2 : Surface morphology of semiconductor crystals obtained from solutions of neat TIPS-pentacene (a), TIPS-pentacene: PS blends in the ratio of 3:1 (b), 1:1 (c), and 1:3 (d), showing similar terracing structure.

Figure 3.3 shows the X-ray diffractograms for four types of TIPS-pentacene films. The degree of crystallinity of all the crystals resulting from the blend solutions was higher than that of the neat TIPS-pentacene. The full width at half of the maximum (FWHM) was found to decrease with increasing polymer content; 0.18 for neat TIPS-pentacene films to 0.023 for 1:1 TIPS-pentacene:PS film, indicating an increase in the crystallinity. The crystallinity of TIPS-pentacene depends on its amount in the solution and the rate of solvent evaporation from the film. Though the semiconductor content decreases from neat TIPS-pentacene to 1:1 TIPS-pentacene: PS case, the crystalline order still improves, which can be explained with the kinetics of the film formation by solvent evaporation from the semiconductor: polymer blend solutions [Lee et al.,2012].

The process of solvent evaporation is quite complicated with the interplay of various related factors like vapor pressure, temperature, surface area to volume ratio etc [Lim et al.,2008, Kim et al.,2014]. In the initial stages, solvent evaporation is vapor pressure controlled and unaffected by the presence of the solute. However, as the solvent evaporates, the solution turns more viscous and solvent evaporation is limited by the diffusion of the solvent molecules to the surface of the solution. The rate of solvent evaporation is relatively slower for the case of a blend solution than that for a neat TIPS-pentacene solution due to increased viscosity of the blend solutions resulting from the added polymeric insulator. Rise in fraction of the polymer in the semiconductor: polymer blend solution leads to further increased viscosity. As the solvent evaporates from the blend solution, the viscosity further increases and, free volume decreases. All these factors retard the rate of solvent evaporation. However, during the slow process of solvent evaporation, semiconductor molecules get the sufficient time to improve their arrangement and enhance crystalline order in the final film [Kim et al.,2008]. Thus, abundance of polymer in the solution results in to a slower rate of the solvent evaporation and eventually to a more crystalline

final film. However, for 1:3 TIPS-pentacene:PS film, the FWHM value increases slightly, which is associated more with the reduced semiconductor content rather than the reduced solvent evaporation rate-dependent crystallinity.

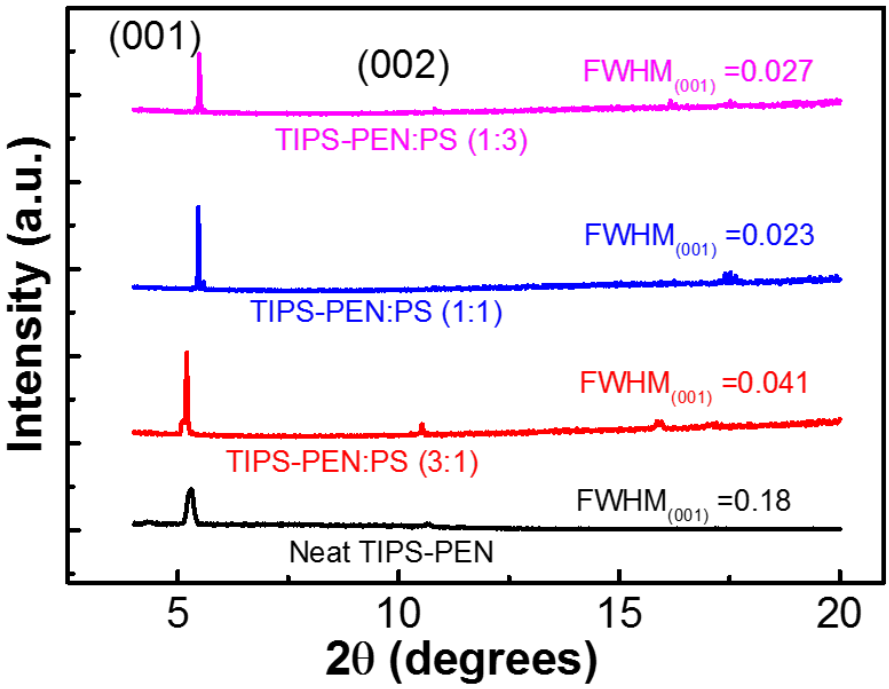

Figure 3.3 : X-ray diffractogram of semiconductor crystals obtained from neat and blended active layer films, showing an increase in crystalline nature with the increase in PS content.

3.4.2 Electrical Performance

Figure 3.4 shows the electrical characteristics of OFETs corresponding to all the four cases. Table 3.2 summarizes various electrical parameters for all four types of OFETs. 1:3 TIPS-pentacene: PS blend OFETs outperform other types of OFETs with an average and maximum field-effect mobility of 0.37(±0.14) and 0.57 $cm^2 V^{-1} s^{-1}$ while operating at a low voltage of -5 V. 1:1, 3:1 blend and neat OFETs show average field-effect mobility of 0.19(±0.04), 0.18(±0.04), and 0.05(±0.01) with maximum of 0.25, 0.24 and 0.08 $cm^2 V^{-1} s^{-1}$ respectively. The higher performance of blend OFETs can be attributed to the formation of a uniform dielectric-semiconductor interface through the process of vertical phase separation (resulting in TIPS-pentacene: PS: TIPS-pentacene tri-layer structure [Bharti and Tiwari,2016]) and several associated factors [Kang et al.,2008, Smith et al.,2012]. Foremost among them can be the enhanced quality of the active semiconductor layer due to slowest solvent evaporation in polymer-rich 1:3 blend films in comparison to all other cases as discussed before, which causes ameliorated charge transport in the corresponding films. The second reason can be the decreased dipolar disorder and carrier localization at the PS: TIPS-pentacene interface, which reduces the broadening of the density of states leading to a lower density of trap states than that in the neat device [Veres et al.,2003, Hulea et al.,2006, Kalb et al.,2010]. However, the reasons of increasing device performance with increasing polymer fraction are not yet completely understood. However, further deficiency of the semiconductor in the blend solution will obviously lead to performance roll-off, as also suggested by some previous reports [Madec et al.,2008, Cho et al.,2013]. This loss in the performance has been reasoned with the discontinuous active material film formation due to reduced semiconductor content.

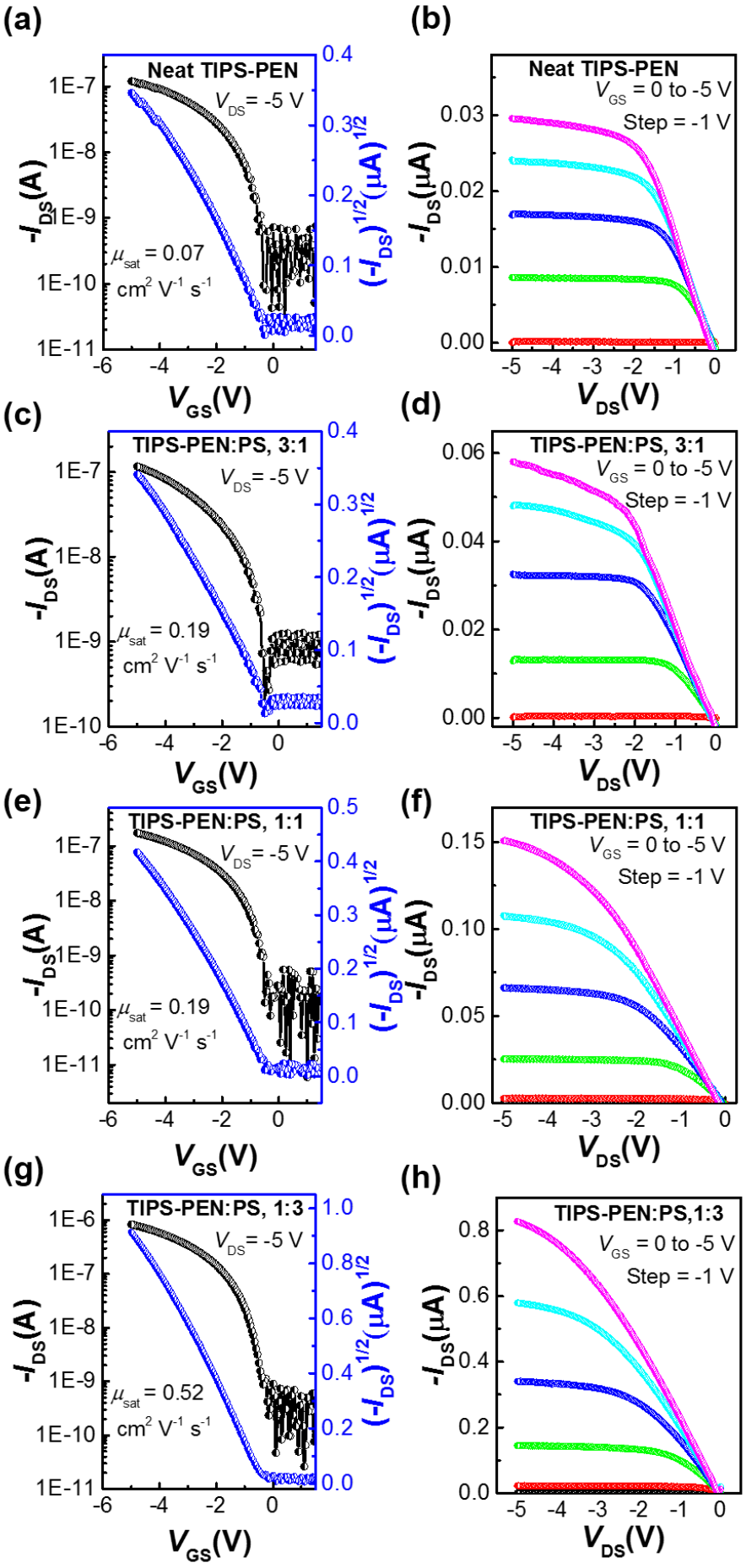

Figure 3.4 : Transfer and output characteristics of representative neat TIPS-pentacene OFET (a) & (b), TIPS-pentacene:PS blend OFET with mixing ratio of 3:1 (c) & (d), 1:1 (e) & (f), and 1:3 (g) & (h).

Table 3.2 : Summary of the extracted electrical parameters for neat and blend OFETs.

Device	C_i (nF/cm²)	μ_{sat} (cm²/Vs)	μ_{max} (cm²/Vs)	V_{TH}(V)	I_{on}/I_{off}
Neat	200	0.05(±0.01)	0.08	-0.55(±0.61)	~10^3
3:1	31	0.18(±0.04)	0.24	-0.44(±0.24)	10^4-10^5
1:1	27.4	0.19(±0.04)	0.25	-0.9(±0.28)	10^4-10^5
1:3	21	0.37(±0.14)	0.57	-0.42(±0.2)	10^4-10^5

3.4.3 Electromechanical Stability of Blend OFETs

Figure 3.5 (a) shows the decay in the normalized drain current at biasing conditions of V_{DS} = V_{GS} = -5 V for 1 hour for all cases. Under constant bias-stress conditions, drain current decreases for all the cases due to charge trapping in various regions in the device including the bulk of the semiconductor, the disordered areas of semiconductor, the grain boundaries of the semiconductor, and at the dielectric-semiconductor interface [Salleo et al.,2005, Chang and Subramanian,2006, Street et al.,2006]. This charge trapping leads to a shift in the threshold voltage of the device. Neat devices exhibit the highest decay in the drain current due to large number of defects present on the HfO_2 surface, acting as trapping centers. Whereas in the blend devices, the degree of charge trapping is limited due to relatively uniform dielectric-semiconductor interface resulting in reduced broadening of the density of states, ultimately leading to a lesser density of trap states on low-*k* PS surface. 1:3 blend devices exhibit excellent bias stress stability with the least decay in drain current ~2 % in comparison to that of 11.2 %, 17.8 % and 41 % for 1:1 and 3:1 blend and neat OFETs respectively. One of the possible reasons for the increasing trend of bias stress stability can be the lesser number of trapping locations available with reduced semiconductor content.

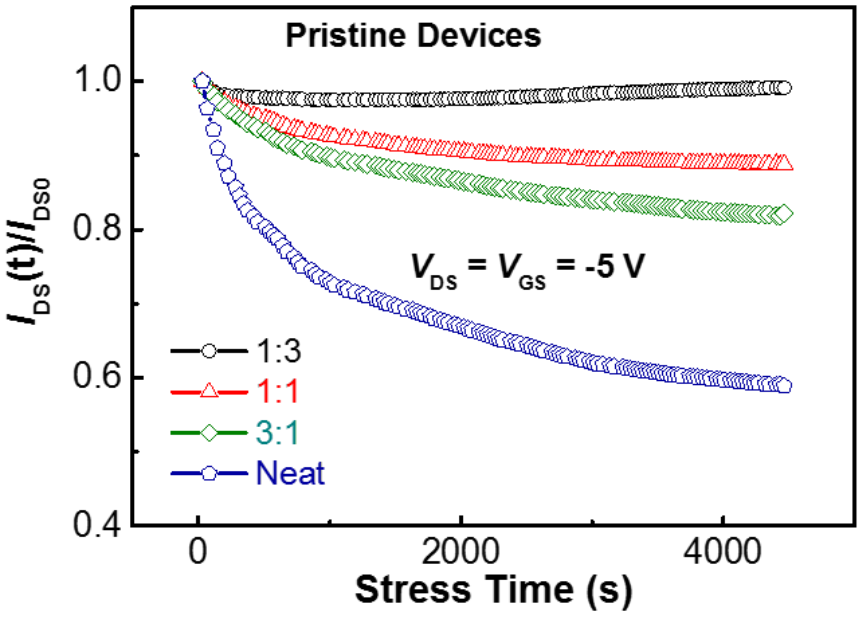

Figure 3.5 : Bias stress-induced decay in normalized drain current for various TIPS-pentacene OFETs for pristine devices.

To investigate the effect of mechanical strain on the bias stress stability, various blend devices were subjected to a tensile stress of 1.27 % (bending radius of 5 mm) for 1 hour, the examination strategy is depicted in Figure 3.6. To bend the devices, the sample was tightly pasted over a cylindrical tube of desired radius for one hour and further characterized in pristine state.

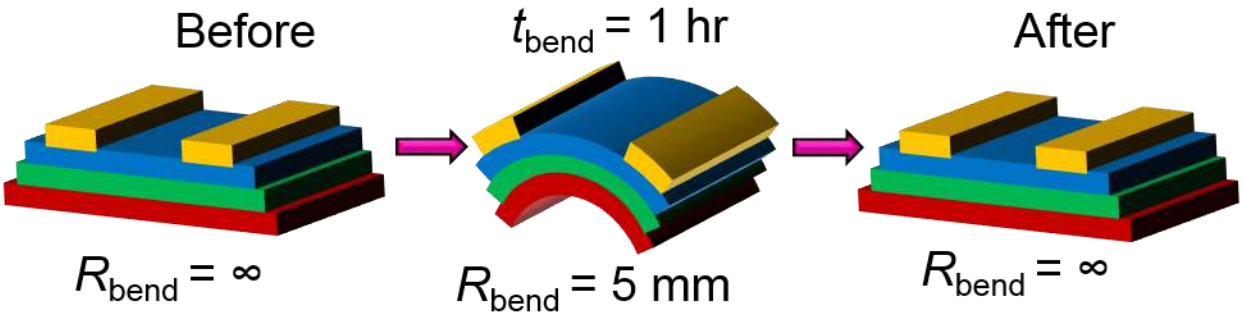

Figure 3.6 : Demonstration of bending strategy used to test the electromechanical stability.

The decay in the normalized drain current at the same biasing conditions as that used in the unstrained case (V_{DS} = V_{GS} = -5 V for 1 hour) was measured for all cases and shown in Figure 3.7(c). The drain current decay in strained devices was found to be similarly dependent on the blend ratio, as observed for pristine devices, however, the magnitude of the decay was increased. Strained 1:3 blend devices showed the least decay of 11 % in compared to strained 1:1, 3:1 and neat devices with 20 %, 26 % and 44 % respectively. The larger magnitude of current decay in strained devices can be attributed to the generation and propagation of micro-defects/cracks in the semiconducting crystal or at the dielectric-semiconductor interface which depends on several factors including modulus mismatch between film and substrate, film-thickness and interfacial adhesion [Lewis,2006, Leterrier et al.,2010]. The generation and propagation of such defects/cracks under applied mechanical strain deteriorate dielectric-semiconductor interfacial conditions. Such defects act as additional charge trapping locations, resulting in higher drain current decay.

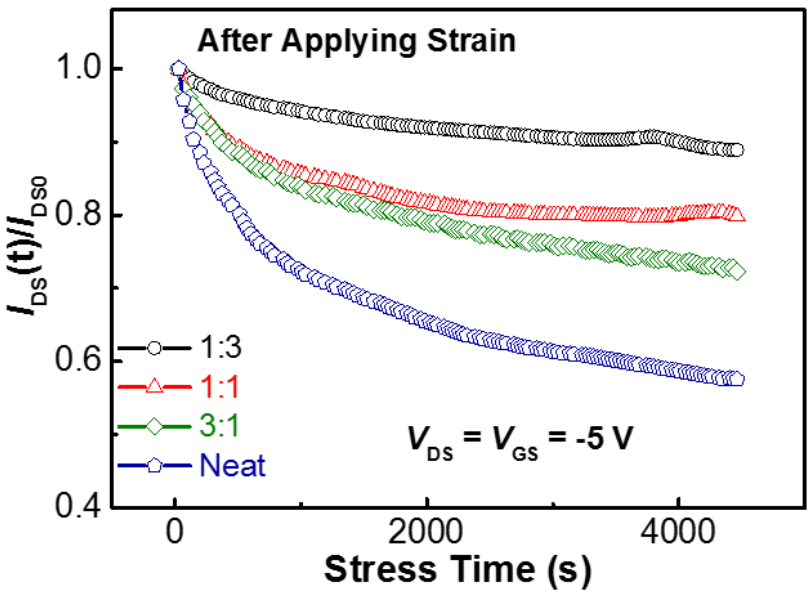

Figure 3.7 : Bias stress-induced decay in normalized drain current for various TIPS-pentacene OFETs after applying strain.

Mathematically, the normalized decay in the drain current in the saturation regime can be expressed as the ratio of the I_{DS} at time t and 0 s, and can be given by Eq. (2.6) and the corresponding shift in the threshold voltage can be represented mathematically as a stretched exponential function given by Eq. (2.8).

For both the unstrained and strained situations, values of β (which reflects the width of involved trap distribution) and τ (a measure of typical trapping time of charge carriers) have been extracted for all the four cases by fitting the experimental data in 2.7 and given in Table 3.3.

Table 3.3 : Extracted electrical parameters before and after applying strain.

Device	I_{DS} Decay (%)		β		τ (s)		ΔV_{TH} (V)	
	Before	*After*	*Before*	*After*	*Before*	*After*	*before*	*After*
Neat	41	44	0.437	0.423	8.3×10^{4}	8.4×10^{4}	1.06	1.1
3:1	17.8	26	0.471	0.429	5.4×10^{5}	2.6×10^{5}	0.48	0.76
1:1	11.2	20	0.375	0.337	6.8×10^{6}	2.2×10^{6}	0.30	0.56
1:3	~2	11	0.313	0.446	1×10^{9}	2.7×10^{6}	0.05	0.27

The highest value of τ is obtained for 1:3 blend OFETs which indicate the least degree of charge trapping among all the four cases because of previously mentioned reasons. The value of τ decreases with increasing semiconductor content signifying the aggravating extent of charge trapping in the corresponding devices. Shifts in threshold voltages for all cases have been calculated using equation 2.8 and have been plotted in Figure 3.8.

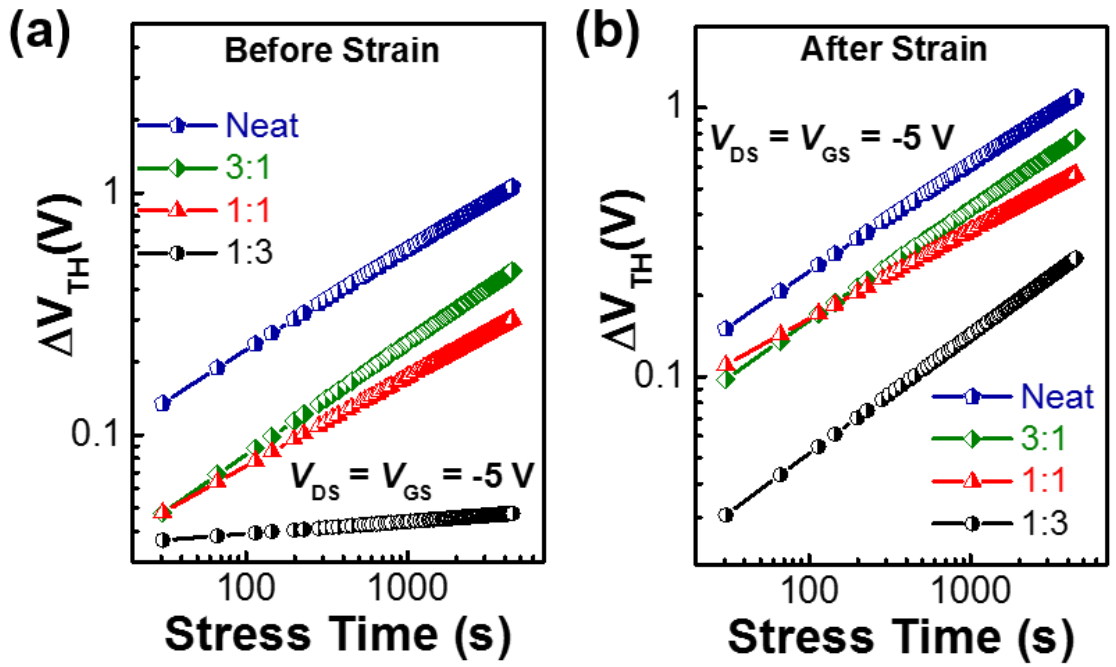

Figure 3.8 : Threshold voltage shift as a function of stress duration for various TIPS-pentacene OFETs for (a) pristine and (b) strained condition.

As per the discussion before, due to lesser charge trapping in blend devices, incurred shifts in threshold voltages are also lesser. Due to very high τ value, the associated threshold voltage shift for 1: 3 blend device is also the minimum 0.05 V (Figure 3.8 (a)), which indicates a highly uniform interface with lesser defects in the aforementioned device. The corresponding threshold voltage shifts in 1:1 and 3:1 blend devices and neat devices after 1 hour of bias stress $V_{DS} = V_{GS} = -5$ V followed an increasing trend and were 0.30 V, 0.475 V, and 1.06 V respectively, suggesting sequential inferiority of the interface quality and aggravated charge trapping. As observed for pristine devices, 1:3 blend devices exhibited the largest value of τ and least threshold voltage shift of 0.27 V (Figure 3.8 (b)) among all categories of strained blend devices, which indicates lesser defect generation and extent of charge trapping in these devices even after strain application. The corresponding threshold voltage shifts in 1:1 and 3:1 blend devices and neat devices after 1 hour of bias stress ($V_{DS} = V_{GS} = -5$ V) followed a similar increasing trend and were 0.56 V, 0.76 V, and 1.1 V respectively, each higher than that of respective pristine devices. This indicates an increasing degree of charge trapping with decreasing polymeric insulator content under combined effects of mechanical strain and bias-stress, which was also predicted by decreasing τ values, as obtained for pristine devices.

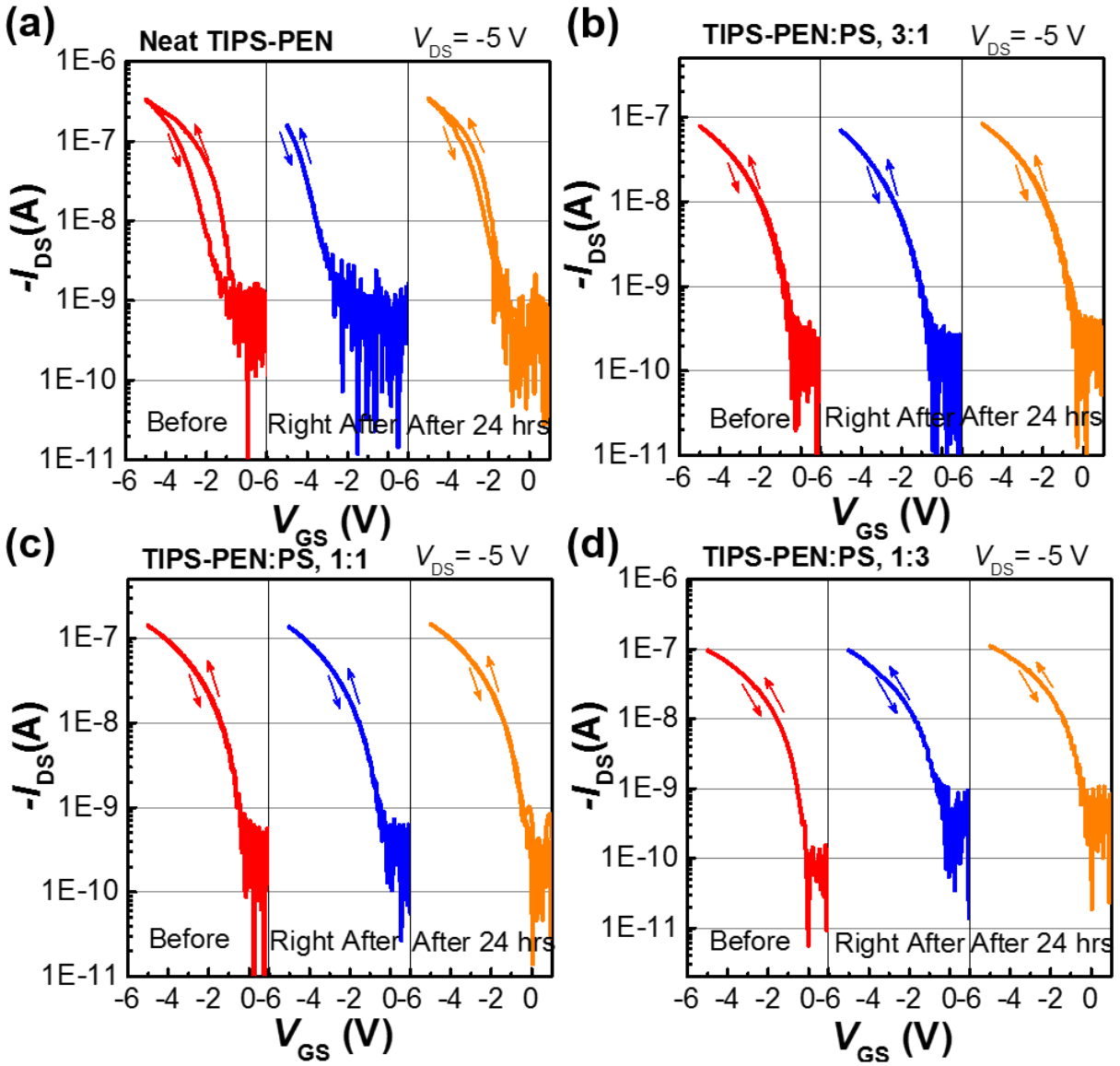

Figure 3.9 : Recovery characteristics after bias stress of a representative neat TIPS-pentacene OFET (a), TIPS-pentacene:PS blend OFET with mixing ratio of 3:1 (b) 1:1 (c), and 1:3 (d) in pristine situation.

To study the reversibility of the bias stress effect, transfer curves of the stressed devices were recorded just before stressing, just after stressing and after 24 hours of stress. These transfer curves for all cases recorded in both sweep directions have been shown in Figure 3.9 (a-d). As per inferences drawn earlier, neat devices suffer from a larger shift in threshold voltage after application of bias stress due to large density of trap states, which are not occupied completely even during the stress period. However, the trap sites available at relatively uniform dielectric-semiconductor interface in the blend devices are lesser and are completely filled during the stress period as indicated by the overlapping of transfer curves of both sweep directions for all the blend devices, ultimately leading to very small threshold voltage shift. Interestingly, both transfer characteristics overlap each other and shifts in threshold voltage are negligibly small in 1:3 blend OFETs, in all the three conditions, suggesting the least density of trapping locations available, possibly due to reduced semiconductor content.

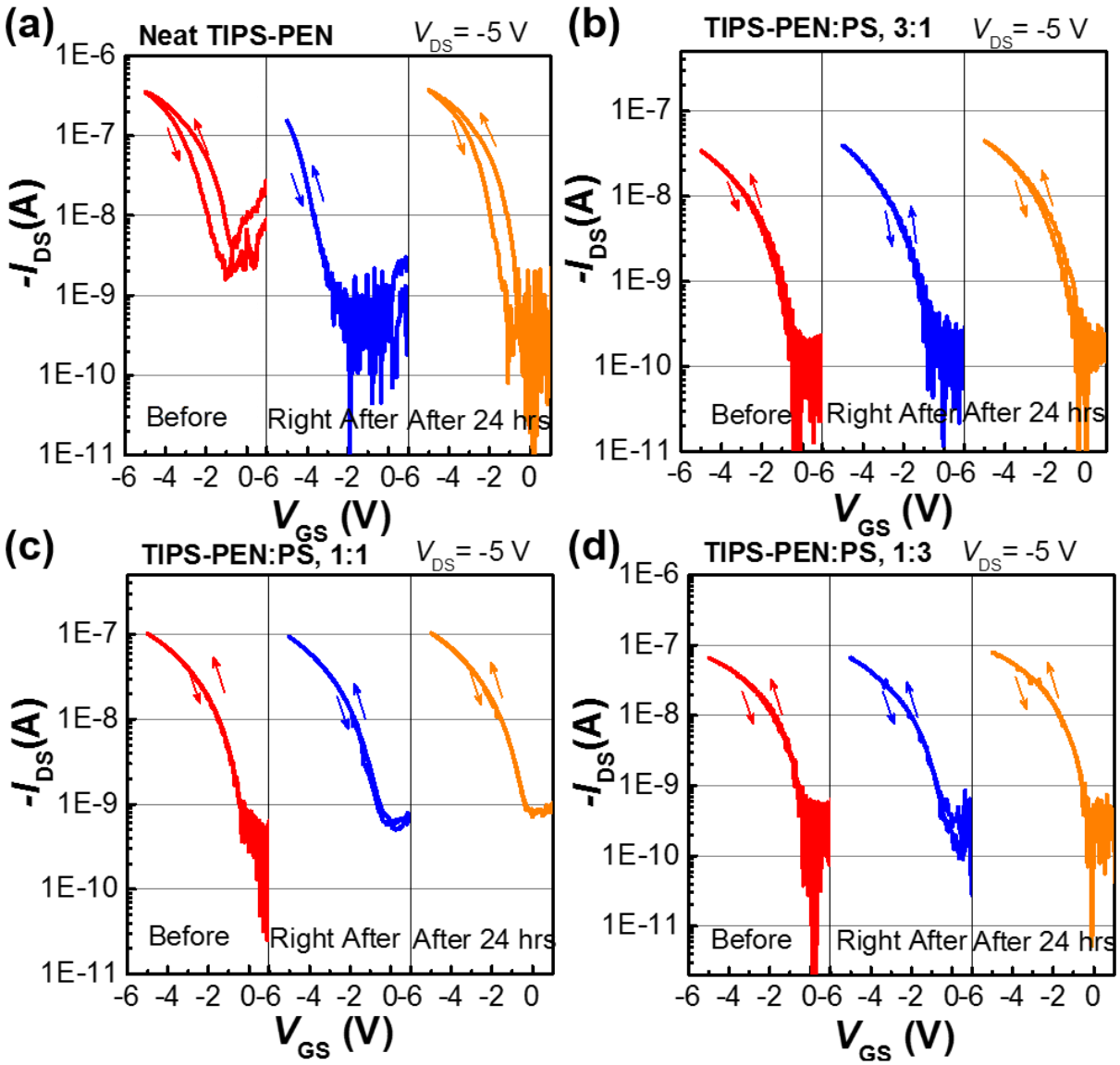

Figure 3.10 : Recovery characteristics after bias stress of a representative neat TIPS-pentacene OFET (a), TIPS-pentacene: PS blend OFET with mixing ratio of 3:1 (b) 1:1 (c), and 1:3 (d) after applying strain.

All types of devices are recovered almost completely during rest duration of 24 hours, showing identical threshold voltages, on currents to that of the pristine devices. In addition, the hysteresis areas in both cases are largely equal. This observation suggests that charge trapping in all kinds of devices takes place mostly in the shallow trap sites. Under rest conditions, with thermal

energy, charge carriers easily de-trap from these shallow trap sites and density of trap states in the devices are replenished, which is clearly reflected from recovered threshold voltages, on currents and areas of hysteresis. In a report from our group, where the devices on Si/SiO_2 were operated at -30 V, TIPS-pentacene: PS blend devices were almost recovered, however, neat TIPS-pentacene devices on Si/SiO_2 were not recovered completely due to severe charge trapping in the deep trap sites.

Comparison of the discussed two cases suggests that charge trapping in the deep or shallow trap sites may be a voltage (energy of the charge carriers) dependent and /or ALD HfO_2 has a lesser number of deep trap sites than thermally grown SiO_2. Similar observations were also made in the bias stress reversibility studies conducted after the application of tensile strain, as shown in Figure 3.10 (a-d). Though after mechanical deformation an evident performance degradation was observed which was found to diminish with increasing polymer content, quantitative and qualitative inferences about trap state dynamics drawn for pristine devices remain valid for strained devices as well. In addition, the electro-mechanical stability was tested by sequentially subjecting devices to 100 continuous transfer characteristics measurement cycles, 1.27 % strain application for 1 hour followed by another set of 100 transfer characteristics measurement cycles. Results obtained from this study are shown in Figure 3.11(a-d).

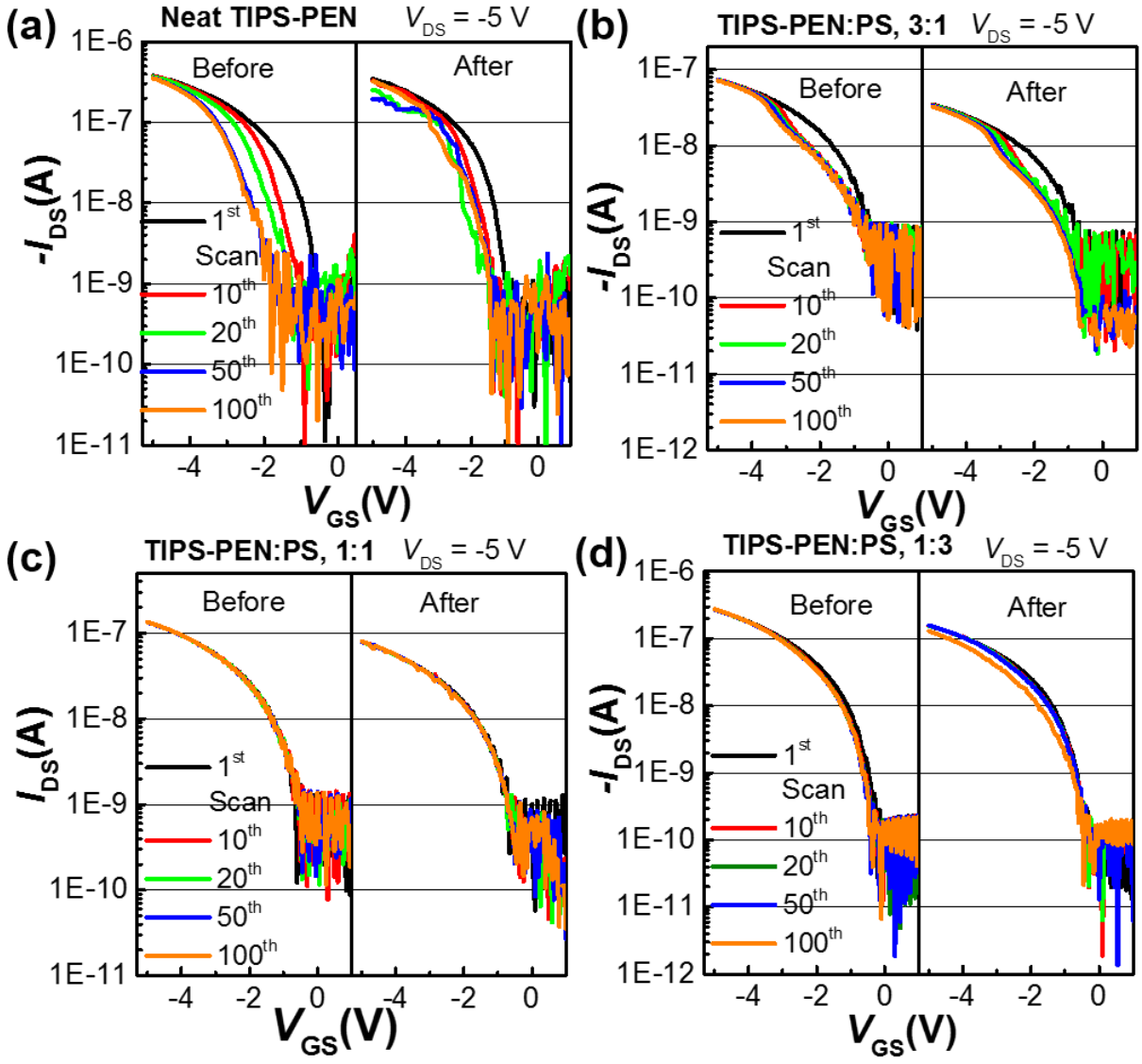

Figure 3.11 : (a) Transfer characteristics of a representative neat TIPS-pentacene OFET, TIPS-pentacene:PS blend OFET with mixing ratio of 3:1 (b), 1:1 (c), and 1:3 (d) before and after 100 measurement cycles.

Before the application of strain, measurement cycles cause huge performance spread in neat devices due to the inferior quality of the dielectric-semiconductor interface, causing a large degree of charge trapping. Performance spread in blend devices is lesser due to earlier discussed reason of uniform dielectric-semiconductor interface and is reduced with the increasing polymer content in the film. 1:3 and 1:1 blend devices show the least performance spread due to similar reasons of a lesser number of available trap sites with reduced semiconductor content. After bending the devices at 1.27% tensile strain for 1 hour, neat TIPS-pentacene devices continue to show large performance spread. However, the blend devices continue to operate reliably for another set of 100 measurement cycles even after 1 hour of strain, nonetheless with some evident performance degradation. Performance roll-off on the application of mechanical strain can be explained with the manifestation of micro-defects in the semiconducting crystal or at the dielectric-semiconductor interface, as discussed earlier. After the application of strain, performance spreads in blend devices are increased due to the aforementioned reasons for performance degradation; however, a similar trend of decreasing performance spread with increasing polymer fraction is still preserved.

3.5 CONCLUSIONS

In this chapter, the relation between the mixing ratio of semiconductor and polymer solutions on the electro-mechanical stability of the TIPS-pentacene:PS blend OFETs is investigated. The performance of OFETs was found to increase with increasing polymer content in the solution. The maximum field-effect mobility increased from 0.08 for neat TIPS-pentacene OFETs to 0.24, 0.25 and 0.57 $cm^2 V^{-1} s^{-1}$ for semiconductor: polymer blend with mixing ratio of 3:1, 1:1 and 1:3 respectively. Small drain current decay values of ~2% and 11% and small values of threshold voltage shifts of 0.05 V and 0.27 V were observed for 1:3 blend devices under the gate bias stress before and after strain application respectively. Devices exhibited almost a complete recovery from the degrading effects of gate bias stress. In comparison to all other types of OFETs, which showed a large spread in their electrical characteristics for 100 continuous measurement cycles before and after application of mechanical strain of 1.27 % for 1 hour, OFETs with 1:3 semiconductor: polymer blend ratio showed a highly stable electrical performance.

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