4
Flexible OFETs with High-k BST Gate Dielectric

One of the major concerns in electronic devices is reducing the operating voltage and also a major goal of the research work undertaken in this thesis is to improve operational stability along with reducing the operating voltage in flexible devices. Among the three major constituents (electrodes, dielectrics and the semiconductor) in OFETs, gate dielectric stack is the most sophisticated part and plays a crucial role in deciding the performance, reliability and operating voltage of the device. The reduction in operational voltage is directly linked with the capacitive density of the gate stack and which in turn directly proportional to the dielectric constant and area of the dielectric and is inversely proportional to the thickness of the layer. With shrinking device dimensions, effective dielectric layer area cannot be increased and the reduction in dielectric layer thickness may lead to an increase in leakage currents. However, utilizing the benefits of the high-k dielectric layer can be a great strategy towards lowering the operating voltage requirement. In addition, to utilize the high-k dielectric in a flexible device the deposition temperature must be compatible with flexible substrates. In this chapter, improved device performance with low operating voltage in flexible OFETs by utilizing the benefits of room-temperature deposited BST gate dielectric is discussed. The results discussed in this chapter have been recently published [Raghuwanshi et al.,2020].

4.1 INTRODUCTION

OFETs are the key component in many potential applications, such as active matrix display circuitry, biosensors, memories, and radio frequency identification (RFID)[Peng et al.,2014, Lai et al.,2016, Ren et al.,2016, Chen et al.,2018]. The performance of OFETs is today comparable to amorphous silicon devices. However, lowering the operating voltage and reducing the processing temperature are the key factors and are still the field of exploration for portable and flexible battery-operated devices. Low voltage operation signifies sufficient charge accumulation at the dielectric-semiconductor interface with low power applied. Dielectric materials are the core of the transistor that affect the operational voltage directly. The induced accumulated charges at the dielectric-semiconductor interface are proportional to the capacitance density C_i (Capacitance per unit area) of the dielectric insulator, which in turn is proportional directly and inversely to the dielectric constant and thickness of the material respectively. The C_i can be increased either by reducing the thickness of the dielectric layer or by using dielectrics with high dielectric constant. Reducing the dielectric layer thickness may lead to an increase of leakage current through the gate, which is undesirable for high-performance OFETs. Alternatively, the charge accumulation at low operating voltages can be increased by employing dielectrics with high dielectric constant. The high dielectric constant dielectrics also allow a larger thickness of the dielectric layer to reduce the leakage current. In the past few years high-*k* dielectrics like HfO_2, Al_2O_3, $ZrTiO_x$, ZrO_2, BTO, BST, etc. have been investigated to utilize them for low operating voltage OFET devices.

Table 4.1 summarizes some high-*k* dielectrics used in OFET fabrication with their processing temperature and substrate used in the study. These dielectrics are deposited either by physical or solution-processed methods. Most of these methods require high processing temperature, which is higher than the glass transition temperature of most of the flexible substrates like PET, PEN, etc., which hinders their suitability towards flexible electronics. A suitable dielectric

in flexible OFETs for low voltage operation must possess some properties like high dielectric constant, low leakage current, smooth surface morphology, higher stability and feasible low-temperature deposition. Considering the need for low temperature processable high-*k* dielectrics for low voltage flexible OFETs, we have proposed RF sputtered BST as a dielectric material for low voltage operation.

Table 4.1 : Summary of some high-k dielectrics used for low-voltage OFETs.

Dielectric Material	**Method of Deposition**	***Temp (°C)***	***Substrate***	**Reference**
$ZrTiO_x$	Spin Coating	750	Si	[Zhao et al.,2014]
HfO_x	Sol- gel Method	600	Si	[Acton et al.,2008]
BTO	Spin Coating	180	Glass	[Wei et al.,2010]
ZrO_2	Spin Coating	290	Glass	[Jang et al.,2013]
BST	Pulsed laser Deposition	110	PEN	[Wang et al.,2012]
HfO_2	Atomic Layer Deposition	100	PET	[Raghuwanshi et al.,2016]
Al_2O_3	Spin Coating	170	Si	[Sun et al.,2016]
HfO_2	Atomic Layer Deposition	200	Si	[Zhang et al.,2009]
STO	Sputtering	50	PET	[Yadav and Ghosh,2016]
BST	Solution Processing	400	Si	[Dimitrakopoulos et al.,1999]

In this Chapter, RF sputtered thin film of high-*k* dielectric material BST has been explored for room-temperature processed gate dielectric layer for low voltage OFETs. The growth conditions of the BST film were engineered to optimize the film for high-performance OFETs. The BST film properties such as dielectric constant, surface morphology and the crystallinity were found to be significantly dependent on the film deposition temperature. The room temperature deposited BST films were found to be amorphous in nature with low leakage current, high dielectric constant, smoother surface morphology, and high electromechanical stability. With the optimized BST as a dielectric layer, OFETs have been fabricated using TIPS-pentacene: PS as an active layer on the flexible substrate. The room temperature deposited BST have led to excellent electrical characteristics in flexible OFETs while operating at -5 V. The devices were found to be operationally stable with minuscule variation in electrical performance when bias stressed and when tested continuously for a large number of transfer scan cycles. The devices were found to be electromechanically stable with stable electrical characteristics in extreme bending situations. In addition, the fabricated OFETs have been shown to demonstrate long term bending stability for continuous tensile strain for a duration as large as 1 month. At a bending radius of 5 mm, even after strained for 1 month the devices have not shown much degradation in the electrical performance.

4.2 EXPERIMENTAL

4.2.1 BST Film Optimization and Device Fabrication

OFETs were fabricated in a bottom-gate top contact structure with optimized BST films as a dielectric layer. The high-*k* dielectric films of BST were deposited in an RF magnetron sputtering system by utilizing a high purity $Ba_{0.5}Sr_{0.5}TiO_3$ (99.99%) composite target of 2-inch diameter. BST was deposited on a highly doped n+ silicon substrate with different deposition parameters in order to evaluate ideal settings for optimizing film properties. Prior to the film deposition, the substrates were thoroughly cleaned by a bath in heated organic solvents i.e. 2-propanol, trichloroethylene, acetone, and methanol. The substrates were given a DI bath before heating to a particular solvent. The substrates were finally dried with a heavy nitrogen blow. The samples were loaded into the vacuum chamber and the base pressure as high as 4×10^{-7} was achieved. Under the optimized process parameters, BST films were deposited where the RF power was kept to 100 W, the substrate to target distance was fix to 5 cm, the working pressure and Ar flow rate was 2×10^{-2} mbar and 65 SSCM respectively. The thickness of the BST films was controlled by the growth time with the deposition rate of 0.1μm/hr. To obtain the desired dielectric properties in the film, the substrate holder temperature was varied from room temperature to as high as 600 °C. The optimized BST film was then deposited on flexible polyethylene terephthalate (PET) substrates (thickness = 127 μm, surface resistivity 60 Ω/sq.). The flexible substrates were cleaned in methanol, de-ionized water, and 2-propanol respectively, followed by drying in an N_2 blow before film deposition.

The highly doped n+ type silicon substrate with 70 nm BST films deposited at different temperatures, n+ type silicon substrate with 300 nm thermally grown SiO_2 and ITO coated PET with 70 nm BST films were cleaned with the standard cleaning process. To prepare the active layer solution, p-type semiconductor (6,13-Bis((triethylsilyl)ethynyl)pentacene) (TIPS-pentacene) and polymer binder polystyrene (PS) were individually dissolved in toluene with the concentration of 0.5 wt. %, both the solutions were stirred for 3 hrs. at 70 °C. After 3 hrs. to make the semiconductor: polymer blend solution, both the solutions were mixed in 1:1 ratio by volume followed by shaking of the solution for a few minutes. To form the active layer, the as-prepared blend solution was then drop cast on the substrates and the samples were covered with a glass petri dish to give solvent rich environment to the drying semiconductor film and left for few hours. The Au source and drain contacts were made in the thermal deposition system under a high vacuum of 10^{-6} Torr using shadow masks. Figure 4.1(a), (b) and 4.1(c), (d) shows the schematics and digital image of the fabricated rigid and flexible devices respectively. Figure 4.1(e) and (f) show the chemical structure of the semiconductor and the polymer binder used in the study. All the solution processing and device fabrication steps were done in dark and ambient conditions. Constant environmental conditions were maintained in the processing area. The exact channel length and width of the devices were taken from the length and sum of the width of the semiconducting crystals joining the source and drain region. The demonstrated transistors have channel width and length of 1500 μm and 150 μm respectively. The electrical characterization methods and tools used are similar as discussed in chapter 2.

4.2.2 Flexibility and Reliability Characterization

The operational stability of the fabricated OFETs was analyzed by measuring 500 transfer measurement cycles continuously one after another. Electrical measurements were observed with device bias stressed with $V_{DS} = V_{GS} = -5$ V. To test the reliability of the devices under strain conditions the devices were characterized after applying tensile strain with decreasing bending radius to as low as 5 mm. The devices were also characterized after applying multiple bending cycles to as high as 500 bend cycles. In addition, the long-term bending stability test was performed where the devices were bent to a 5 mm radius for a month duration and the electrical measurements were recorded periodically.

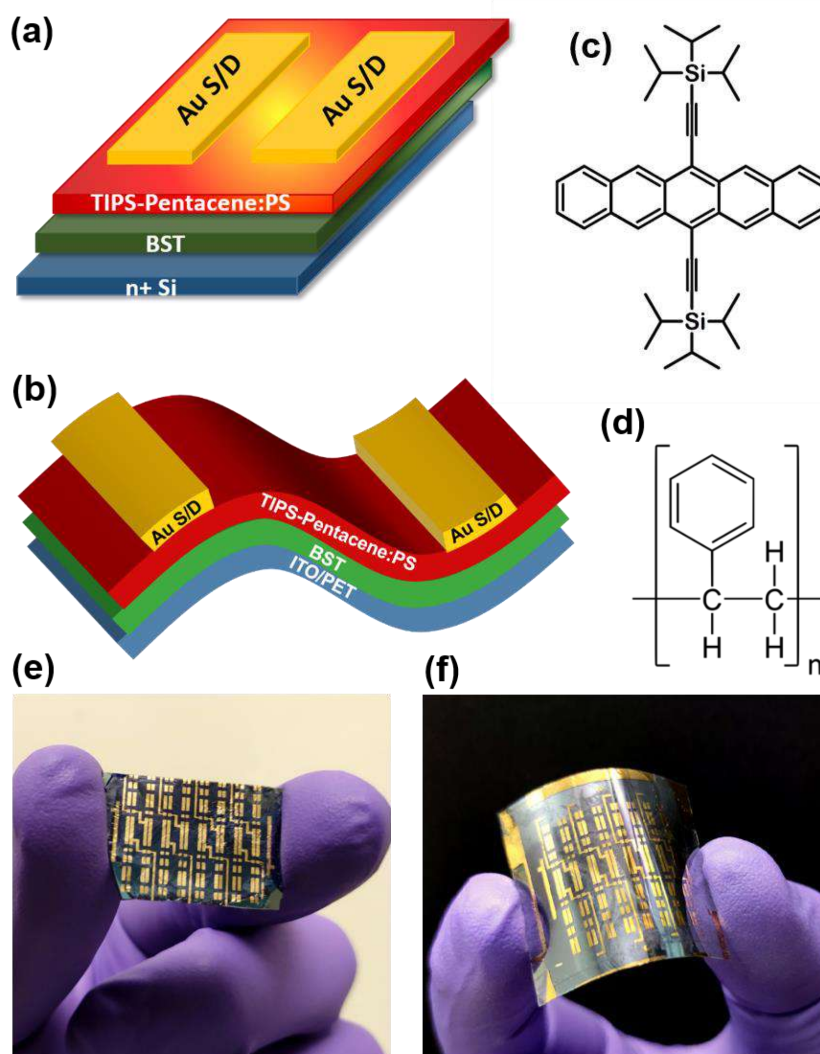

Figure 4.1 : (a), (b) Schematic representation and (c), (d) digital image of bottom gate top contact OFETs fabricated on rigid and flexible substrates. Chemical structure of (e) TIPS-pentacene and (f) Polystyrene used in active layer preparation.

4.3 RESULTS AND DISCUSSION

4.3.1 BST Characteristics with Deposition Temperature

The crystalline conditions of the deposited BST films were first studied through X-ray diffractograms (XRD) and the results are shown in Figure 4.2. In the XRD study, it was observed that the crystallinity of the BST film can be largely affected by the deposition temperature. The films were deposited from room temperature to 600 °C and it was found that the BST film was amorphous at low growth temperature, whereas films were found to have polycrystalline phase at a high temperature of 600 °C.

The surface roughness of the dielectric film is another crucial factor determining the performance of the OFETs. The charge carriers are accumulated at the dielectric: semiconductor interface. A smoother surface morphology leads to lesser trapping of charge carriers and in turn a better device performance. Figure 4.2 (b-f) show the Atomic force microscopy (AFM) images of the BST films grown at different deposition temperature. The surface roughness of the BST film was found to be 0.17(±.01) nm, 0.28(±.05) nm, 0.57(±.06) nm, 2.18((±.11) and 2.86(±.06) nm for room temperature (RT), 200 °C, 400 °C, 500 °C and 600 °C deposited BST film. With the increasing deposition temperature, surface roughness was found to increase. Variation of more than one order in the surface roughness was observed between the amorphous and the polycrystalline film.

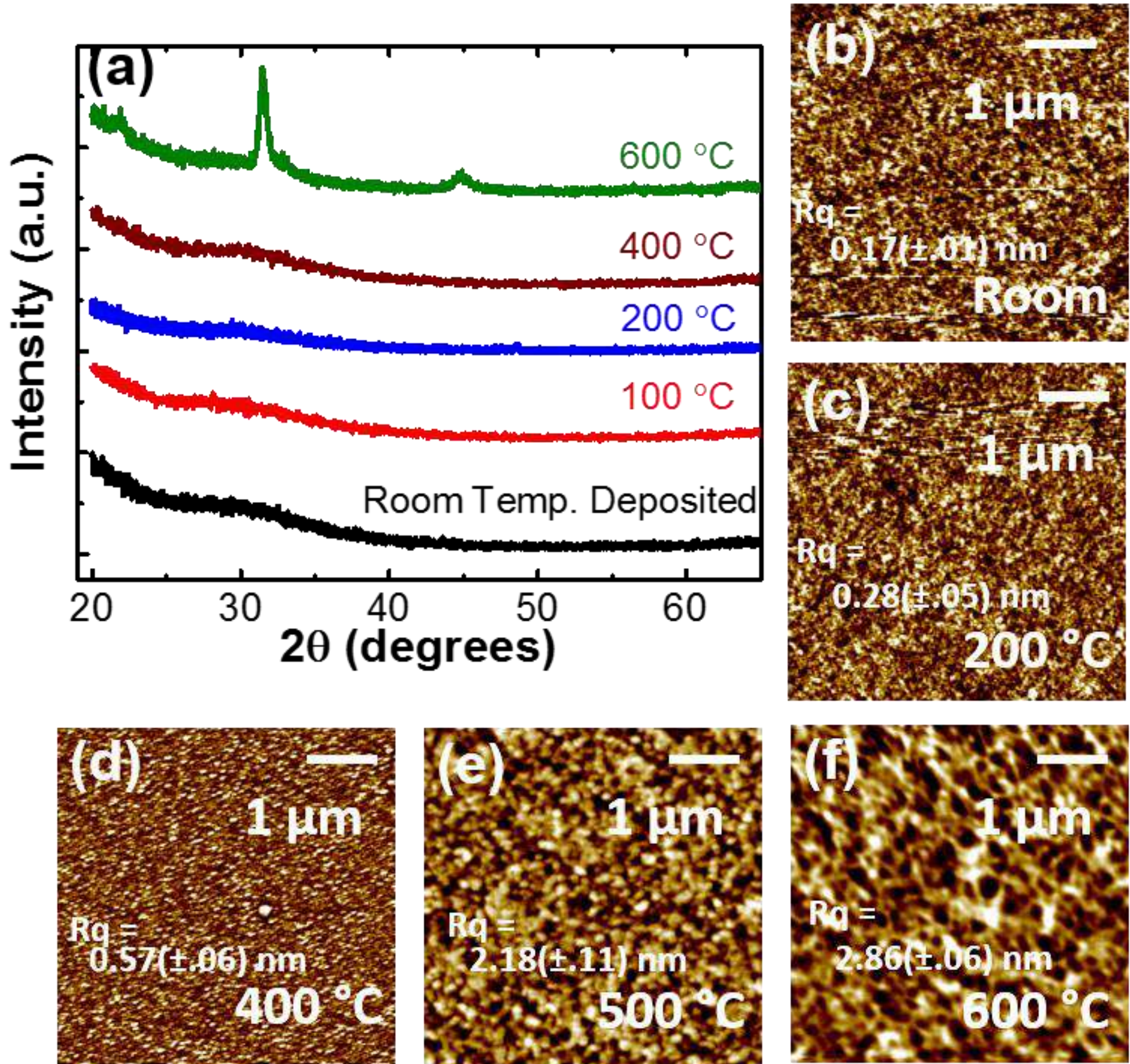

Figure 4.2 : (a) X-ray diffractograms of the BST films grown at different temperatures. Atomic force microscopic images of the BST film grown at (b) R_T (c) 200 °C (d) 400 °C (e) 500 °C and (f) 600 °C.

Figure 4.3 (a) shows the capacitance vs. frequency curve for the BST films deposited with varying deposition temperature, where the frequency was varied from 1 KHz to 1 MHz (Au-BST-n+ silicon structure was used for measurement of the capacitance). No significant variation in capacitance with frequency was observed for the amorphous BST films, however the polycrystalline filmS exhibited a large variation in capacitance in the given frequency range. The overall capacitance for the gate dielectric layer is calculated through (Au-BST-PS-TIPS-pentacene) MIS structure, where PS layer is also considered and the value of capacitance density was found to be 13.33(±2.3) nF/cm^2 and 22.8(±1.38) nF/cm^2 at 1 KHz for RT and 600 °C deposited BST film devices respectively. The value of *k* (dielectric constant) was calculated from the capacitance measurement of the BST film and was found to be 11 and 35 for RT and 600 °C grown BST film respectively. Figure 4.3(b) shows the current density vs. voltage curve for the two types of BST films. The current density was found to be low for both types of BST films and was further reduced in the actual device configuration due to the use of polymer binder in the semiconductor.

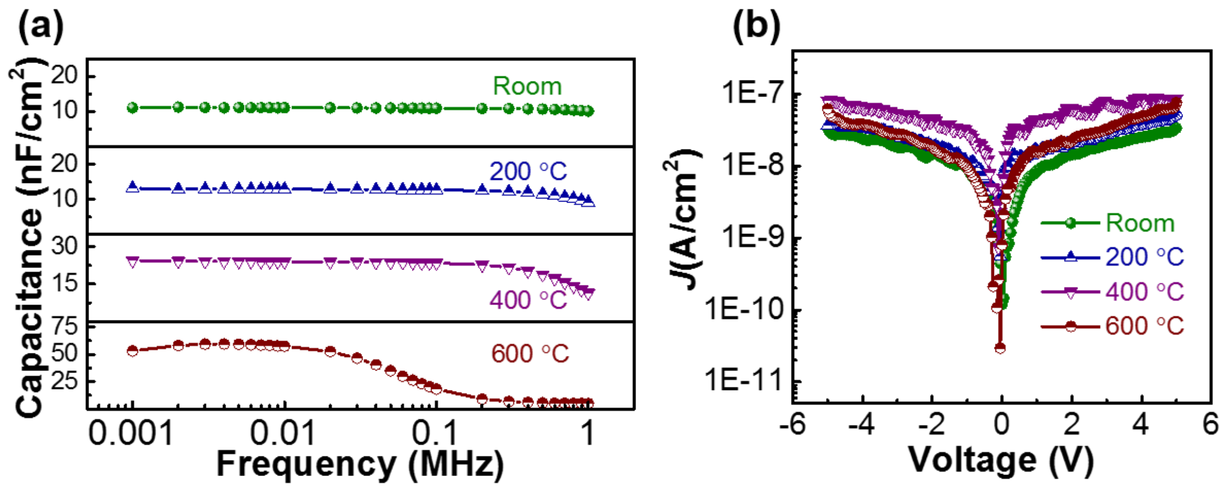

Figure 4.3 : (a) Capacitance - frequency and (b) Current density - Voltage curve for BST films deposited at various temperatures.

4.3.2 Electrical Performance of Rigid OFETs

Figure 4.4 (a-b), (c-d) and (e-f) show the transfer and output characteristics for the thermally grown SiO_2, room temperature deposited BST and 600 °C deposited BST film respectively. As SiO_2 is classically used as the most popular gate dielectric for thin-film transistors because of its chemical stability and smoother surface morphology for transistor fabrication, the electrical characteristics of the BST based transistors are thus compared with SiO_2 based transistors. As seen in the device characteristics and reported by many other researchers, the OFETs with SiO_2 as dielectric will work at a high operating voltage of 30-80 V, because of the low dielectric constant of the SiO_2 [Kim et al.,2008, Giri et al.,2011, He et al.,2012, Huang et al.,2017] This is a major constraint limiting its utilization as a gate dielectric material in portable low power applications. The SiO_2 based OFETs in our study were operated at - 30 V, whereas the same level of drain current in BST based OFETs was achieved at - 5 V operation. The room temperature deposited BST based OFETs have shown excellent p-channel characteristics with the average field-effect mobility (μ_{sat}) of 0.43(±0.05) $cm^2 V^{-1} s^{-1}$ and average threshold voltage (V_{TH}) of -0.54(±0.52) V with on-off current ratio (I_{on}/I_{off}) of ~10^5 while operating at a relatively low voltage of -5 V. On the other hand, the OFETs with 600 °C deposited BST films have shown p-channel characteristics with μ_{sat}, V_{TH} and I_{on}/I_{off} of 0.15(±0.05) $cm^2 V^{-1} s^{-1}$, -0.67(±0.05) V and ~10^3 respectively at an operating voltage of -5 V. The electrical parameter of R_T and 600 °C deposited BST based OFETs are summarized in Table 4.2

Table 4.2 : Summary of electrical parameters extracted from room temperature and 600 °C deposited BST based OFETs.

Deposition Temp.	*Avg. data for*	*Capacitance Density (nF/cm²)*	μ_{sat} (cm^2/Vs)	μ_{max} (cm^2/Vs)	V_{TH} (V)	SS (V/dec.)	D_{it} ($10^{12} cm^{-2} eV^{-1}$)	I_{on}/I_{off}
RT	10 Dev.	13.0 (±2.30)	0.43 (±0.05)	0.51	-0.54 (±0.52)	0.46 (±0.12)	0.6 (±0.8)	~10^5
600 °C	10 Dev.	22.8 (±1.38)	0.15 (±0.05)	0.23	-0.67 (±0.05)	1.40 (±0.30)	3.2 (±0.57)	~10^3

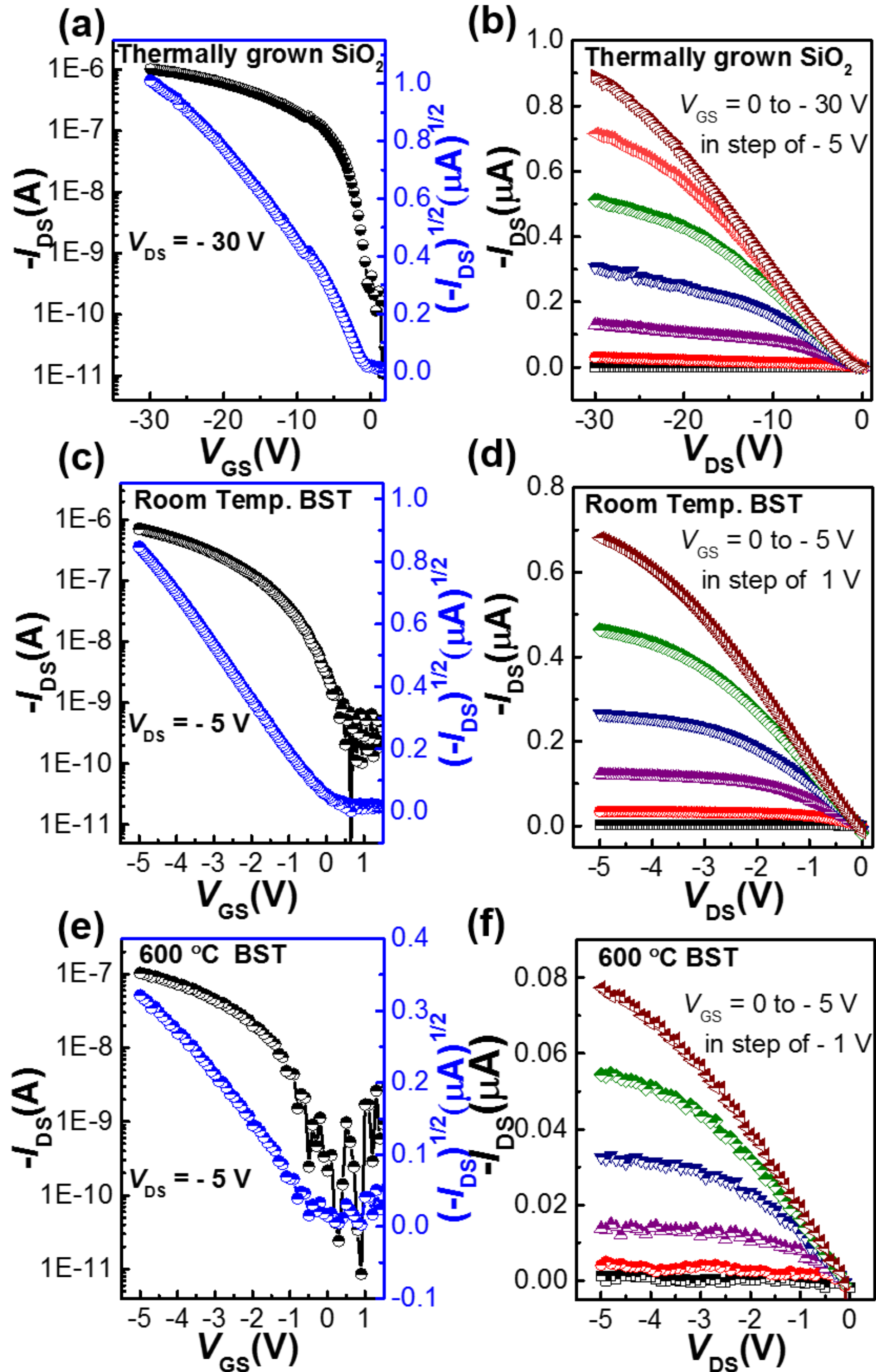

Figure 4.4 : Transfer and output characteristics of OFETs fabricated with (a), (b) 300 nm thermally grown SiO_2, (c), (d) room temperature deposited BST and (e), (f) 600 °C deposited BST film as dielectric.

The high performance of the RT deposited BST based OFETs is primarily attributed to the amorphous nature of the deposited films which have shown smooth surface morphology in the high-*k* dielectric as verified through the XRD and AFM analysis. The smoother surface morphology of the dielectric films provides a suitable surface for active layer deposition and favors the evolution of dielectric: semiconductor interface with fewer traps to have less-hindered charge transportation. The better quality of dielectric: semiconductor interface will result in better performance of the device. In addition, the semiconductor: polymer blend used in the study also favors the development of a smooth dielectric: semiconductor interface and provides high performance in the devices as also discussed in chapter 1. On the other hand, the polycrystalline

BST (600 °C deposited) film has a large number of surface traps because of its higher surface roughness, which degrades the quality of dielectric: semiconductor interface. Charge carriers tend to get trapped in these physical traps and eventually cause the poor electrical performance of the devices as seen through the transfer and output characteristics in Figure 4.4 (e-f). In general, the nature of the dielectric film hugely affects the device performance, as the grain boundaries in the polycrystalline films lead towards high leakage currents, which deteriorates the device performance. In addition, the surface roughness, mechanical and ambient stability of the polycrystalline dielectric films are not desirable for high-performance transistors. On the other hand, the amorphous films are highly stable and their surface properties offer desirable situations for high-performance OFET devices. The observations obtained in our study are in line with the previous studies. The investigation on silicon substrate confirms the suitability of room-temperature deposited BST films for high performance low operating voltage OFET.

4.3.3 Electrical Performance of low-voltage Flexible OFETs

To confirm the utility of the room temperature grown BST film in flexible devices, the amorphous BST film was deposited on ITO coated PET substrate. To maintain the substrate integrity, BST films on PET were deposited at room temperature. The deposition parameters are similar as deposited on the silicon substrate at room temperature. The thickness of BST film was measured to be 70 nm. Figure 4.5 (a) and (b) show the current density and capacitance vs. frequency (*C-f*) curves for the BST dielectric film on the flexible substrate. These characteristics were measured separately from Au/BST/ITO devices. The observations for the BST film on a flexible substrate were found to be similar to those recorded for the BST film on the silicon substrate. The variation in capacitance in a frequency range from 1 kHz to 1 MHz was insignificant and the leakage current density was found to be small.

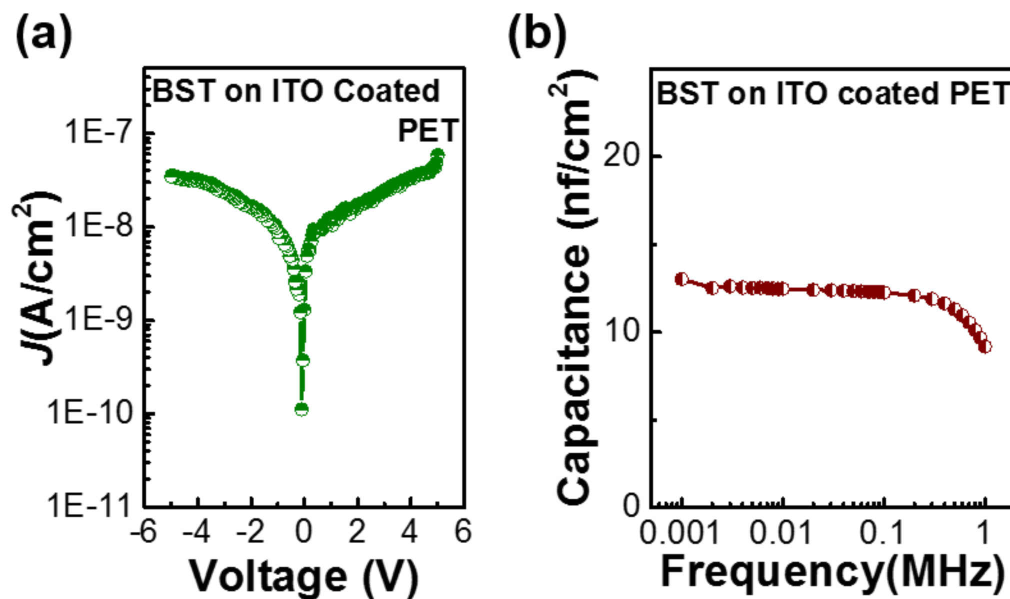

Figure 4.5 : (a) *J-V* and (b) *C-f* characteristics of room-temperature deposited BST films on flexible PET substrate.

The device schematic and digital image of the flexible OFETs are shown in Figure 4.1(b) and 4.1 (f) respectively. Figure 4.6 (a) shows the AFM image of the TIPS-pentacene crystal deposited over BST film. As expected the general terracing structure of TIPS-Pentcacene crystals was observed similar to various previous reports [Li et al.,2012, Diao et al.,2013, Bharti et al.,2016]. Figure 4.6 (b) shows the XRD spectra of the deposited TIPS-pentacene film and was found to have a high degree of crystallinity.

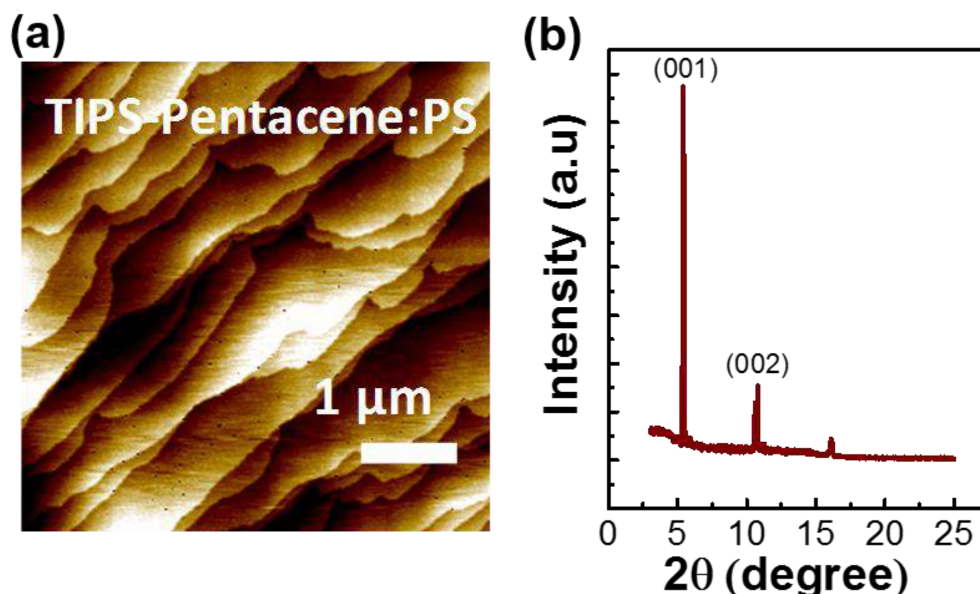

Figure 4.6 : (a) AFM image showing terracing structure, and (b) X-ray diffractogram of TIPS-pentacene crystals deposited over the amorphous BST layer.

Figure 4.7 (a) and (b) show the transfer and output characteristics of the fabricated flexible device with RT-deposited BST as gate dielectric and TIPS-Pentcane: PS blend as an active layer. The devices have shown excellent p-channel electrical characteristics with average (μ_{avg}) and maximum field-effect mobility (μ_{max}) of 0.56(±0.20) $cm^2 V^{-1} s^{-1}$ and 1.01 $cm^2 V^{-1} s^{-1}$ respectively with V_{TH} of -0.90(±0.59) V and I_{on}/I_{off} of ~10^5 while operating at -5 V. Performance of amorphous BST based OFETs was found to be comparable to various recently reported flexible low voltage OFETs. As the BST film was deposited at room temperature and no annealing process was used in the complete fabrication process, the substrates don't get affected by any annealing process and there is no heat-induced strain on the substrate. The high performance in these OFETs is due to earlier discussed reasons for the utilization of high-*k* dielectric, smoother morphology of the RT grown BST films and an even dielectric: semiconductor interface developed between semiconductor and polymer binder.

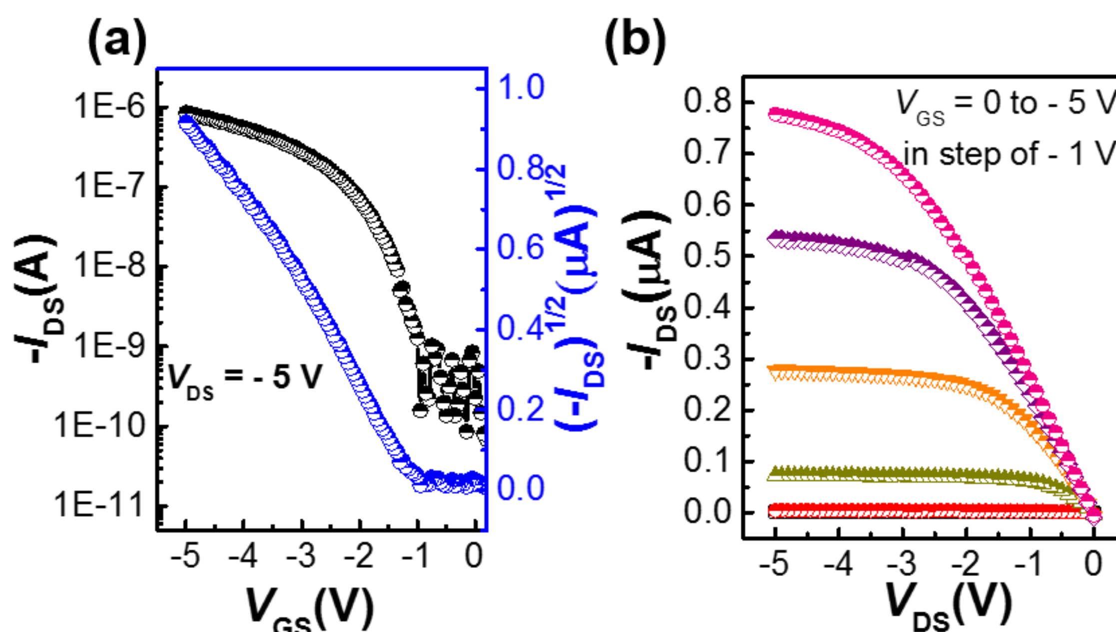

Figure 4.7 : **(a)** Transfer and **(b)** output characteristics of the flexible OFETs.

To test the operational stability of these flexible devices the transfer characteristics were continuously measured 500 times as shown in Figure 4.8. The recorded results reveal that the transfer characteristics were found to be almost overlapping even after the 500th transfer cycle. There is very little performance spread with ΔI_{DS} of 4 nA and $|\Delta V_{TH}|$ of 0.05 V. Such high operational stability implies very less interfacial traps due to high-quality dielectric: semiconductor interface as discussed earlier.

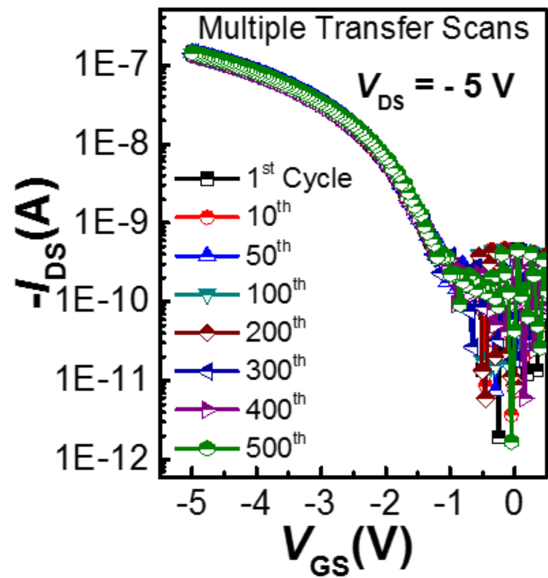

Figure 4.8 : Representation of flexible device operational stability with 500 continuous multiple transfer scans.

4.3.4 Electromechanical Stability of Flexible OFETs

To explore the utilization of these flexible devices in practical applications, variation in electrical parameters with strain needs to be investigated. In this study, the devices were characterized in pristine case (no strain) and then with increasing strain, the electrical characteristics were recorded. Figure 4.9 (a) shows the transfer characteristics of the flexible devices with increasing strain. The strain is calculated using Eq. (2.8).

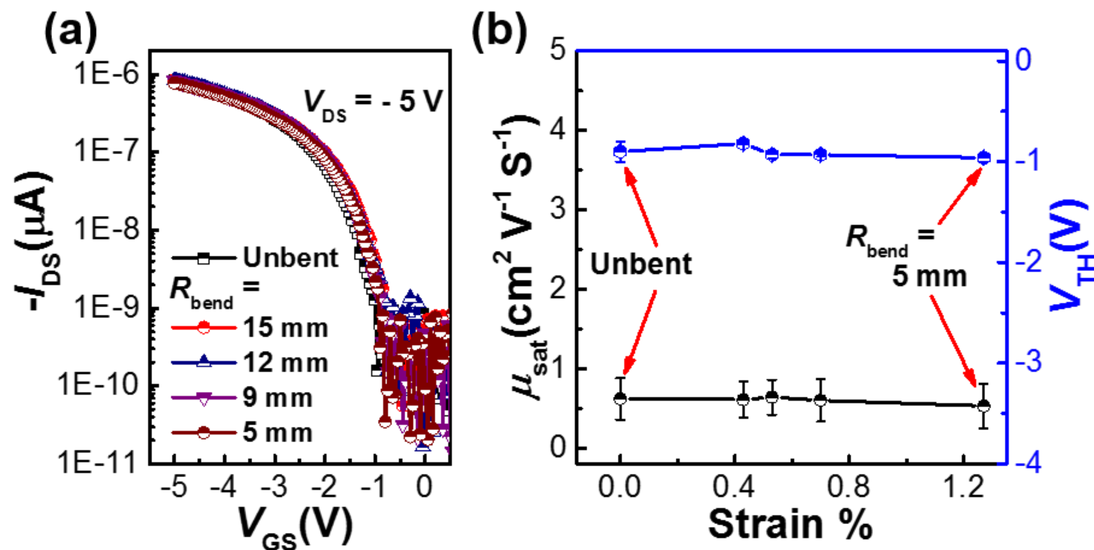

Figure 4.9 : (a) Transfer characteristics, (b) extracted mobility and the threshold voltage of the flexible OFETs with varying bending radius.

The devices were given a maximum strain of 1.27 % corresponding to R_{bend} of 5 mm in this study. With increasing strain, there is very little change in electrical parameters. The maximum drain current (I_{Don}) has reduced by 7.7 % after 1.27 % strain. The variation in mobility and threshold voltage with increasing strain is shown in Figure 4.9 (b). The variation in mobility ($\Delta\mu_{sat}$) and threshold voltage (ΔV_{TH}) was not severe and found to be 0.09 $cm^2 V^{-1} s^{-1}$ and 0.06 V respectively even after bending the devices to a radius as small as 5 mm. These small changes in the electrical parameter are due to the rupture of the semiconductor crystals and generation and propagation of microcracks/defects in the semiconductor crystals with increasing strain. Further, in continuation of the bending test, the bias stress-induced effects in the device were tested with and without the application of strain. In this test, the devices were subjected to the maximum potential of $V_{DS} = V_{GS}$ = -5 V and the variation in normalized drain current was recorded before and after application of strain, which is shown in Figure 4.10 (a).

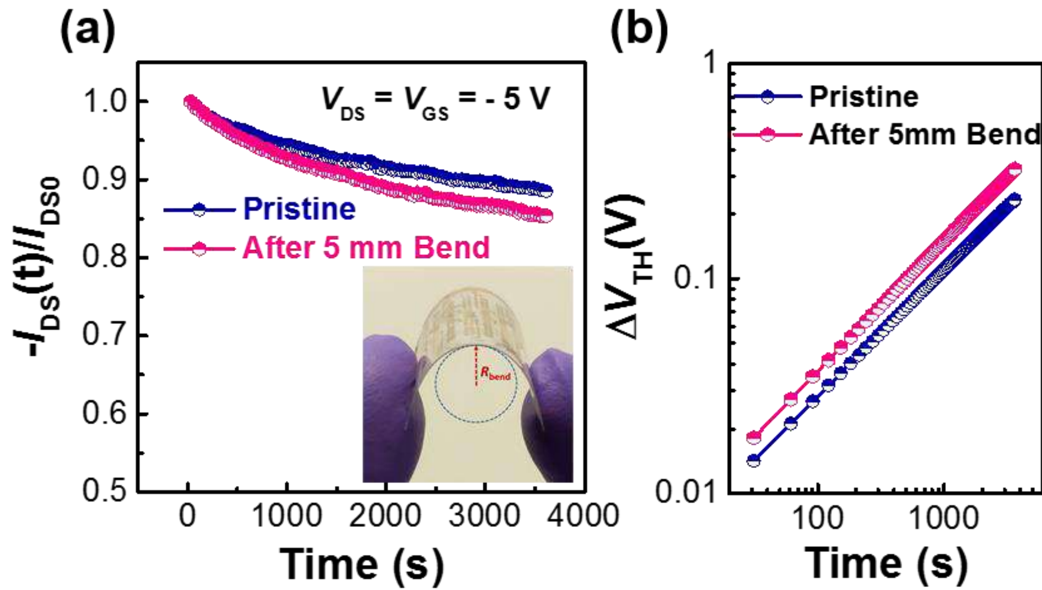

Figure 4.10 : (a) Normalized drain current decay and (b) shift in threshold voltage of the device, induced due to bias stress for pristine and after bending the devices to 5 mm radius.

In the pristine situation when the bias stress has applied the trapping of charge carriers takes place in various regions of the semiconductor mainly at the dielectric: semiconductor interface, which leads to shifting in threshold voltage and thus the drain current decays with time. For the flexible BST based devices in pristine situation, a decay of 11 % was found in drain current after bias stress application for 1 hour. The low value of drain current decay further confirms the lesser trapping sites at the interface. When a similar bias stress test was performed after applying 1.27 % strain (R_{bend} = 5 mm), a decay of 14 % in the normalized drain current was observed. The slight increase in decay due to bending is possible because of the generation and propagation of micro defects in the semiconducting crystals. The width of trap distribution which is identified by the temperature-dependent dispersion parameter β and the relaxation time τ was calculated by fitting the experimental data in Eq. (2.6). The values of τ and β were found to be 3.8×10^5 s and 0.59 for pristine, and 2.1×10^5 s and 0.61 for the devices stressed after the bent. The high value of τ for both the pristine and strained case indicates lesser trapping sites in the BST based flexible OFETs due to various reasons discussed previously. The shift in threshold voltage due to bias stress effect is given mathematically by Eq. (2.7) and extracted values of τ and β were used to find the threshold voltage shift and the results are shown in Figure 4.10 (b). The obtained shift in threshold voltage is very small and was found to be 0.21 and 0.31 V, after the application of bias stress for the pristine and stained situation respectively. A little high shift in strained devices is perhaps because of the extra defect generated due to bending.

To determine the extent of tolerable bending, devices were later bent at radius of 2 mm, which led to severe degradation in performance (even device failure in some cases). To examine the possible causes, microscopic images of the device surface were captured. After undergoing strain at a 2 mm radius, the gold S/D contacts lose their uniformity and appear to peel-off as shown in Figure 4.11, which may be due to cracks developed in the crystals underneath, leading to deteriorated device performance. These observations suggest that under tolerable bending conditions, uniformity of dielectric: OSC interface remains intact, imparting high electromechanical stability to devices. Under extreme bending situations, device performance is degraded due to deteriorated uniformity of this interface due to crystal rupture not due to uniformity degradation in the dielectric layer.

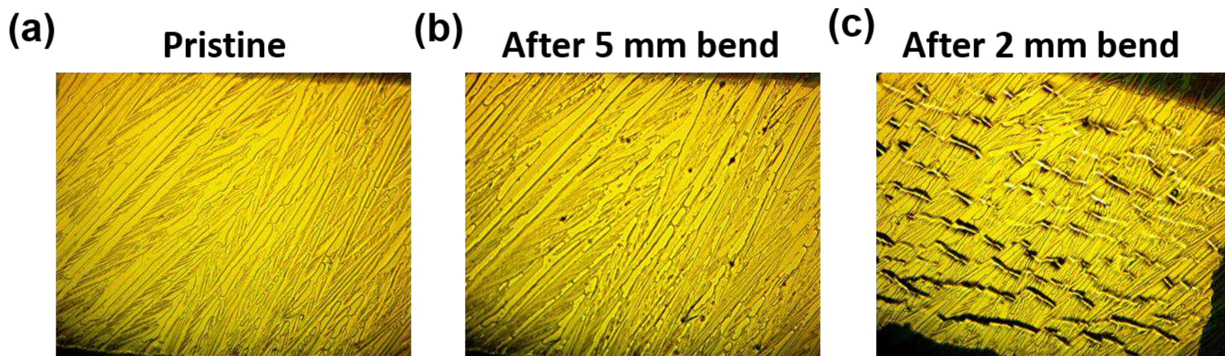

Figure 4.11 : Optical Microscope image of the top view of the device for (a) Pristine, after (b) 5 mm and (c) 2 mm bending showing developed cracks at lower bending radii.

Further to take the mechanical stability test to more pronounced level, the devices were subjected to multiple strain cycle comprises of compressive and tensile strain, each cycle consists of upward and downward bending to 1.27 % (R_{bend} = ±5 mm). The illustration of the bending cycle is shown in Figure 4.12.

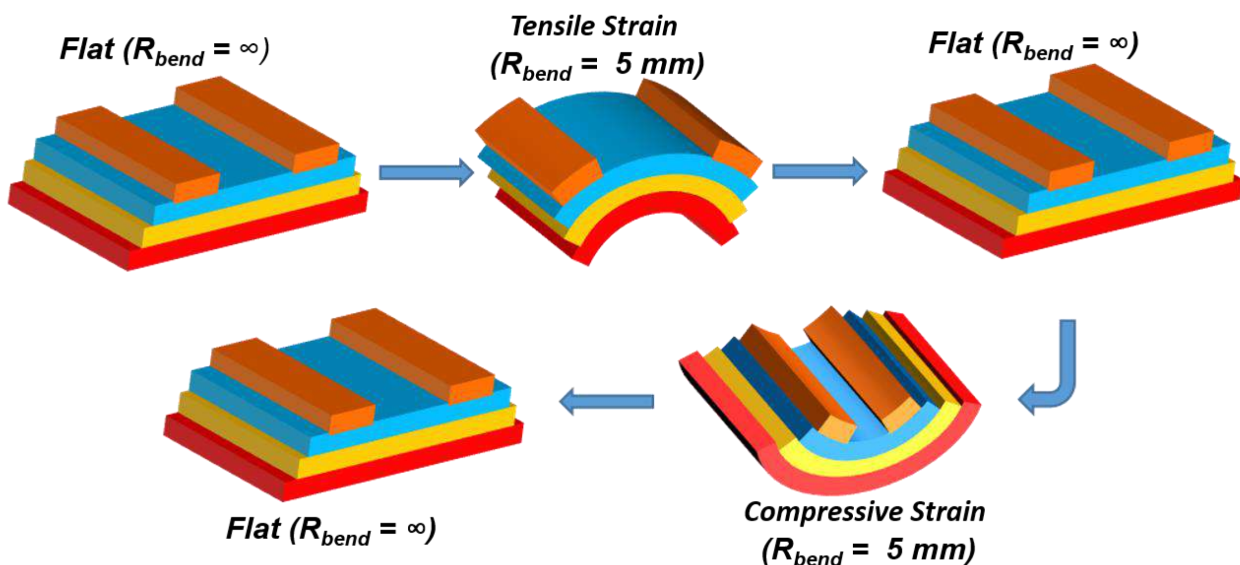

Figure 4.12 : Illustration of a single bending cycle for mechanical stress test comprising of tensile and compressive strain.

By fixing the radius to 5 mm, the devices were subjected to strain cycles as high as 500 cycles and the transfer characteristics were recorded periodically. Figure 4.13 (a) shows the effect of multiple bend cycles on the transfer characteristics and Figure 4.13 (b) shows the effect of strain

cycles on the mobility and threshold voltage. The electrical parameters were found to have very small deterioration due to the combined effect of a large number of compressive and tensile strain cycles as high as 500 cycles. The outcomes observed indicate the stable nature of amorphous BST based OFET devices and found them suitable for flexible foldable devices.

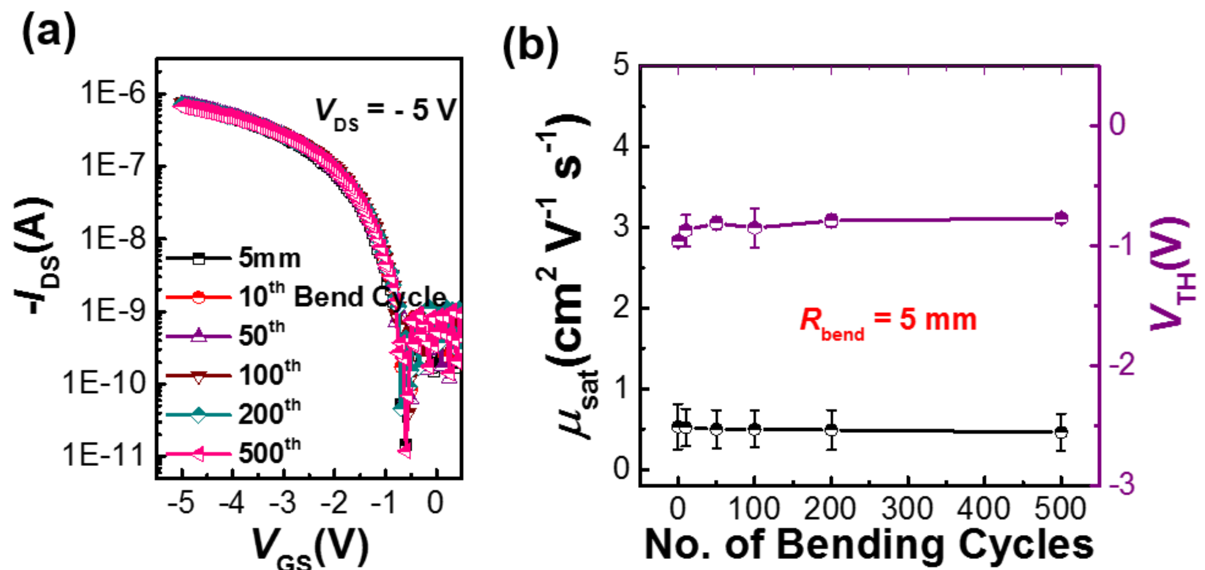

Figure 4.13 : (a) Transfer characteristics and (b) variation in mobility and threshold voltage with an increasing number of bending cycles.

In addition, to test the long-term bending stability of these OFETs the devices were strained to 1.27 % strain for a duration of 5 min to 1 month and the transfer characteristics were analyzed. Figure 4.14 shows the effect of long-term bending on the transfer characteristics of the flexible devices. A slight deterioration in the device performance can be noticed which can be due to cracks developed in semiconducting crystals and/or degraded uniformity at semiconductor: polymer and metal: semiconductor interfaces.

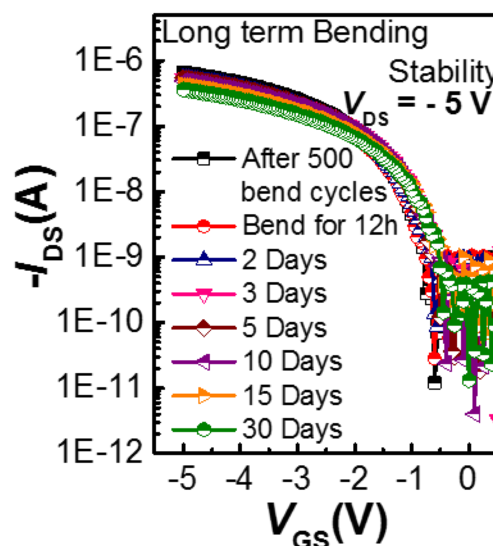

Figure 4.14 : Variation in transfer characteristics with increasing bending duration showing long term bending stability in flexible OFETs.

In the flexibility studies of OFETs there found a very minuscule change in the device parameters. To confirm the fact whether the BST film has any contribution or not towards the small

degradation of the OFETs performance with bending, it is highly essential to investigate the electromechanical stability of these films individually on flexible substrates. In this test, Au/BST/ITO-PET structure was subjected to the varying degree of tensile strain and measurements were recorded. Figure 4.15 (a) shows the capacitance vs. frequency curve of BST film at different bending radii from pristine case to 5 mm radius. Figure 4.15 (b) shows the capacitance vs. frequency curve of the structure after several bending cycles as illustrated in Figure 4.12. These results suggest that the capacitance is relatively independent of strain and its repeated cycles in the measured frequency range. The invariant nature of capacitance of the BST film also testifies that the small changes in mobility or threshold voltage of the flexible BST OFETs under mechanical strain are not due to capacitance changes of the dielectric layer, but are due to the generation and propagation of microcracks/defects in the semiconductor crystals with increasing strain. With various observations related to performance and stability of the amorphous BST based flexible OFETs, it can be asserted that the combination of several highly desired attributes such as room temperature deposition, high dielectric constant, smooth surface morphology and stable nature under severe bending situations certainly make the amorphous BST layer as one of the promising candidate as a dielectric for low cost, low voltage operating flexible OFETs.

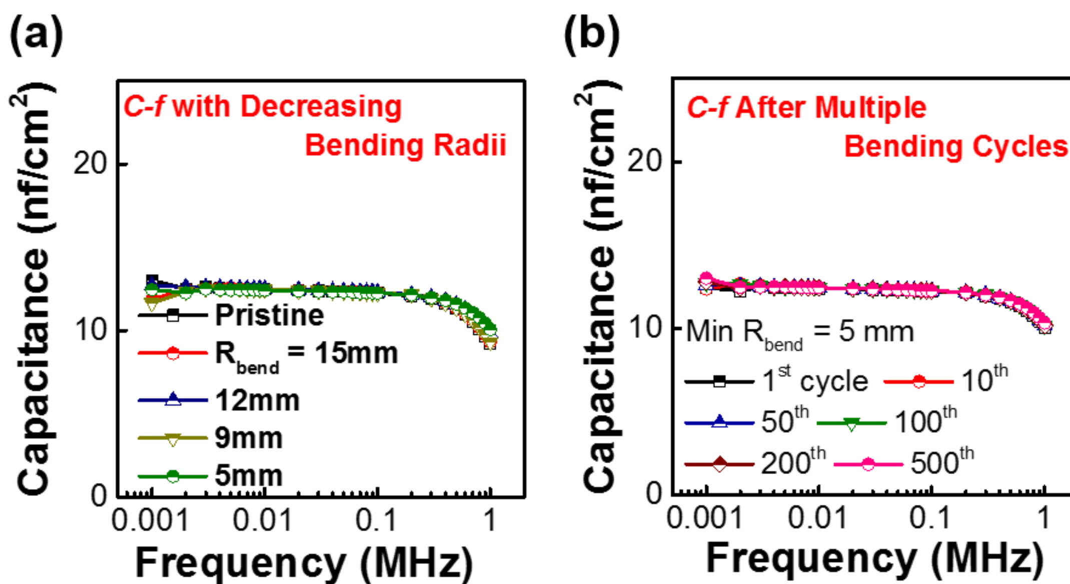

Figure 4.15 : *C-f* measurement of the BST film with (a) varying bending radius and (b) increasing number of bending cycles.

4.4 CONCLUSION

In conclusion, the use of room temperature RF sputtered BST film as a dielectric layer in high-performance low voltage operated flexible OFETs is demonstrated in this chapter. The BST film was found to be amorphous with smooth surface morphology. The flexible OFETs with the aforementioned BST film as gate dielectric and TIPS-pentacene: PS blend as active layer have shown μ_{max} of 1.01 $cm^2 V^{-1} s^{-1}$ with near-zero V_{TH} and I_{on}/I_{off} of ~10^5 at -5 V operation. The devices have shown high mechanical stability when gone through series of bending tests. Electrical parameters were found to be negligibly affected even when the devices were strained to a radius as low as 5 mm. The electrical stability under a large number of compressive and tensile strain cycles have shown their potential to be used in low voltage bendable flexible electronics applications. In addition, the long-term bending stability was demonstrated by capturing the electrical performance of devices strained at 5 mm bending radius for a duration of 1 month.

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