Chapter 2

RESISTIVE RANDOM ACCESS MEMORIES

As discussed in the previous chapter, the comparison among the various non-volatile memory (NVM) technology confirmed that the RRAM has emerged as a game changer owing to its scalability, low power consumption, facile structure, and easy integration with the complementary metal-oxide semiconductor (CMOS) technology. This chapter talks about the in-depth analysis of working principle, type of resistive switching, various performance parameters, and the state-of-the-art status of the RRAM technology.

2.1 RESISTIVE SWITCHING AND RRAM

2.1.1 Resistive Switching Phenomenon & its Types

As stated earlier, the resistive switching refers to the change in resistance due to the formation or rupture of a conductive path in the dielectric material, sandwiched between the two electrodes in a metal-insulator-metal structure. The formation and rupture of CF switch the memory cell between the HRS and the LRS, respectively. Figure 2.1 demonstrates the schematic of the programming sequence of RRAM cells starting from forming, set, and then reset the process. Unlike permanent/hard dielectric breakdown, which is an irreversible phenomenon, resistive switching offers a soft breakdown that is reversible and can be repeated multiple times. The reversible change in the resistance state is non-volatile and can be maintained even after the external electric field is removed. This phenomenon is exhibited by a specific class of dielectric and semiconducting materials such as metal oxides, nitrides, perovskites, organic polymers, and chalcogenides.

The resistive switching phenomena was first detected by Hickmott et al. in 1962 in aluminum oxide insulating layer sandwiched between Au and Al electrodes [Hickmott, 1962]. These devices showed an exponential rise in current up to a voltage and with further increment in voltage, a sharp fall in resistance, which is termed as negative differential resistance or resistive switching [Hiatt and Hickmott, 1965]. Later in the 1960s and 1980s, more research articles and review papers were publishes exploring the resistive switching and non-volatile memory capabilities of metal oxides [Hirose and Hirose, 1976; Ovshinsky, 1968]. Due to the lack of experimental techniques that could have produced the evidential proves of physics behind the resistive switching and the related phenomena, the pace of research in these devices slowed down. At the same time, Silicon-based electronics gained a lot more attention, and hence the application part of resistive switching in metal oxides was ignored. However, the research and development of the process for high-quality oxide thin film growth was in high demand for metal-oxide-semiconductor (MOS) devices. Moreover, major microscopic and spectroscopic techniques for film and material characterization were also in their advanced stages. As predicted by Gordon Moore in 1965, the number of transistors on a chip will double every 18 months [Moore, 2006]. Since the 1980s, the primary focus was shifted to MOS devices and their scaling for high packaging density, high functionality, and less power consumption. The aggressive

scaling of MOS devices resulted in the feature size reduced to about 100 nm by the early 2000s that promoted severe concern regarding the physical limitations of these devices and evolving issues as after-effects [Hokazono *et al.*, 2000]. This causes the demand in the scientific research community for shifting the focus from MOS devices that demands the search for alternative materials and devices structures for future large-area electronic application, in particular the non-volatile memories.

In early 2000, the research focus got shifted to resistive switching devices with some impressive results produced by Wanatnabe et al. and Ignatiev et al. on Cr-doped $SrZrO_3$ and $Pr_{0.7}Ca_{0.3}MnO_3$ respectively [Liu *et al.*, 2000; Watanabe, 2001]. During the period from the 1960s to 2000, the development of analytical tools played an essential role in understanding the physics and mechanism of resistive switching phenomena, especially the formation and rupture of CF and corresponding changes at the bulk level [Yang and Huang, 2018]. Since then, the application of resistive switching devices in the development of non-volatile memories has gained significant attention, and the prime focus remains the search for a high-quality switching layer and switching layer-electrode combination [Zahoor *et al.*, 2020].

Figure 2.1 demonstrates the various steps involved in the switching mechanism of a typical bipolar RRAM device. Initially, the as-fabricated device will behave as an insulator (high resistance or HRS), and triggering is required to initiate the switching process in the devices. Once the forming process is completed, the device switches to LRS with the evolution of CF between the top and the BE. Forming free RRAM devices is highly desirable as it reduces one step from the operation sequence and requirement for high voltage application. Forming is a soft breakdown process where the current density and electric field intensity are controlled by external current compliance. Compliance current that is imposed through a transistor avoids permanent breakdown in the device. The application of compliance current is a useful technique to regulate the CF dimension that eventually improves the device's lifetime and reliability. As the device is in its initial state, the forming voltage is generally higher than the set and reset voltages. Forming voltage depends on many factors, such as switching layer thickness, film quality, characterization environment, and electrode material [Yu *et al.*, 2012].

Once the device is formed and is in LRS, the dissolution of CF is required to switch the device back to HRS and to begin the normal working of a memory cell. The process of switching the device from LRS to HRS due to partial dissolution of CF is termed as reset process or "ERASE" (storage of '0' bit). There are multiple mechanisms proposed and investigated to understand the physical events that occurred during the reset process. Some primary mechanisms are migration of electrochemically active metal atoms such as Ag and Cu (CBRAM), thermal dissolution of CF due to extremely high current density in the nanosized filament (unipolar switching), and fracture in CF formed due to oxygen vacancy migration (VCRAM) [Bocquet *et al.*, 2014; Valov and Kozicki, 2013]. The reset event is a stochastic process due to the incomplete breakage of filament in every cycle. Some residual CF remains in the switching layer that later results in severe reliability issues such as higher leakage current that affects the memory window and poor cycle to cycle and device to device variability, which is one of the significant issues in RRAM technology [Govoreanu *et al.*, 2011].

In the subsequent cycles, the device switches between the HRS and LRS due to repeatable reset and set processes, respectively. Unlike the forming process that switches the fresh device to LRS, the set process occurs due to the repeatable formation of CF after every device reset, and this process is also termed as the "WRITE" process (storage of '1' bit). The set voltage is generally higher than the forming voltage due to the CF length reduction in the switching layer due to residual filament after every reset. The mechanism behind the set process is attributed to the formation of the CF by the migration of electrochemically active metals such as Ag or Cu (CBRAM), the oxidation and reduction of oxide switching layer resulted in the formation of oxygen ions and oxygen vacancies (VCRAM), charge trap and detrap, and conformal changes in the switching layers in case of organic materials or polymer dielectrics [Lee *et al.*, 2015].

The two widely discussed resistive switching mechanisms and that are scientifically proved are redox-based switching in oxide materials for VCRAM and migration of metal ions in the case of CBRAM. The techniques involved in ex situ probing of resistive switching mechanisms

include current-voltage characteristics, capacitance-voltage characteristics, cyclic voltammetry, noise measurement, and impedance spectroscopy [Kozicki and Barnaby, 2016]. However, the complete investigation and understanding of complex dynamics of the set and reset process in both the VCRAM and CBRAM is highly challenging and unreliable when examined using the ex-situ characterization technique. In contrast, with the development of high-resolution microscopy and spectroscopy techniques, the real-time examination of switching dynamics can be performed using in-situ techniques more accurately and precisely and hence has gained significant attention

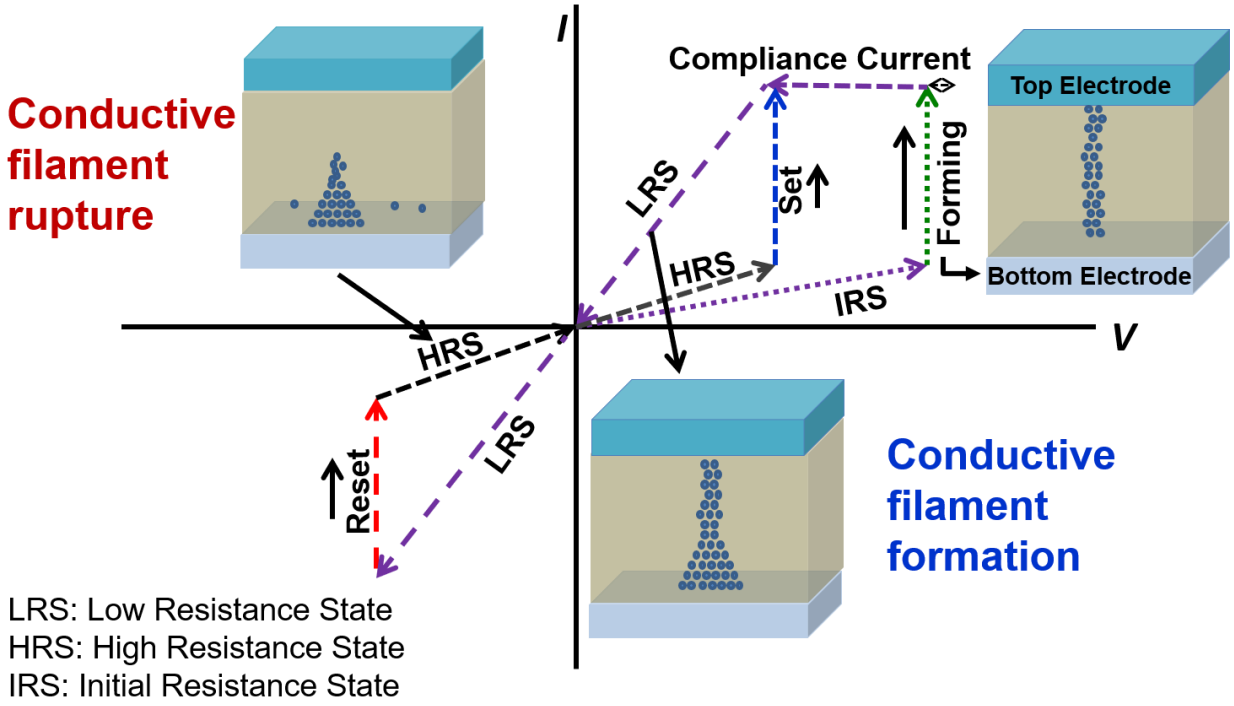

Figure 2.1: Schematic demonstrating the resistive switching mechanism with the demonstration of forming, set, and reset processes in a typical bipolar RRAM cell.

in recent times [Chiu *et al.*, 2017]. This in situ observation of the switching process requires to bring the nanoscale characterization and electrical measurement set up in a standard experimental unit at the same time, which requires highly sophisticated instruments and precise sample preparation. Some of the popular in situ characterization techniques include cross-sectional high-resolution transmission electron microscopy (X-HRTEM) and elemental mapping, X-ray photoelectron spectroscopy (XPS), conductive atomic force microscopy (CAFM), electron energy loss spectroscopy (EELS) mapping, X-ray absorption spectromicroscopy, and thermoreflectance [Liu *et al.*, 2012; Park *et al.*, 2013; Yang *et al.*, 2017; Yao *et al.*, 2012].

2.1.1.1 Unipolar Resistive Switching

As mentioned earlier, the resistive switching is termed as of unipolar type when the set and reset occurs at the same polarity of applied bias. It means that if the set process has occurred at the positive set voltage, then the reset process will also be executed at the positive reset voltage; hence it will be termed as positive unipolar switching [Lin and Lin, 2016]. The same will happen if the set and reset processes are happening on the negative bias potential and that switching will be termed as negative unipolar switching. Figure 2.2 has demonstrated the execution of positive and negative unipolar resistive switching process. The compliance current is imposed for the set process to avoid permanent breakdown of the devices, whereas the reset current is generally higher during the reset process, therefore the reset process is left compliance free [Yanagida *et al.*, 2013].

The unipolar resistive switching characteristics are majorly observed in metal-oxide based dielectrics such as HfO_x, TaO_x, TiO_x, AlO_x, ZnO, and NbO_x [Deswal *et al.*, 2018; Maestro-Izquierdo

et al., 2020; Park *et al.*, 2016; Sahu *et al.*, 2018; Xu *et al.*, 2016]. Sometimes, the tuning of compliance current and applied bias has resulted in the observation of both the unipolar and bipolar resistive switching characteristics in the device [Sun *et al.*, 2011]. The unipolar resistive switching behavior of an RRAM device is primarily controlled by the pair of top and BEs. Many reports suggested the occurrence of unipolar switching when both the top and BEs are either of the same material or the both are inert metals having the least oxidation or reduction tendency. While the set process for unipolar switching is governed by the attraction of oxygen vacancies in the CF due to the Soret forces, the reset process is typically a joule heating assisted thermal dissolution of CF where the Fick forces govern repulsion of oxygen vacancies from the CF, respectively. As the joule heating is independent of the electric field direction, the reset process is a polarity independent event [Lee *et al.*, 2015]. Moreover, when the electric field starts to dominate the joule heating effect, the ionic motion becomes more affected by the bias polarity that may lead to bipolar resistive switching.

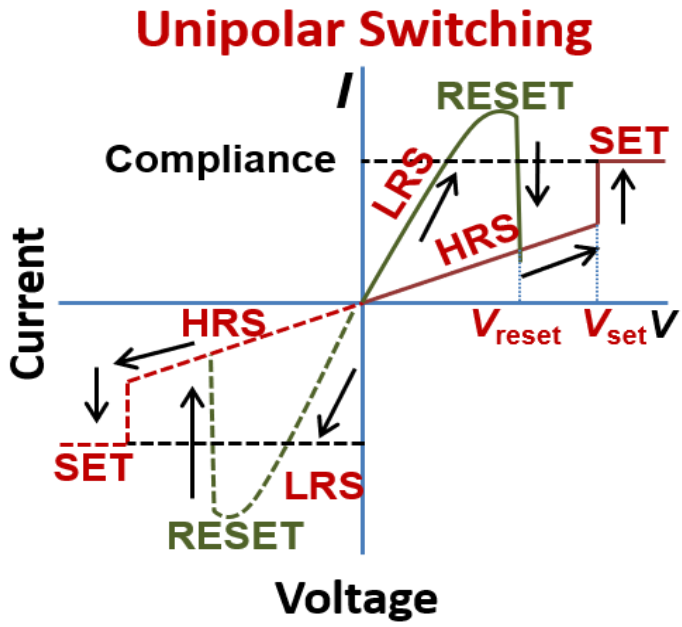

Figure 2.2: Schematic demonstration of unipolar resistive switching using device *I-V* characteristics.

2.1.1.2 Bipolar Resistive Switching

Contrary to the unipolar resistive switching, bipolar resistive switching takes place when the set and reset processes occur on the opposite polarity of applied bias. If the set process is happening on the positive bias, then the reset process will happen at the negative bias (figure-of-eight, F8) and vice-versa (counter-figure-of-eight, cF8). Figure 2.3(a) and (b). demonstrates the bipolar resistive switching using a schematic *I-V* curve in F8 and cF8 modes, respectively. As the sudden rise in current at set voltage (V_{set}) indicates the occurrence of set process where the device displays the transition from HRS to LRS, whereas the sudden fall in the current at reset voltage (V_{reset}) corresponds to the reset process that switches the device back to HRS. For an F8 type of switching, the set process occurs at the positive voltage and reset on the negative voltage whereas, the cF8 bipolar switching requires the set process to be executed on the negative polarity of bias and reset on the opposite polarity. As mentioned above, a compliance current limit is a must in both types to avoid a permanent breakdown during the set process. The two major mechanisms that govern the switching process in bipolar RRAMs are charge trapping/de-trapping and oxygen vacancy migration. Many commonly explored metal oxides such as TiO_x, HfO_x, TaO_x, AlO_x, $BaTiO_3$, and graphene oxide (GO) have demonstrated the F8 bipolar resistive switching, while WO_x, PCMO, and Nb-doped $SrTiO_3$ have displayed both or interchangeability between the F8 and cF8 bipolar resistive switching. The interchangeability between the two is generally a TE dependent phenomenon, and it has been largely observed that the formation of a very thin oxide

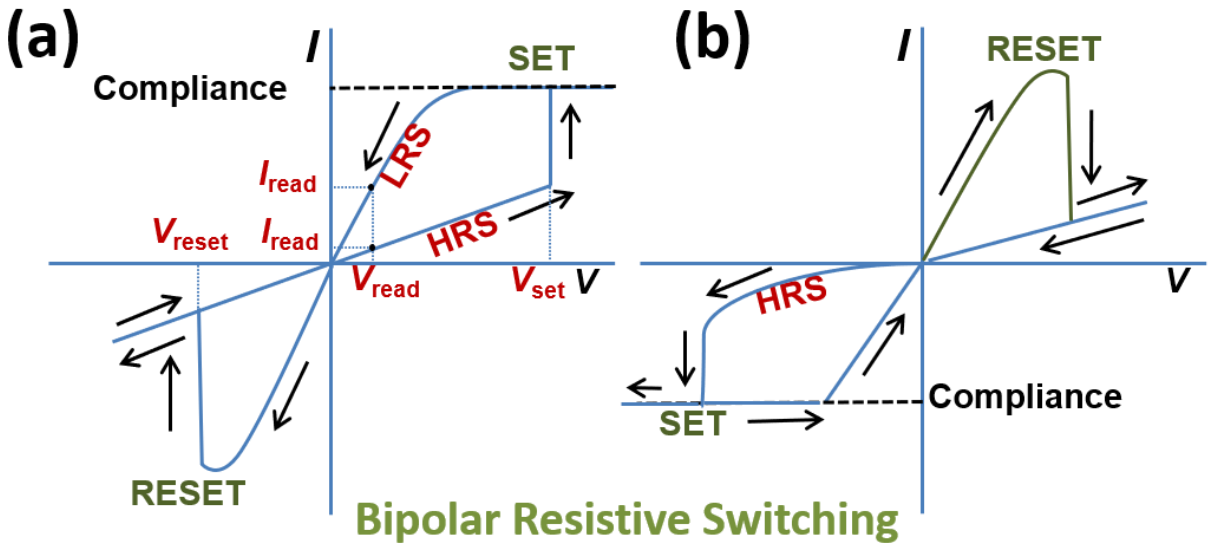

Figure 2.3: Typical *I-V* characteristics of Bipolar resistive switching characteristics in F8 **(a)**, and cF8 modes **(b)**.

film at the active TE material at the TE-metal oxide interface governs the cF8 type of switching. The F8 type of bipolar resistive switching is broadly desired for memory applications that offer a reliable and stable resistive switching with a larger memory window and lower power consumption [Li *et al.*, 2018].

2.1.1.3 Threshold Switching

Threshold switching is also an electrical characteristic of metal-insulator-metal structures; however, unlike unipolar and bipolar resistive switching devices, threshold switches are mostly volatile. Apart from memory switching, the threshold switches find their application not limited to research areas such as the selector devices for crossbar 3-dimensional architectures and neurons for neuromorphic computing. Figure 2.4 shows the typical *I-V* characteristics of a threshold switch, demonstrating the positive and negative threshold switching. Depending upon the device structure and characterization parameters, the devices may exhibit either negative or positive or both negative and positive threshold switching. In a threshold switch, the LRS is maintained for a short voltage range termed as threshold voltage V_T. The compliance current is imposed to control the peak current flowing through the device, and hence the permanent breakdown can be avoided. Unlike resistive switching, threshold switches hold the LRS when voltage is swept back to zero, and transition from LRS to HRS occurs hold voltage V_H. Thus, a threshold switching device has a single stable state, i.e., the HRS, where the read operation can

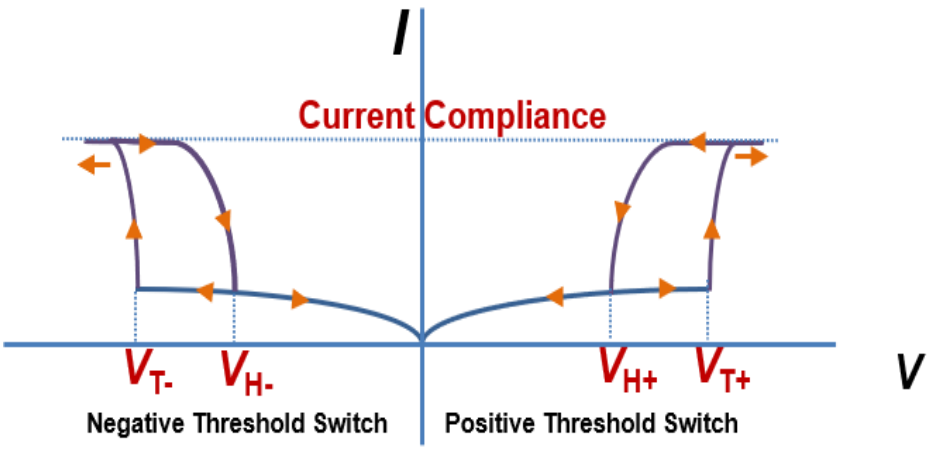

Figure 2.4: Switching behavior of a threshold switch demonstrated using typical *I-V* characteristics indicating the positive and negative threshold switching and threshold voltage V_T and the hold voltage V_T.

be performed, whereas the LRS is stable only during the voltage range between V_H and V_T [Wang *et al.*, 2018b].

2.2 Valance Change RRAM (VCRAM)

The RRAMs can be categorized further on the basis of their working principle into Valance change RRAM (VCRAM), Conductive bridge RRAM (CBRAM), Thermochemical memories (TCM). These devices may be found with many other names in literature such as electrochemical metallization memory (ECM), Oxide RRAM (OxRAM), atomic switches, programmable metallization cells (PMC), and memristor.

The preliminary research on the RRAM devices using the metal oxides was performed as the VCRAM devices. The reduction-oxidation (redox) reactions in transition metal oxides takes place when a strong electric field is applied across the two terminals of device governs the movement of ions in VCRAM. The VCRAM device structure comprises of an easily oxidizable ohmic TE such as Ta, Hf and Ti, whereas the inert Schottky electrode such as Pt, Ir or other high work function materials are employed as the BE. Symmetric structures with the same top and BEs are also often reported. During the electroforming process, the soft breakdown of pristine metal-oxide generates the negatively charged oxygen ions O^{2-} and positively charges oxygen vacancies $V_o^{\cdot\cdot}$. The evolution of O^{2-} and $V_o^{\cdot\cdot}$ inside the metal oxide bulk, causes a change in valance state of the transition metal cation (M^{n+}) that affects the electrical conductance of the switching layer. The generation and movement of vacancies can be explained using the following electrolytic reaction equation:

$$O_x^o \leftrightarrow \frac{1}{2} O_2(g) + V_o^{\cdot\cdot} + 2e^- \qquad (2.1)$$

$$me^- + M^{n+} \leftrightarrow M^{(n-m)+} \qquad (2.2)$$

Using the Kroger-Vink notations, the O_x^o denotes oxygen ion at a regular lattice, and $V_o^{\cdot\cdot}$ indicates an oxygen vacancy. These oxygen ions will migrate towards the anode-oxide interface, and their movement will be regulated by: (i) Electric drift due to potential gradient, (ii) Fick diffusion due to ion-concentration gradient, and (iii) thermophoresis resulting from the temperature gradient

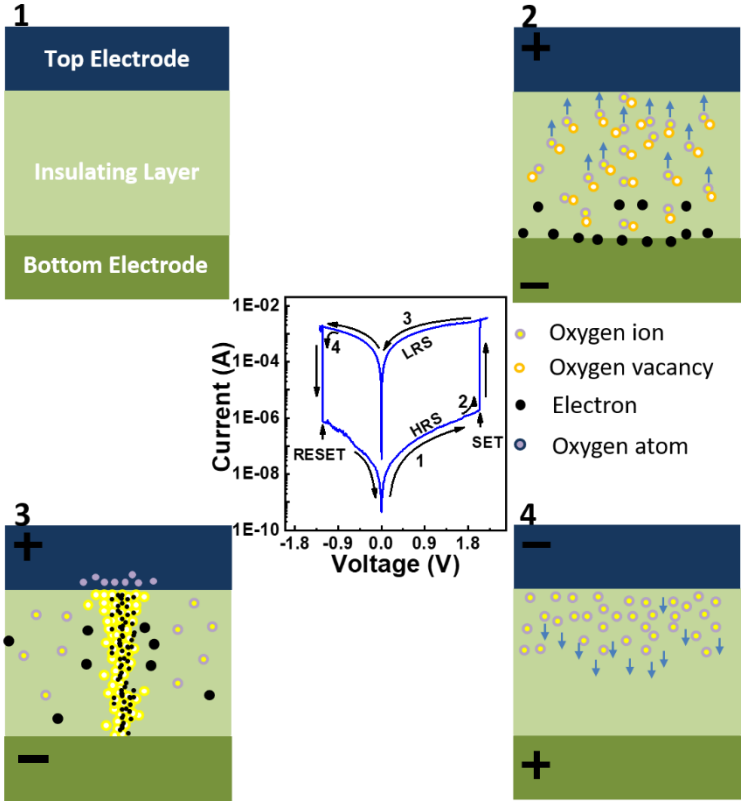

Figure 2.5: Schematic demonstration of resistive switching mechanism in a VCRAM.

[Yang *et al.*, 2013]. Upon reaching the anode, these ions will either oxidized to neutral non-lattice oxygen atoms which can diffuse into the electrode resulting in the evolution from the electrode surface or will react with the oxidizable anode to form thin interface oxide that may be insulating or conducting. Furthermore, the positively charged oxygen vacancies will simultaneously drift towards the cathode, forming an n-type semiconducting region near the interface. Eventually, the oxygen vacancies inside the bulk will form a highly conductive path when the electrons traverse though them between the two electrodes. Figure 2.5 demonstrates the events and redox reactions involved in the switching process for the bipolar VCRAM device. Apart from the above-mentioned filamentary-VCRAM, when any of the insulator- electrode interfaces form a Schottky contact, and other interface forms an Ohmic contact, the device will be termed as interface-VCRAM. The Schottky barrier will result in an energy band's banding to align the energy bands with the Fermi energy levels across the interface. The electromigration of oxygen vacancies will modulate this Schottky barrier that will regulate the resistance of the device. These devices often produce a gradual set and reset process that makes them a suitable candidate for the Neuromorphic computing applications [Yu *et al.*, 2012].

2.3 Conductive Bridge RRAM (CBRAM)

In contrast to the VCRAM, the conductive bridge RRAMs (CBRAM) device's switching mechanism is governed by the metal ion migration from an electrochemically active electrode. When a bias is applied on the electrochemically active metal electrodes, it oxides to cations that traverse through the insulating dielectric layer, and connects the electrode with another inert electrode located at the other terminal of the device. Figure 2.6 shows a typical example of HfO_x

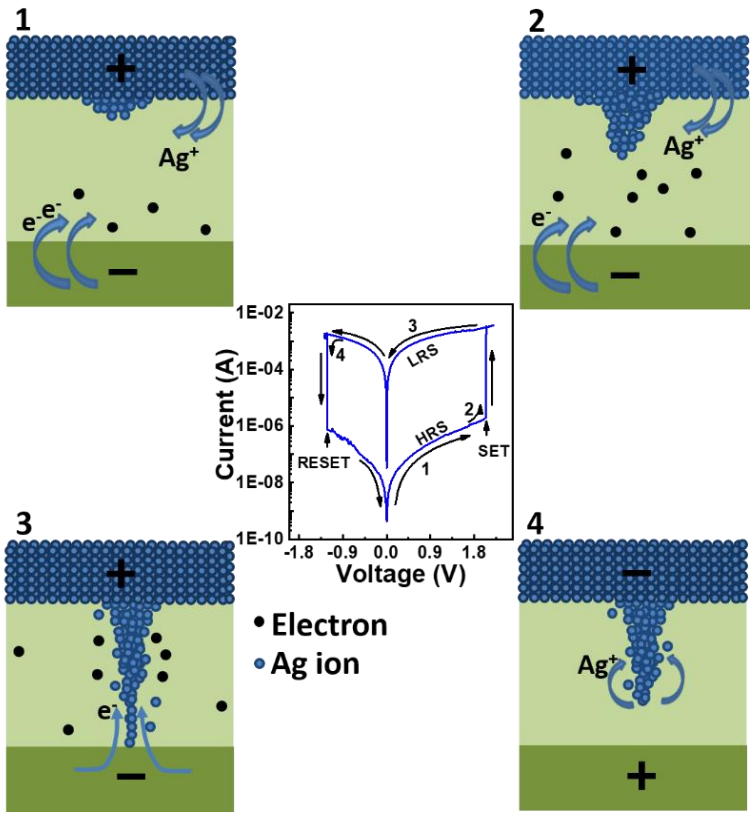

Figure 2.6: Demonstration of switching mechanism in a CBRAM device using typical current-voltage characteristics and related movement of ions and atoms during each transition (1-4) between the HRS and LRS.

switching layer based CBRAM device with Ag active TE where the complete switching mechanism has been bifurcated into four parts. The pristine devices are in their inherent HRS

state, and an initial forming process is often required to activate the devices. When no bias is applied on the device, there will be no migration of metal ions from the TE into the dielectric. Firstly, a smaller positive voltage applied to the Ag electrode, the electrochemical dissolution of Ag ions ($M \rightarrow M^{x+} + xe^{-}$) will be initiated (1), and simultaneously, the injection of electrons from the BE will also happen. With a higher bias voltage, more Ag ions will migrate through the dielectric layer (2) and get reduced to Ag atom near the dielectric-BE interface ($M^{x+} + xe^{-} \rightarrow M$). Eventually, the ion migration and accumulation of Ag atoms will initiate the formation of CF and thus resulting in modulation of conductance of the device. With sufficient bias on TE, the Ag atoms will reach the TE, creating a highly conductive path between the two electrodes (3) and thus completing the "Forming" process that switches the device from HRS to LRS. This will result in the accomplishment of the set process. The device will retain its LRS state even when the voltage bias is removed. When the voltage polarity is reversed, the Ag atoms will again oxides to Ag ions, which will traverse back towards the TE that will switch the device to HRS. The switching of the device from LRS to HRS completes the reset process. The migration of Ag ions and formation of CFs has been majorly recognized by the cross-section TEM images in M-I-M devices or the topographic TEM image in case of lateral structures during the in-situ characterization of the devices. The most common active metal electrodes exploited for CBRAM devices are Ag Cu, Ni, and Al. All these metals tend to dissolve and migrate through dielectrics when an electric field is applied across them. As the switching behavior of a CBRAM device often depends on the TE activity, the switching is mostly bipolar with biasing at the TE and the BE at ground potential [Kozicki and Barnaby, 2016].

2.4 RRAM Device Structures

The RRAM device structure and its dimensions are vital points that regulate device performance and its reliability. At the university or research institute level, the facilities required to fabricate a wafer-scale RRAM chip may not be the state-of-the-art standard, and hence most of such places fabricate the proof-of-study test sample with simple M-I-M sandwich structures. The commonly fabricated device structures to study the RRAM characteristics are as following:

i) Common BE
ii) Cross-point architecture
iii) Cross-bar architecture

Each structure carries its advantage, disadvantage, and complexities. Figure 2.7(a) demonstrates the common BE structure with different cell size, where the BE is made common to all devices. In this structure either a conducting substrate or a conductive film over an insulating film is used. An insulating layer is deposited over the entire BE. Some part of the bottom is left exposed so that during the electrical characterization, the electrical connections can be made out of it. Furthermore, the TE of the desired material and different sizes can be patterned over the switching layer using shadow mask or the lithography. The issues with these structures is that the TE cannot be scaled below 100 μm^2 owing to limitation of probe station characterization tip size. Primary solution to this issue is the use of conductive atomic force microscopy for scan and resistive switching behavior characterization by placing the CAFM tip on the TE and keep the BE grounded; however, that requires a highly sophisticated setup and seems not feasible for research being conducted at academic and research institute level [Lanza *et al.*, 2019].

To overcome the abovementioned issue, cross-point RRAM devices can be a useful approach, although the device fabrication steps involved in this architecture is a bit more complex as it requires the devices to be patterned using lithography twice, firstly for the BE and second for the TE. In some cases, the etching of switching layer is also required for complete isolation of each memory cell. Figure 2.7(b) displays a device schematic of a cross-point memory cell showing the overlapped region of the two electrodes as the active switching area. Using this architecture, the device dimensions can be scaled down to as small as 1 μm^2 and 100 nm^2 using the photolithography and electron beam lithography (EBL), respectively whereas the top and BE pad

size are still large (~10^4 μm^2) to take proper contacts using probs in the probe station [Govoreanu *et al.*, 2011; Park *et al.*, 2012]. While the cross-point structure provides excellent scalability, some

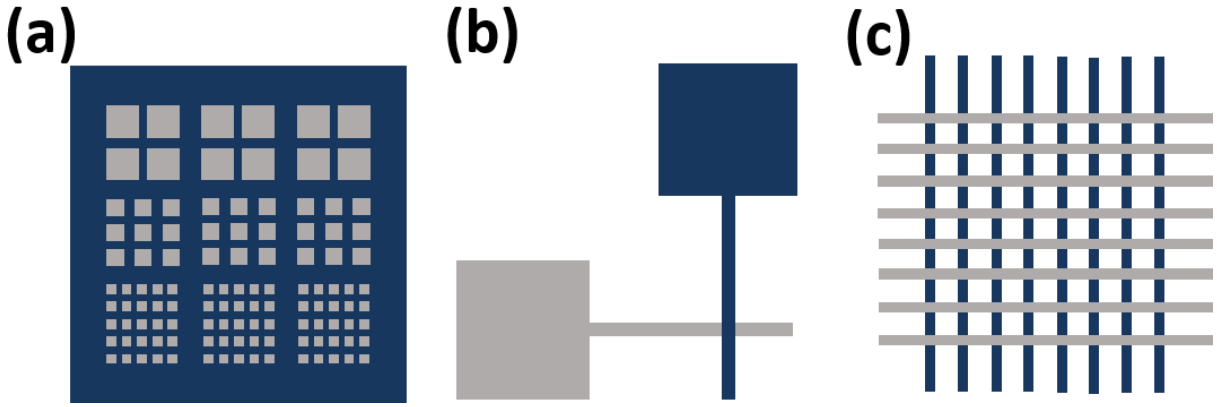

Figure 2.7: Schematic diagram of the commonly used RRAM device architectures. **(a)** The BE is common to every cell and the switching layer and TEs were patterned. **(b)** Cross-point structure provides the isolation between each device with separate bottom and TEs. **(c)** Cross-bar structure forms multiple cross-point cells interconnected to each other, providing higher device density and advantage of 3D architecture fabrication.

vital issues such as the sneak path leakage current cannot analyzed with this type of structure. These issues can be resolved using a technique which is rather more complex but with a higher on chip cell density. As shown in the Figure 2.7(c), the 3D device structure comprises of multiple cross-bar arrays of M-I-M cells that interconnected using thin wires terminating at larger pads. The characterization setup for these advanced cross-bar circuit structures typically requires die packaging and printed circuit board along with a switching matrix tool [Prezioso *et al.*, 2015; Prezioso *et al.*, 2016].

The cross-bar architecture is in-fact a combination of multiple interconnected cross-point devices. As the resistive switching phenomenon is a stochastic process where formation and rupture of CF is a random event that depends majorly on the device size. Device size also contributes towards the reliability issues as the larger device size introduces variability in switching voltages and peak currents during set and reset process. Hence, the device size above 100 μm^2 should be avoided when characterizing on the probe station. However, these devices can be characterized using nanoscale characterization setups such as CAFM [Wei *et al.*, 2016].

2.5 Performance Parameters of RRAM Devices

The various electrical characteristics of an RRAM device defines the clear interpretation of switching performance. Before analyzing the electrical characterization data, the fabrication processing is critically important to obtain a high performance device. Obtaining a highly uniform switching layer with excellent interfaces with the electrode is highly desirable. A high level of vacuum must be maintained while transferring the sample from on fabrication process to another, although this is not feasible in most cases as the deposition equipment are often different for electrodes and switching layer. The electrical parameters that are crucial for analyzing the device performance are as following:

i) Endurance
ii) Retention time
iii) Switching speed and power consumption
iv) Variability
v) Scalability

2.5.1 Endurance

Endurance of an RRAM device is termed as the maximum number of times a cell switching between multiple electrical resistance states while maintaining a sufficient resistance ratio between each state. The desired on/off ratio value may vary from application to application and hence the criterion for the device failure may vary; however, the failure is a progressive event and may not happen in one specific cycle [Yu *et al.*, 2012]. The endurance characteristics of an RRAM cell can be achieved using differential experimental techniques such as:

i) Continuous *I-V* sweeps
ii) Pulsed voltage stress

Figure 2.8(a) demonstrates the example of a ITO based RRAM device where the HRS and LRS levels are extracted from continuous *I-V* sweeps for 100 cycles at 0.1 V read voltage. The read voltage needs to be chosen very so as to achieve the maximum memory window. This technique confirms the switching in each cycle. One major drawback of this method is that the time required for collecting the data points of an *I-V* sweep from the semiconductor characterization system is longer (60 s) than actual switching time when characterized using a voltage pulse source. This issue becomes more severe when characterization system has to measure low currents of nano ampere range. In the pulsed voltage stress (PVS) method, a pulse sequence of set-read-reset-read has been applied and the current is measured simultaneously for each transition. The set and reset pulse width and amplitude can be adjusted as per the requirement and device performance. Figure 2.8(b) displays a similar curve that shows 10^6 cycles of pulse endurance with 500 ns set pulse width with -1.5 V amplitude and 1 µs reset pulse width with +2 V amplitude. As discussed above, the memory window in the two curves significantly differ from each other. The primary challenge with this method the requirement of an additional hardware i.e. the pulse source that adds additional cost (for example Keithley 4225 PMU). As the research progressed, the cyclic endurance has been remarkably improved up to 10^{12} cycles [Hsu *et al.*, 2013].

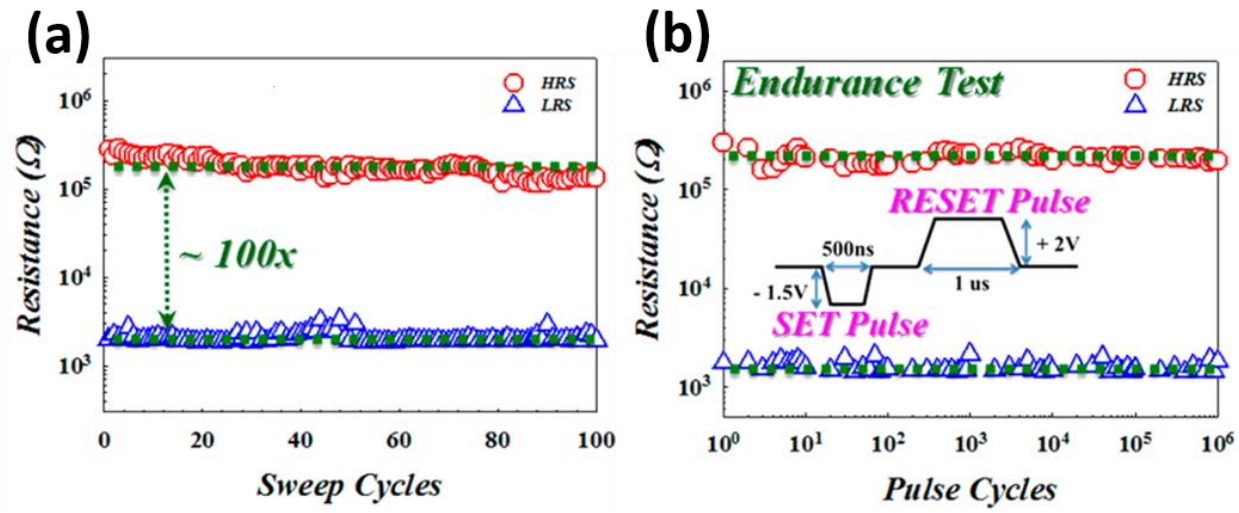

Figure 2.8: (a) Displays endurance test using the continuous *I-V* sweep method for 100 cycles in ITO based RRAM device. **(b)** Demonstration of pulsed voltage stress method for endurance test using the voltage pulse shown in the inset. Reprinted with permission from [Chen *et al.*, 2017].

2.5.2 Retention Time

The RRAM devices being a NVM must hold the data stores even if the biasing is removed. Holding the data for an RRAM device means it must retain its HRS and LRS for longer time after the set and reset transitions, respectively. The retention time of an RRAM can be examined by switching the device to either the HRS or LRS and then apply a constant voltage stress at a particular read voltage (often 0.2 V) and subsequently measure the current versus time (*I-t*) curve for each state [Qi *et al.*, 2018]. Figure 2.9 demonstrates the retention time characteristics of an ITO

based RRAM cell, tested for 10^4 s at 125 ℃ . Maintaining the current levels during HRS retention measurement

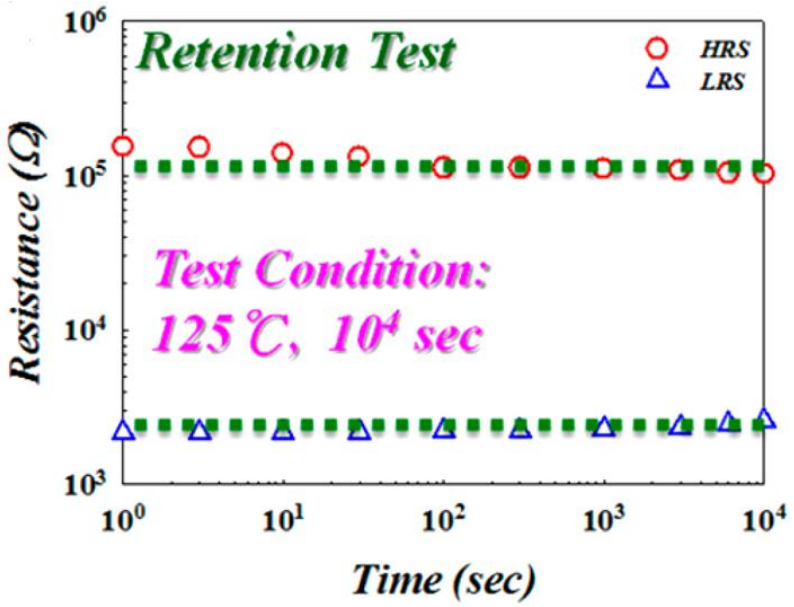

Figure 2.9: The retention time measurement of ITO based RRAM for 10^4 s at 125˚C. Reprinted with permission from [Chen *et al.*, 2017].

is much easier as it is the natural state of the device. However, LRS current may fluctuate with time due to the atomic rearrangement induced during the set transition may forgo with time. Compliance current limits also affects the stability of LRS levels as it controls the filament dimensions or in other words the strength of the filament. Hence, higher the compliance current limit, stronger and stable will be the filament formed that leads to a longer retention time. Ideally, the desired data retention figures for NVM technologies is 10 years at 85 ℃ [Subhechha *et al.*, 2016]. The retention measurement for 10 years is not practically possible and for that reason, the retention time of few hours or days are reported where the retention time of 10 years has been by extrapolating the time axis [Nail *et al.*, 2016].

2.5.3 Switching speed and Power Consumption

The performance of a memory device is primarily by investigating the time required for the device to transit between the two states by using a pulse source. Similarly, the power consumption of a cell is also a critical aspect that must be taken care of while considering the device performance. Careful selection of switching layer material like high-k material with high

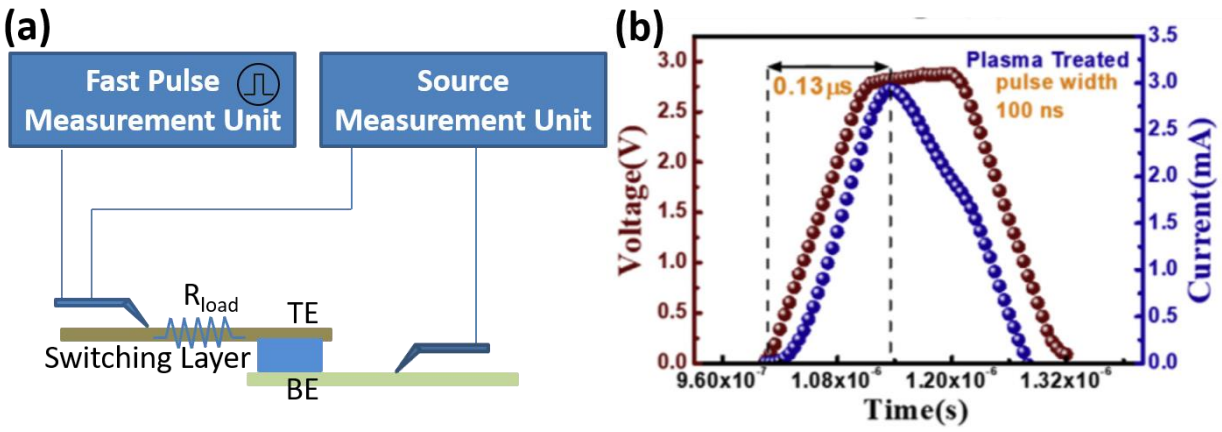

Figure 2.10: (a) Schematic diagram of setup for high-speed switching measurements. **(b)** Switching speed of a Ti/HfO_x(Ar plasma treated)/Pt RRAM device using a voltage pulse. Reprinted with permission from [Fantini *et al.*, 2012; Ku *et al.*, 2018].

oxygen ion conductivity and low-k material of lesser thickness will improve the switching speed of the device [Kumbhare *et al.*, 2017]. For a state-of-the-art NVM device, the ideal switching speed is few nano seconds which is much higher than the existing main memory and the storage. Figure 2.10(a) shows the schematic diagram of characterization setup for switching speed analysis using a pulse measurement unit for application of high-speed square or triangular pulses and a source measurement unit to simultaneously acquiring the applied voltage and resulting current [Chen *et al.*, 2019]. Figure 2.10(b) demonstrates the switching speed analysis of Ti/HfO_x(Ar plasma treated)/Pt RRAM devices using a voltage pulse with pulse with 100 ns and amplitude 2.85 V. Furthermore, the switching speed for the set process has been reported as 130 ns [Ku *et al.*, 2018]. Optimization of pulse width, voltage amplitude, rise time, and fall time must be done before concluding the switching speed.

The same setup can be used for switching power characterization for distinct operating currents under varying load resistance magnitude. The power consumption can be controlled by efficiently decreasing the compliance current [Molas *et al.*, 2018]. The main component of power consumption during the transition is the reset power as the device is in the LRS. Also, the power consumption of a CBRAM device is lower as the formation/rupture of CF is easier in comparison to a VCRAM device [Wu *et al.*, 2019].

2.5.4 Variability

The variability in RRAM devices is one of the major reliability issues that needs to be resolved before initiating the bulk fabrication at chip level. The device-to-device and cycle-to-cycle variation in the electrical characteristics limits the exploitation of these devices in memory and neuromorphic computing application. However, variability can be taken as advantage for the development of application such as true random number generators and physically unclonable function for hardware security. The cell-to-cell variability can be controlled by improving the fabrication process environment i.e. the uniform thicknesses, smooth interfaces, and identical device dimensions [Li *et al.*, 2017]. The cycle-to-cycle will be a difficult to handle until the exact device physics and mechanism behind switching events is known. The cycle-to-cycle variability is primarily caused due to the stochastically formation and rupture of the CF. The dimensions and place of formation and rupture of CF is still cannot be controlled precisely and introduces variability issues in the electrical characteristics of the device. Hence, it is important to incorporate the study of variation and yield in our research. The cycle-to-cycle

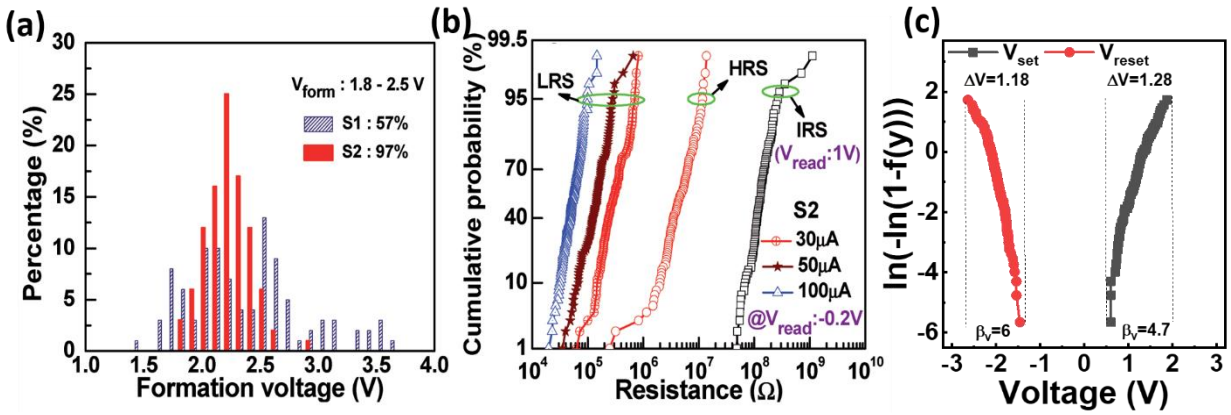

Figure 2.11: (a) Histogram formation for forming voltage distribution of 100 W/Al_2O_3/TaO_x/TiN RRAM devices. **(b)** Cumulative probability distribution of IRS, LRS, and HRS for 100 W/Al_2O_3/TaO_x/TiN RRAM devices. Weibull's distribution of V_{set} and V_{reset} of initial 200 cycles for Ag/PVP:GO/HfO_x/ITO RRAM devices. Reprinted with permission from [Samanta *et al.*, 2017; Varun *et al.*, 2020a].

variability must be tested for I_{HRS} and I_{LRS} at a particular read voltage (generally 0.2 V) during voltage sweep and pulse endurance test [Grossi *et al.*, 2016]. Furthermore, the recommended method to study the variability is to plot to plot each parameter on the histogram or cumulative distribution or the Weibull's distribution [Samanta *et al.*, 2017; Varun *et al.*, 2020a]. These plots

will provide valuable information to ascertain the threshold value for distinct HRS and LRS levels. Figure 2.11(a) shows the distribution % of forming voltage of 100 W/Al_2O_3/TaO_x/TiN RRAM devices from Sample 1 where the 97% devices have shown a range bound variation (1.8 V to 2.5 V) whereas the Sample 2 shows 57% variation. Similarly, Figure 2.11(b) demonstrates the cumulative probability distribution of IRS, HRS and LRS resistances at read voltage -0.2 V for HRS and LRS and +1 V for IRS. Furthermore, Figure 2.11(c) displays the Weibull's distribution of switching voltages of Ag/PVP:GO/HfO_x/ITO RRAM device for 200 initial voltage sweep cycles. The shape factor (β) value of Weibull's distribution confirms the reliability of the device.

2.5.5 Scalability

As the RRAM is still considered as the emerging NVM technology, the scaling limits of these devices is still been explored. For convenience of electrical characterization, researchers generally fabricate devices with large area (~100 µm × 100 µm). However, the switching characteristics and performance varies abruptly when devices are scaled down to sub nanometers. In devices with larger area (>25 μm^2), the resistive switching takes place along the weak regions of the switching layer whereas the nanoscale devices (area<100 nm^2) will execute the switching process at the stronger region. The standard lithography process can scale down the device to only micrometers whereas to scale the device to sub nanometer range, highly sophisticated instruments such an EBL or Extreme Ultra-Violate (EUV) lithography is required [Luo *et al.*, 2017; Yu *et al.*, 2016]. However, affordability and throughput of these instruments will be an issue at university or research institute level. Electrical characterization of nanoscale RRAM devices also requires high level expertise where CAFM tips or scanning tunneling microscope are used to apply electrical stresses. Figure 2.12(a) displays the X-HRTEM image of a highly scaled TiN/Ta_2O_5/Ta/TaN RRAM devices with switching layer thickness varying from 0.5 nm to 2 nm and device lateral dimension are 28 nm [Park *et al.*, 2015]. Furthermore, Figure 2.12(b) describes the effect of scaling of TaO_x film on the reset voltage was explore where the 0.5 nm thick devices showed a constantly increasing reset voltage while increasing the targeted HRS resistance was reached. Other three device showed no trend in the reset voltage. Moreover, the devices with higher thickness failed to reset after 1000 pulse endurance cycles with wider resistance spread where the 0.5 nm thick device demonstrated a remarkable endurance of 12000 cycles with narrower distribution of the HRS resistance, as shown in Figure 2.12(c).

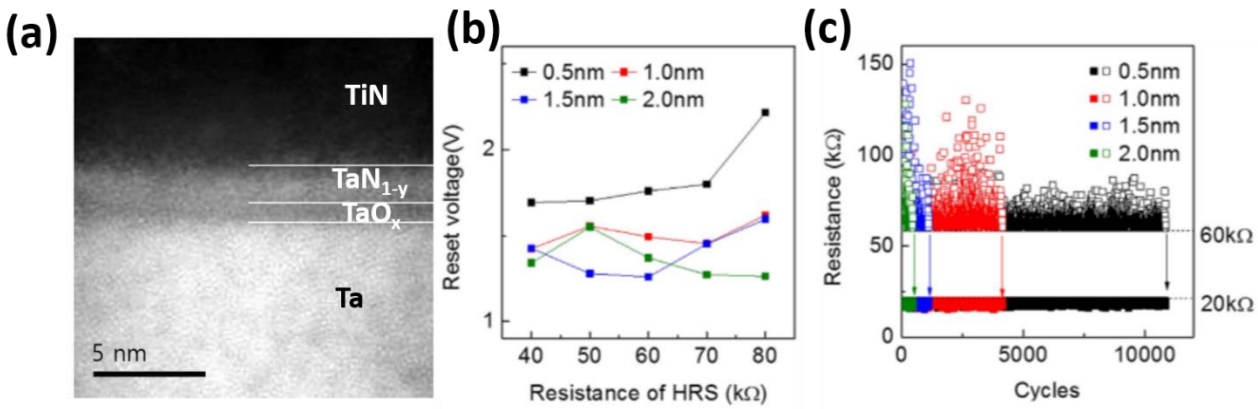

Figure 2.12: (a) X-HRTEM image of TiN/Ta_2O_5/Ta/TaN RRAM devices on 5 nm scale. **(b)** Reset voltage variation with TaO_x thickness with increasing targeted HRS resistance. **(c)** Pulse endurance characteristics of TaO_x based device with varied thickness. Source: [Park *et al.*, 2015].

2.6 CURRENT STATUS

The last few years have been crucial for research and development in the field of RRAM devices and the related applications. The extensive research of decades has created a platform for RRAM technology from where it can land into futuristic applications such as neuromorphic

computing, logic implementation, in-memory computing, random number generator, and obviously the memory storage. Table 2.1 comprises of some of the major contributions in last six years and an attempt has been made to provide a brief performance comparison analysis of RRAMs fabricated on different substrates.

Table 2.1: Comparative analysis of various high-performance RRAMs reported on flexible and rigid substrates in previous six years. Subs: Substrate; I_{cc}: Compliance current; Memory Window: I_{on}/I_{off} or R_{off}/R_{on}; Endure: Endurance; Ret: Retention

Device Structure	Subs.	V_{set} (V)	V_{reset} (V)	I_{cc} (A)	Memory Window	Endur.	Ret.	Ref.
Ag/G-QDs/PVP/Ag	PET	1.6	-1.7	100 µ	14	5×10^2	30 d	[Ali *et al.*, 2015]
Ag/DUV-ZnO:Mn/ITO	PET	−1.8 – (−4.2)	2.4–4.5	NA	60	10^2	4×10^3 s	[Wu *et al.*, 2015]
Ag/PMMA/FTO	Glass	~1.3	~1.9	NA	10^3	400 s	NA	[Mangalam *et al.*, 2016]
Al/PMMA/MoS_2/PMMA/Al	PET	4.8	-4.9	NA	10^4	10^2	10^5 s	[Han *et al.*, 2016]
Al/PVA+GO/ITO	Glass	-0.75	3	0.1	10^4	1.5×10^4	10^4 s	[Sun *et al.*, 2016]
Ag/hBN–PVOH/ITO	PET	0.8	-1	10 µ	4.8×10^2	10^3	10^4 s	[Siddiqui *et al.*, 2017]
Cu/Ti/PVP/ITO	PEN	0.25	-0.5	NA	10^5	10^3	10^4 s	[Kang *et al.*, 2017]
Al/PVK/ITO	Glass	1	-3.1	0.1	10^3	$\sim5\times10^3$	10^4 s	[Ling *et al.*, 2017]
Au/ZnO/$CH_3NH_3PbI_3$/ITO	Glass	1.1	-0.6	1 m	500	10^2	10^4 s	[Hwang and Lee, 2017]
Ag/ZrO_2/G/Pt	Si/SiO_2	~.65	~-1	10 m	$\sim10^5$	10^6	10^4 s	[Liu *et al.*, 2016]
Al/PS+ZnO/ITO	Glass	-1.15	NA	0.1	$10^{4.7}$	3×10^4	10^4 s	[Sun *et al.*, 2018]
Al/ZnO–PVA/PEDOT:PSS/Al	PET	3.6	-3.6	5×10^{-2}	3×10^5	10	2×10^3 s	[Hmar, 2018]
Al/GO-TiO_2/ ITO	PET	0.52	-0.5	1 m	10^2	5×10^2	10^5 s	[Zhao *et al.*, 2018b]
Al/WS_2 NSs:PMMA/ITO	PEN	~0.5	~-4.5	NA	6×10^4	10^2	10^4 s	[Lee *et al.*, 2019b]
Cu/gMoS_2-PMMA/ITO	PET	-1	~1.1	NA	10^4	10^4	10 d	[Bhattacharjee *et al.*, 2018]
Al/PVP+AMT/Al	Glass	-1.05	~3	0.1	10^4	98	5×10^5 s	[Sun and Wen, 2019]
$IrO_x/Al_2O_3/Ta_2O_5/MoS_2/TiN$	Si/SiO_2	-2.4	1.5	30 µ	3×10^4	10^3	10^4 s	[Qiu *et al.*, 2019]
ITO/TiO_2/HfO_2/Pt	PEN	1.5	-1.5	3 m	10	2×10^3	10^4 s	[Zhang *et al.*, 2019]
TaN/Al_2O_3/ZrO_2/Al_2O_3/TaN	PET	2-2.5	-2-(-2.7)	1 m	10	10^7	10^4 s	[Kumar *et al.*, 2019]

Table 2.1: Comparative analysis of various high-performance RRAMs reported on flexible and rigid substrates in previous six years. Subs: Substrate; I_{cc}: Compliance current; Memory Window: I_{on}/I_{off} or R_{off}/R_{on}; Endure: Endurance; Ret: Retention

Al/PCBM+PVP/Al	Glass	NA	~-1.8	NA	10^4	NA	10^5 s	[Sun *et al.*, 2020]
GaIn/PFBT-TiO_2/ITO	PET	-1.7	1.6	NA	10^3	30	NA	[Zhang *et al.*, 2020a]
Pt/a-IGZO/Ni/Pt	Si/SiO_2	0.76	0.26	10 m	$>10^2$	250	10^4 s	[Lee *et al.*, 2020]
Cu/HfO_2/Au	PDMS	1.2	-1	1 m	10^3	10^5	10^4 s	[Wang *et al.*, 2020b]
Mg/Gelatin/W	PLGA	2.21	-2.2	100 µ	10^2	10^2	10^4 s	[Liu *et al.*, 2020]
ITO/HfO_x/TiN	PI	0.5	-0.22	5×10^{-5}	20	3×10^5	5×10^3	[Zhang *et al.*, 2020b]