Chapter 4

Multi-temperature ALD Scheme for Enhanced Reliability

The primary aim of this research is to develop such a mechanism for RRAM fabrication that provides a better control over filament formation and rupture process that eventually leads toward reliable and low voltage switching operations. The primary component of a VCRAM device is the switching layer which constitutes of binary or ternary metal oxides and the switching mechanism is coltrolled by the movement of oxygen vacancies. This chapter explains one such technique that uses the atomic layer deposition technique to induce the oxygen vacancies during the metal oxide deposition process. A very fine control over the oxygen vacancy conentration in the partial region of switching layer created a gradual profile of oxygen vacancies that eventually created two weak reagions where the connection and rupture of conductive filament process will be executed [Varun *et al.*, 2017].

4.1 INTRODUCTION

Resistive random access memories (RRAMs) have emerged as an excellent choice for future non-volatile memory applications [Lee *et al.*, 2015; Tseng and Sze, 2012]. RRAM has demonstrated excellent miniaturization potential, fast switching, low power operation, long retention of data, and capability of multibit storage over the conventional and emerging memory technologies [Bousoulas *et al.*, 2016; Ma *et al.*, 2016; Park and Lee, 2016; Tsai *et al.*, 2016; Zhang *et al.*, 2015; Zhou *et al.*, 2016]. RRAM has a simple metal-insulator-metal structure with insulating layer sandwiched between two conducting electrodes, working on the resistive switching phenomenon. Information in an RRAM cell is stored in the form of reversible low resistance state (LRS) and high resistance state (HRS) as a result of formation and rupture of conductive filament (CF) [Beck *et al.*, 2000]. Several materials including metal oxides and nitrides [Daniele, 2016], perovskites [Panda and Tseng, 2014; Panwar *et al.*, 2017], polymeric dielectrics [Jang *et al.*, 2016; Mangalam *et al.*, 2016], and chalcogenides [Zhuge *et al.*, 2015] have been explored as the insulating material in RRAMs. However, metal oxides have been the main subject of investigation of switching behavior in RRAMs since last decade. Different metal oxides such as HfO_x [Park *et al.*, 2016], AlO_x [Jana *et al.*, 2016], NiO_x [Daniele, 2016], TaO_x [Park *et al.*, 2016], TiO_x [Tang *et al.*, 2014], and ZnO [Ke *et al.*, 2016] have been extensively explored in order to obtain the improved RRAM characteristics. Among the different metal oxides investigated, AlO_x based RRAM devices have shown promising resistive switching characteristics due to its properties like high dielectric constant, low leakage current, high breakdown voltage, and high thermal stability [Jana *et al.*, 2016; Lai-Guo Wang, 2015; Li *et al.*, 2016; Lin *et al.*, 2014a; Roy *et al.*, 2015]. In addition, it is used in metal oxide semiconductor field-effect transistors (MOSFET) as the oxide layer and encapsulation layer in organic devices [Albadri, 2014; Jeon *et al.*, 2008]. One of the very widely used AlO_x deposition technique is atomic layer deposition (ALD), which produces atomically flat, highly uniform, and stoichiometry-controlled oxide layers, highly desirable for excellent RRAM characteristics. In ALD, the deposition temperature is the one of the key parameters to control the above-mentioned attributes of the oxide layer. However, there are very few reports available in

which the role of deposition temperature has been discussed in detail to improve the RRAM performance [Run-Chen Fang, 2013]. In addition, the deposition temperature has rarely been envisaged as the variable process parameter during the deposition to seek any performance improvement in RRAMs.

In this chapter, four types of Ti/AlO_x/Ti RRAM devices fabricated on glass substrates are studied for their performance. For first two types of RRAM devices, the deposition temperature of switching layer was 80 ˚C and 150 ˚C respectively. For third and fourth type of devices, a multi-layer multi-temperature process (80 ˚C/150 ˚C/80 ˚C and 150 ˚C/80 ˚C/150 ˚C respectively) has been used to deposit the switching layer stack [Bharti and Tiwari, 2015]. All samples were fabricated at low temperatures making the devices compatible with Back-end-of-line CMOS process. The devices have shown typical bipolar resistive switching behavior, however, the devices fabricated with temperature scheme of 150 ˚C/80 ˚C/150 ˚C have shown improved characteristics with comparatively better repeatability, longer retention time, uniform and lower set and reset voltages over multiple cycles of operation. The conduction mechanism in the RRAM Devices has been investigated and it was concluded that ohmic and space charge limited conduction were dominant conduction mechanisms in the devices at lower and higher voltages respectively. Improved performance in devices fabricated with multi-temperature scheme of 150 ˚C/80 ˚C/150 ˚C with lower switching voltage operation was attributed to the localization of switching phenomenon in the region with weaker conductive filament.

4.2 MULTI-TEMPERATURE DEPOSITION SCHEME

The surface morphology of AlO_x thin films is shown in Figure 4.1(a-d). The root mean square (RMS) roughness of AlO_x and Ti films are shown in Table 4.1. Although the AlO_x deposition was performed by ALD, which produces smooth film but due to the inherent

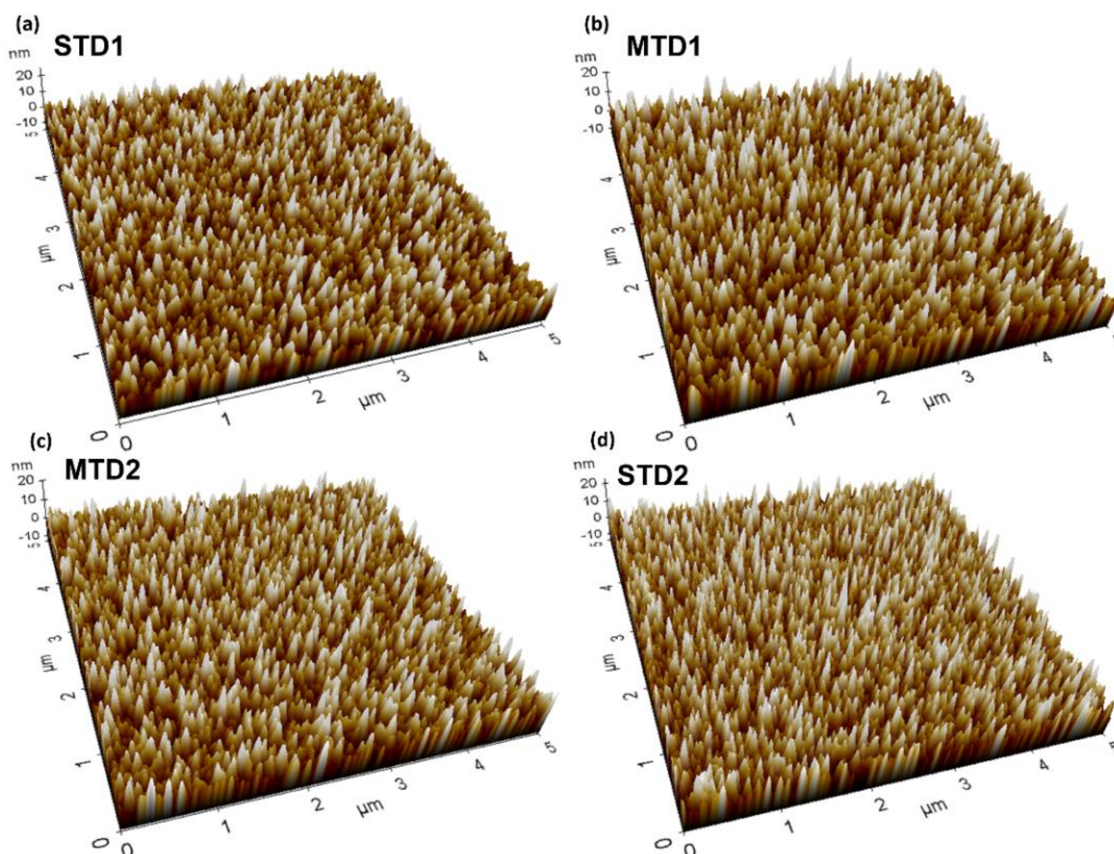


Figure 4.1: (a-d) AFM images of STD1, MTD1, MTD2, and STD2, respectively, demonstrating surface roughness of each film.

roughness of glass substrates and that of polycrystalline Ti BE layer, the subsequent layers assumed the morphology of layers beneath. Interestingly, it can be noticed from table 1 that the roughness of the all four amorphous AlO_x thin films are lower than the polycrystalline layer

Table 4.1. Thickness and roughness of top and bottom surfaces of samples fabricated with different deposition schemes.

Deposition Scheme	Thickness (nm)	Bottom Surface Roughness (nm)	Top Surface Roughness (nm)
STD1 (80 °C)	40	4.18±0.06	3.85±0.80
STD2 (150 °C)	40	4.37±0.24	4.2±0.15
MTD1 (80 °C/150 °C/80 °C)	10/20/10	4.18±0.06	4.02±0.16
MTD2 (150 °C/80 °C/150 °C)	10/20/10	4.37±0.24	3.82±0.18

beneath it having nano-sized roughness, a phenomenon recently observed [Lau *et al.*, 2014]. Roughness in bottom and top interfaces could play an important role to obtain a stable resistive switching in RRAM devices due to schottky barrier lowering at metal-oxide interfaces [Lau *et al.*, 2014]. The ALD AlO_x films deposited at low deposition temperatures (ranging from 80 °C to 150 °C in this case) were found to be amorphous for all the four cases when analyzed by grazing angle X-ray diffraction pattern [Simmons, 1970].

As discussed in Chapter 2, the oxygen vacancies plays a very crucial role in switching mechanism of an VCRAM. The density of oxygen vacancies has direct impact over the conducting filament dimensions, and many research groups have tried to exploit this feature of VCRAMs by artificially amplifying or reducing the oxygen vacancy density [Ge and Chaker, 2017; Lee *et al.*, 2019a; Park and Lee, 2016]. Higher the oxygen vacancy concentration in the medium, wider would be conductive filament inside the switching layer, resulting in better control over filament formation and rupture process. Hence, the MTD technique provides us some regions inside the switching layer where the conductive filament would be wider and some region where it would be comparatively narrower, making weak reagion at the interface between the two.

4.3 EXPERIMENTS

The RRAM devices were fabricated on glass substrates, which were cleaned thoroughly in isopropyl alcohol, trichloroethylene, acetone and methanol sequentially for 10 minutes each. A 200 nm thick Ti bottom electrode (BE) was deposited on the glass substrate using the e-beam evaporation technique under a high vacuum of 10^{-6} torr. A 40 nm thick AlO_x was deposited using Savannah S200 thermal atomic layer deposition (ALD) system from Cambridge Nanotech with tri-methyl-aluminium (TMA) and H_2O as precursors at chamber pressure of 10^{-1} torr using four types of deposition schemes namely STD1, STD2, MTD1, and MTD2 as mentioned in table 1. TMA and H_2O pulse duration at both the deposition temperatures was 15 ms. At 80 °C AlO_x deposition, TMA and H_2O purge duration was 30 s and 60 s respectively whereas for 150 °C AlO_x, both precursors had purge duration of 20 s. Finally a 200m nm thick Ti top electrode (TE) was deposited through metal shadow masks over AlO_x by e-beam evaporation technique under same conditions as BE, with top contact areas ranging from 0.002 cm^2 to 0.16 cm^2. Surface morphology of AlO_x and Ti films was analyzed by atomic force microscopy (AFM) using XE-70 from Park Systems in the noncontact mode. The electrical characterization of the devices was performed using 4200-SCS parameter analyzer from Keithley. During the electrical characterization, the potential was applied on the TE and the BE was kept at ground potential. Figure 4.2(a-d)

demonstrates the device schematic fabricated with deposition scheme STD1, MTD1, MTD2, and STD2, respectively.

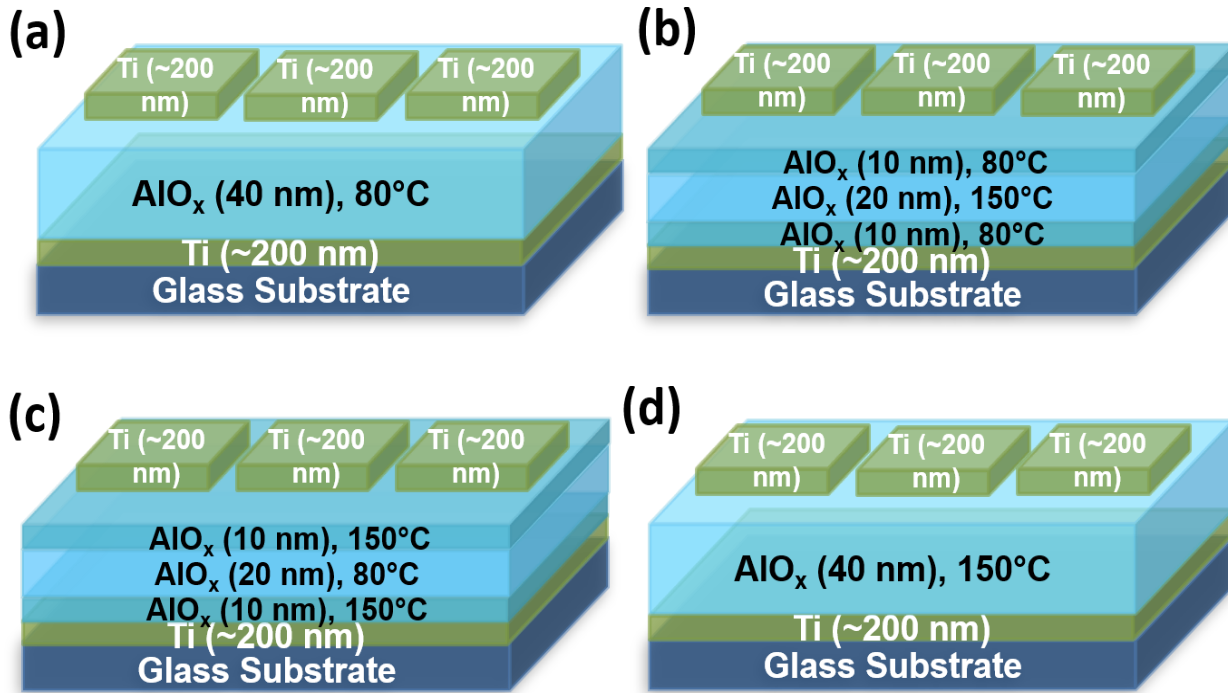


Figure 4.2: (a-d) Schematic representation of AlO_x based RRAM devices fabricated with four different deposition schemes.

4.4 ELECTRICAL CHARACTERIZATION of RRAM DEVICES

Figure 4.3(a-d) shows the current-voltage (*I-V*) characteristics of all type of devices, demonstrating a typical bipolar resistive switching behavior. Voltage biasing was applied on the devices in the sequence of negative potential → zero potential → positive potential → zero potential → negative potential. The current compliance was set to 50 mA to protect the devices from hard breakdown. Figure 4.4(a-d) shows the retention characteristics of all types of devices. In comparison to all other types of devices, MTD2 devices demonstrate a reliable performance with a retention time of 10^3 s at read voltage of 0.1 V. The clear separation between the two states has been maintained for said duration without any degradation in current levels of HRS and LRS suggesting a non-volatile memory characteristic of the devices. Table 2 summarizes various resistive switching parameters for all RRAM devices. It can be observed that MTD2 device has exhibited lower set and reset voltages (V_{set} and V_{reset}), high I_{on}/I_{off}, repeatability and retention time.

Figure 4.5(a) shows the *I-V* characteristics of MTD2 devices with 75 cycles of repeatable operation. The devices were in their inherent HRS before the application of bias. To turn a RRAM device on, one-time application of a high forming voltage (V_f) is required. In the electroforming process, the primary conductive filament (CF) gets formed in the dielectric layer, causing the resistance to drop suddenly and hence a sharp rise in current. The electroforming in the devices has been demonstrated through *I-V* curve in the inset of Figure 4.5(a) showing an abrupt rise in current at V_f = 6.45 V. Figure 4.5(a) shows that at V_{set} = 0.65 V, a sudden rise in current occurs and devices switches from HRS to LRS. Devices are switched back to HRS at V_{reset} = -1.15 V with a sudden drop in current. Figure 4.5(b) shows the DC endurance performance of MTD2 devices in HRS and LRS for 75 cycles measured at 0.1 V read voltage, demonstrating a clear separation between the two states with an I_{on}/I_{off} ratio of 16.

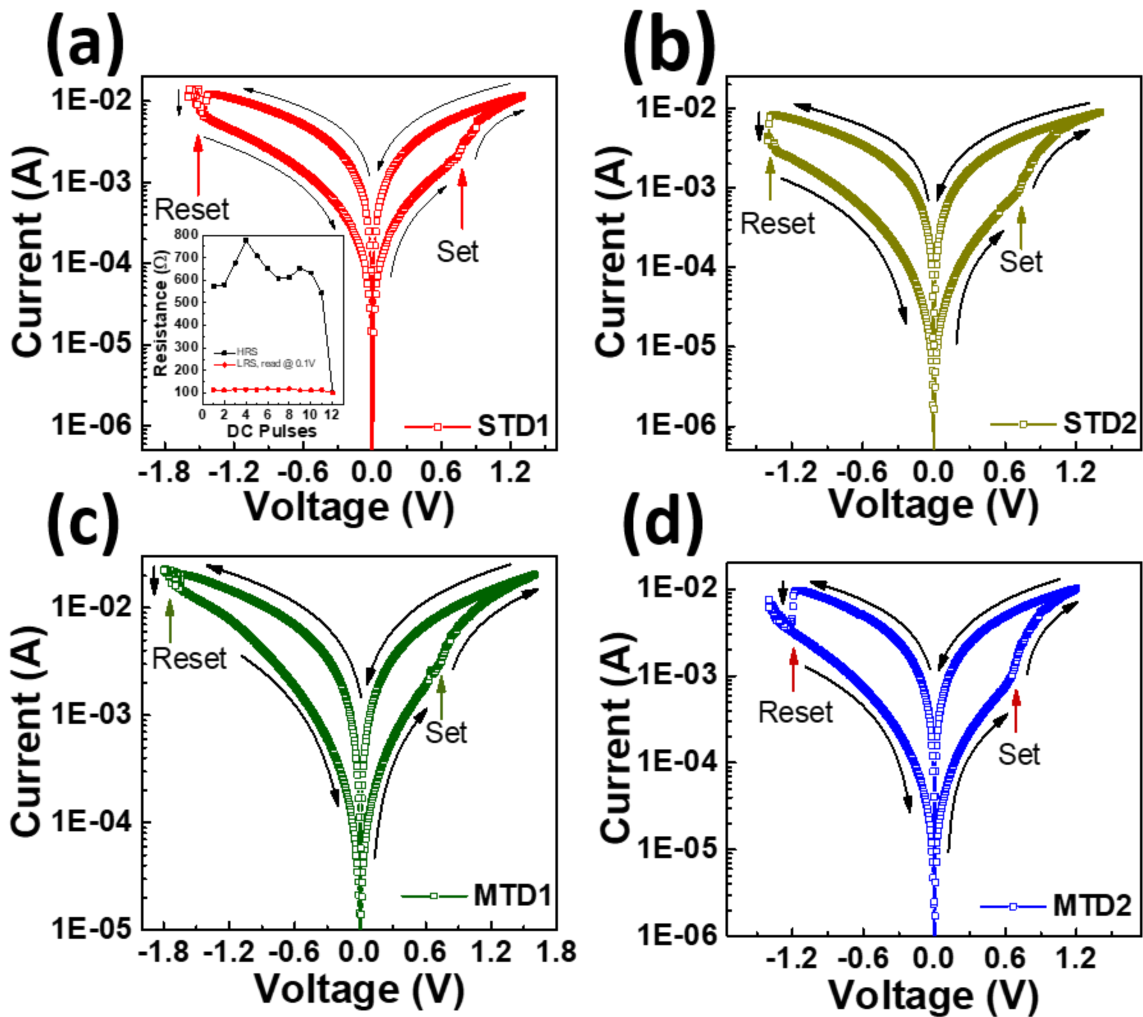


Figure 4.3: *I-V* characteristic of devices showing resistive switching behavior of **(a)** STD1, **(b)** STD2, **(c)** MTD1, and **(d)** MTD2 schemes respectively. Inset of **Figure 4.3(a)** showing the DC endurance test of STD1 device exhibiting 12 cycle of repeatable operation.

It is important to focus on the conduction mechanism of the RRAM devices in order to understand the set and reset process in the device. Figure 4.6(a) and Figure 4.6(b) shows the double logarithmic plot of the *I-V* curve of MTD2 devices as shown in Figure 4.3(d) for the set and reset processes respectively. The double logarithmic curve for positive voltages can be divided into

Table 4.2. Comparison of electrical characteristics of samples in terms of performance parameter.

Parameter	**STD1**	**STD2**	**MTD1**	**MTD2**
Operating Voltage (V)	-1.6 to 1.3	-1.4 to 1.4	-1.8 to 1.6	-1.4 to 1.2
Switching	Bipolar	Bipolar	Bipolar	Bipolar
Repeatability (DC Cycles)	11	1	1	75
I_{on}/I_{off}	6	14	8	16
V_{set} & V_{reset} (V)	0.73 & -1.4	0.7 & -1.25	0.8 & -1.47	0.65 & -1.15

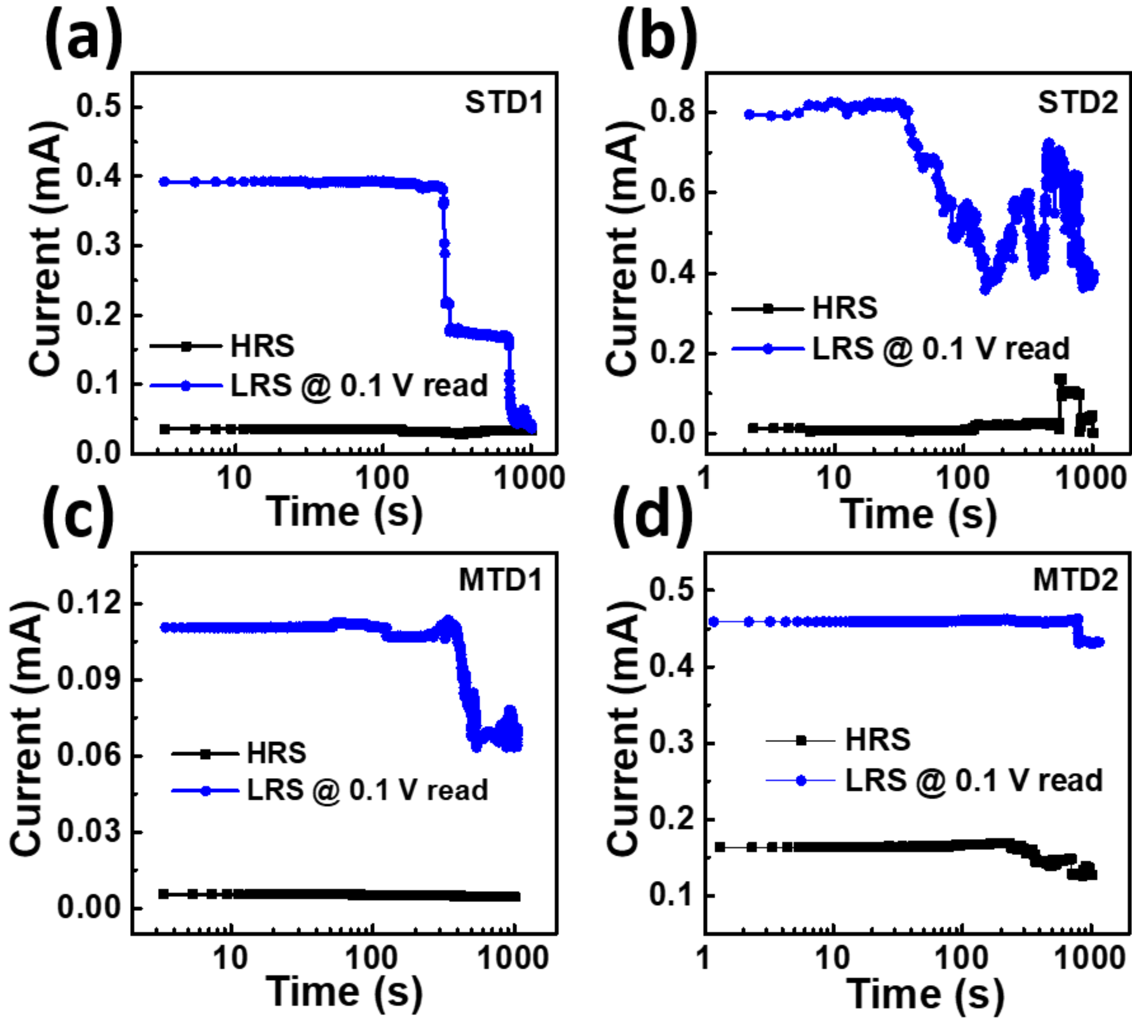


Figure 4.4: Data retention properties of **(a)** STD1, **(b)** STD2, **(c)** MTD1, and **(d)** MTD2 devices measured at 0.1 V read voltage.

four sections depending on the different slopes, which represent different regions of conduction. In the region where, $I \alpha V^{1.1}$, the ohmic conduction is the dominant conduction mechanism. At lower applied voltage, the device will remain in HRS. The associated conduction in this region occurs due to the thermally generated charge carriers, which partially occupies the available trap sites available at either inside the bulk or at the metal-dielectric interface. In the second region, where $I \alpha V^{1.9}$, all the trap sites are filled by the injected charge carriers due to the higher voltages. At $V = V_{set}$, all the available trap sites are filled by the injected charge carriers and consequently further injection of carriers will bring a sharp rise in current as the injected charge density now exceeds bulk charge density [Simmons, 1970]. In this region, the charge transport will be restricted as per the Lampert's theory of space-charge limited conduction (SCLC), driven by the Child's Law ($I \alpha V^2$) given by:

$$J_{child} = 9\varepsilon_m \mu V^2/8d^3 \tag{4.1}$$

where ε_m is the dielectric constant of the material, μ is the mobile of charge carriers, V the applied bias and d the separation between the two electrodes [Chiu *et al.*, 2012]. Further increase in bias voltage will escalate the current with $I \alpha V^{3.85}$ due to the available excess charge carriers. In the fourth region, ohmic conduction prevails.

When the negative bias is applied on TE, the slope of curve will remain unity for voltages ranging from 0 V to -0.95 V in the LRS and follows the ohmic conduction. On increasing the biasing beyond -0.95 V, the trapped electrons will start to escape from the trap sites leaving behind oxygen vacancies which will be annihilated by oxygen ions arriving from the TE-insulator interface. As most of the oxygen vacancies are annihilated by the oxygen ions, the current will suddenly drop [Li *et al.*, 2016].

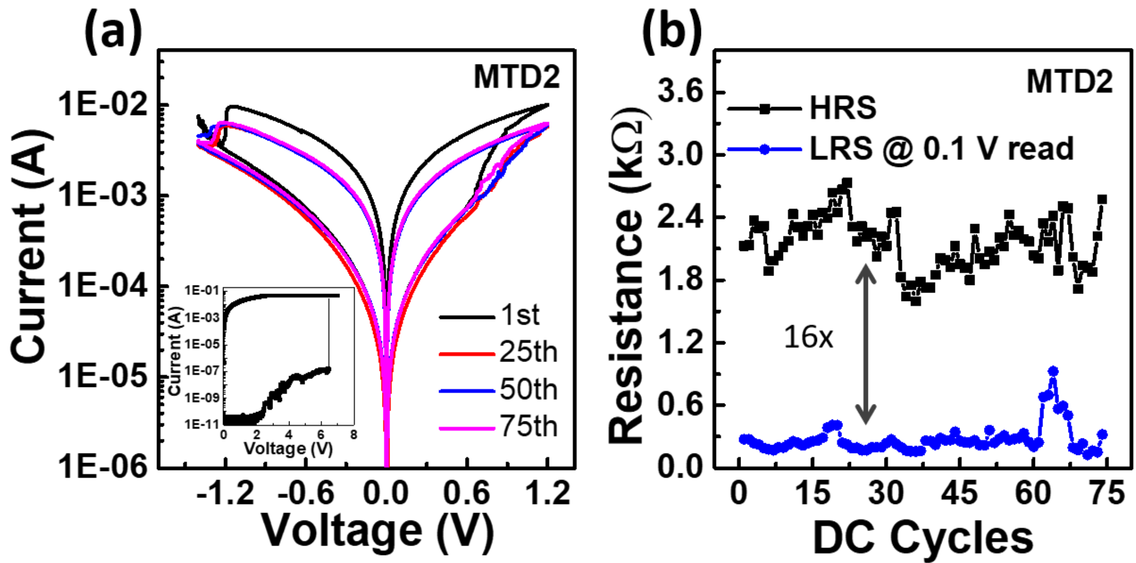


Figure 4.5: (a) *I-V* characteristic of MTD2 RRAM device over 75 cycles of operation, showing typical bipolar resistive behavior. Inset shows the forming process in the device with forming voltage of V_f = 6.45 V and (b) displaying the variation in resistance of device in HRS and LRS (DC endurance test) at read voltage of 0.1 V. Separation of 16 Ω is maintained throughout the operation of 75 DC cycles.

According to the previous studies, the switching mechanism in AlO_x based RRAM devices can be explained as filamentary switching due to redox reactions in the bulk and at the interfaces [Jana *et al.*, 2016; Lin *et al.*, 2007]. From Figure 4.6(a) and Figure 4.6(b), it is deduced that the

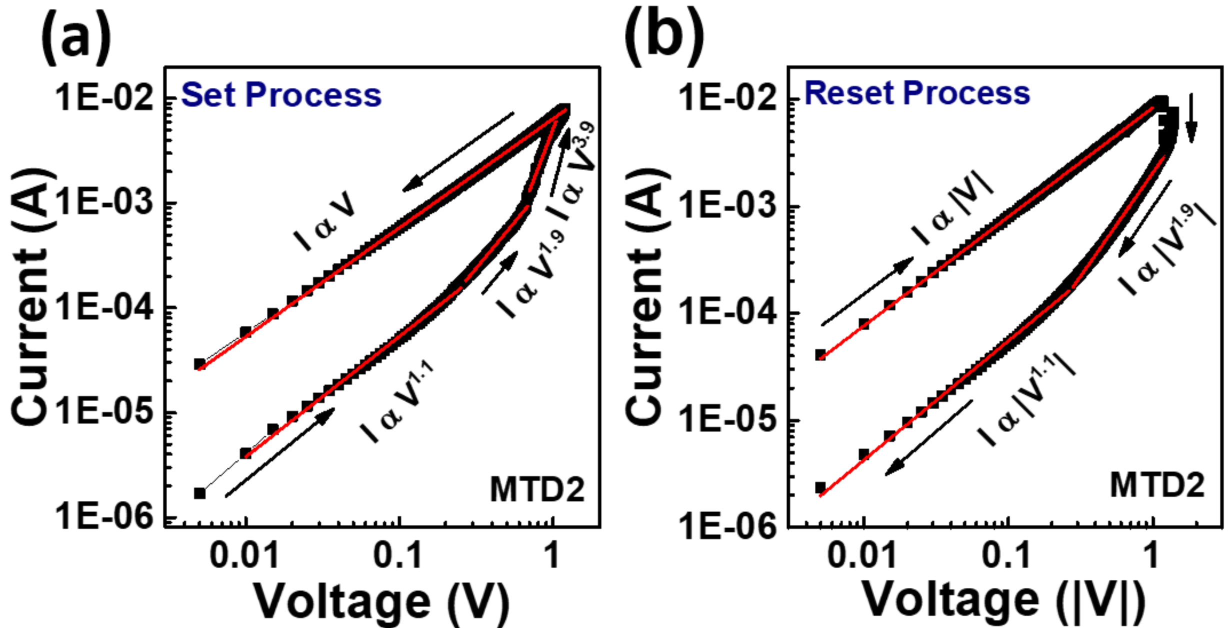
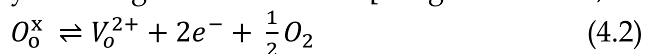


Figure 4.6: (a) The double logarithmic plot of I–V characteristic for positive, and **(b)** for negative voltage to analyze the ohmic and SCLC conduction mechanisms. Red line indicates the curve fitting for ohmic and SCLC conduction.

conduction in the device is due to SCLC. From the mathematical model of SCLC based child's law and conduction mechanism discussed above, the AlO_x can be thought to have trap sites where the injected charges will be trapped and will assist in CF formation. When a positive bias is applied on the TE, the AlO_x will dissociate as $AlO_x \rightarrow Al + O^{2-}$ [Li *et al.*, 2016]. The formation of oxygen vacancies can be illustrated by the Kroger-Vink notation [Kröger and Vink, 1958]:



$$O_o^x \rightleftharpoons V_o^{2+} + 2e^- + \frac{1}{2}O_2 \quad (4.2)$$

where O_o^x is oxygen ion on an oxygen site and is the charged oxygen vacancy. Hence the negatively charged oxygen ions will migrate towards the Ti TE interface functioning like an oxygen reservoir [Lin *et al.*, 2007]. The positively charged OV V_o^{2+}, will act as trap sites for injected charge carriers. The trapped charges inside the oxygen vacancies will assist in CF formation in AlO_x resulting in switching the device from HRS to LRS as shown in Figure 4.7(a). When negative voltage is applied on the TE, the oxygen ions will drift back from Ti-AlO_x interface towards the switching layer to recombine with the oxygen vacancies trapping the injected charges. This will rupture the CF causing the device to reset and switch back to HRS as shown in Figure 4.7(b).

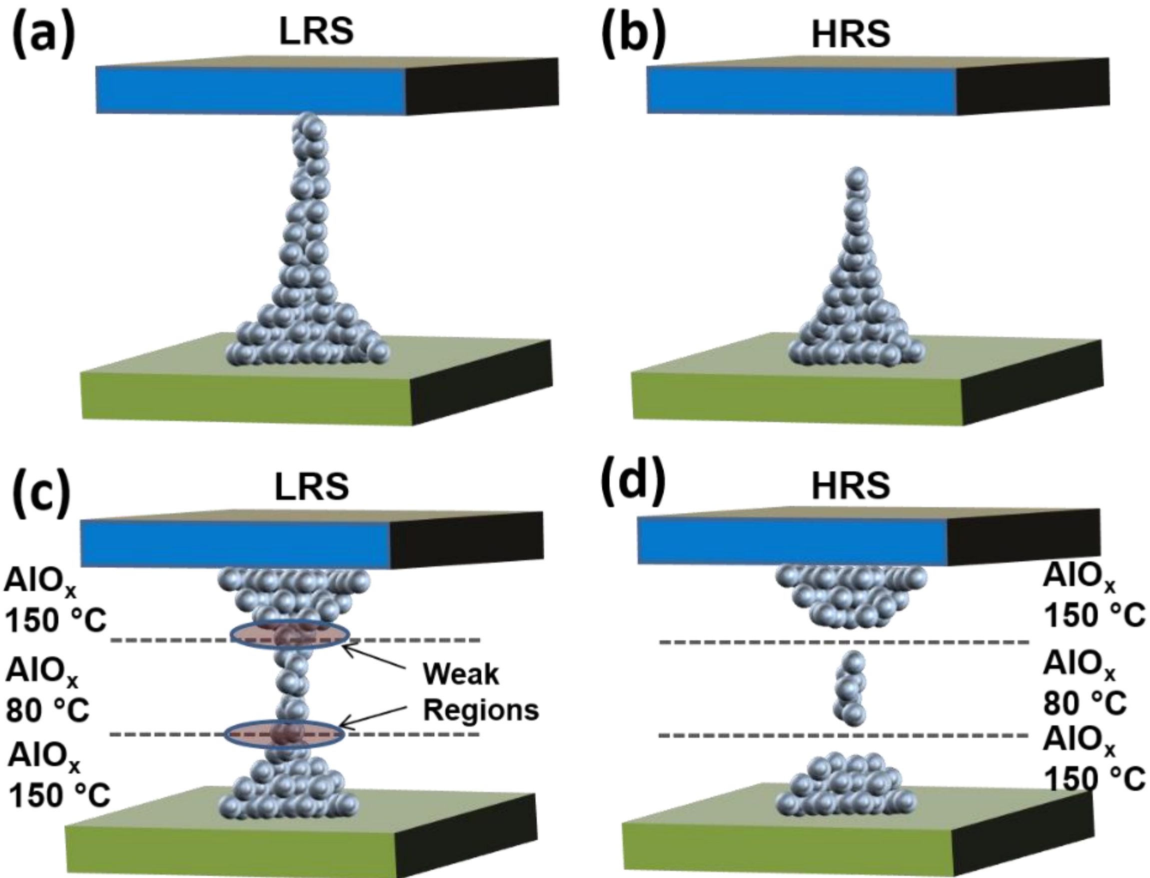


Figure 4.7: (a) and **(b)** Schematic diagram of switching mechanism in STD2, **(c)** and **(d)** for MTD2 devices.

As observed earlier, with lower switching voltages, higher I_{on}/I_{off}, repeatability, reliable and uniform *I-V* characteristics and retention time, MTD2 devices exhibited improved performance in comparison to other type of devices. To ascertain the reasons of improved performance metrics, the switching mechanisms in STD2 and MTD2 devices were investigated. Stoichiometry of ALD AlO_x using TMA and water is largely maintained at deposition temperatures exceeding 200 °C, however a slight stoichiometric imbalance is expected at lower deposition temperatures [Dingemans *et al.*, 2010; Potts *et al.*, 2012; van Hemmen *et al.*, 2007], with decreasing O/Al ratio with increasing deposition temperature. Due to the higher oxygen proportions in the AlO_x films deposited at lower temperature, the film deposited at 80 °C is relatively oxygen rich in comparison to that at 150 °C, which results in relatively higher density of oxygen vacancies in latter case. It should be noted that majority of these vacancies are manifested after application of bias. Density of these vacancies is further increased due to Ti electrodes, which extract larger amount of oxygen ions from 150 °C AlO_x films leading to the generation of large amount of oxygen vacancies at metal insulator interface [Lin *et al.*, 2007]. Due to higher density of oxygen vacancies in the film deposited at 150 °C, the physical dimension of the CF is also expected to be wider [Meng-Han *et al.*, 2010; Park and Lee, 2016] and a reliable operation is expected for this case due to a strong filament formation as shown in Figure 4.7(a).

However, during the reset process, such CFs are difficult to rupture due to their broad dimensions and stability as shown in Figure 4.7(b). Whereas for MTD2 case shown in Figure 4.7(c), the set process creates wider and narrower CFs in the outer and middle layers deposited

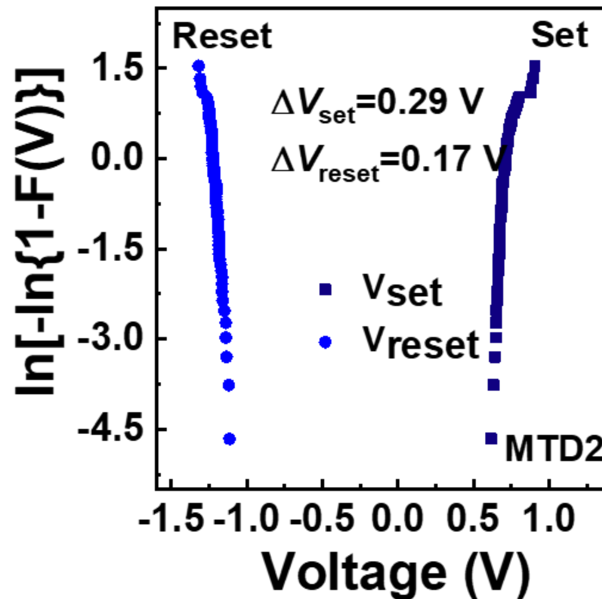


Figure 4.8. Weibull's distribution of set and reset voltages showing marginal variation in V_{set} and V_{reset} and reliable switching operation.

at 150 °C and 80 °C respectively. During the reset process, the CF will be partially ruptured only in the weak regions formed at AlO_x interfaces as shown in Figure 4.7(d), which further assists in the CF regrowth during the subsequent set process. This effective reduction or localization of switching region in the oxygen rich region facilitates the low voltage switching operation in these devices. On the other hand, the switching mechanism in MTD1 devices can be explained in a similar way, where the top and bottom AlO_x layer will have narrow CFs due to higher oxygen concentration and strong CFs in the middle layer. Apart from the comparable mechanism of CF formation as in MTD2 devices, the reset in MTD1 devices will result in complete rupture by the easy dissolution of narrow CFs. This will result in higher switching voltages and poor reliability in the subsequent cycles.

The reliability of MTD2 devices was tested and shown in Figure 4.8 by plotting the V_{set} and V_{reset} voltages as Weibull's cumulative distribution function given by:

$$\ln\left[-\ln\{1-F(V)\}\right] = \beta \ln(V) \quad (4.3)$$

where β is the shape parameter of the distribution [Lawless, 2002]. Weibull's distribution shows a negligible variation of 0.29 V and 0.17 V in V_{set} and V_{reset} respectively over the multiple cycles of operation.

4.5 Conclusion

The multi-temperature deposition schemes for RRAM fabrication and their effect on resistive switching behavior of Ti/AlO_x/Ti devices were discussed. Under proposed scheme, the middle layer of AlO_x was deposited at a lower temperature than that of the outer layers. Among all the explored deposition techniques, MTD2 scheme (with temperature sequence of 150 °C/80 °C/150 °C) has resulted in improved performance in devices with high reliability, higher I_{on}/I_{off}, comparatively low voltage switching operation, repeatability of 75 DC cycles, good uniformity, symmetric *I-V* characteristics, and retention time of over 10^3 s. Conduction mechanism has been found to be ohmic and SCLC and driven by child's law as described by double logarithmic plot of *I-V* curve. The bipolar resistive switching in the devices has been explained with physical model of formation and rupture of CF due to migration of oxygen ions and vacancies. A lower

voltage operation was achieved for MTD2 devices, which was attributed to the localization of switching phenomenon in the region with weaker conductive filament. The proposed multi-temperature deposition can be a potential scheme for the development of high performance and reliable AlO_x based RRAM devices.