Chapter 7

Polymer:2-D Material Composite for High Performance Flexible Devices: Part-II

In the previous chapter, graphene oxide based RRAMs demonstrated excellent memory window and lower switching voltages. However, the high ON current in these devices is still a concern that eventually affects the overall power consumption when we think at the chip level integration. Moreover, performance degradation at higher bending radius in flexible devices provides another scope of improvement. These concerns have been successfully addressed by replacing the graphene oxide with a 2-dimensional transition metal dichalcogenide, the molybdnum disulfide. These devices exhibited ultra low ON current in nano-ampere current range alongwith the excellent bendability to few milimeter bending radii [Varun *et al.*, 2020b].

7.1 INTRODUCTION

The recent rise in demand for flexible, wearable, foldable, lightweight, and transparent electronic gadgets such as displays, watches, radio frequency identification tags, sensors, and mobiles have escalated the need to develop a new class of memory devices [Cai *et al.*, 2016; Lee *et al.*, 2014; Liu *et al.*, 2017]. Resistive switching devices, especially the resistive random access memories (RRAM) have overtaken its rivals owing to its lower power consumption, fast switching speed, miniaturization ability, CMOS compatibility, and highly flexible structure [Bousoulas *et al.*, 2016; Ielmini and Wong, 2018; Nagareddy *et al.*, 2017]. The last decade has been significant for material optimization and performance enhancement for RRAMs; however, the pursuit for a switching layer that can deliver the performance metrics mentioned above simultaneously is still on [Ielmini, 2016; Wang and Yan, 2019]. To achieve a high-performance RRAM device, the resistive switching phenomena has been studied in various class of materials among which metal oxides such as HfO_x, TiO_x, AlO_x, TaO_x, and ZnO, polymer dielectrics like poly(4-vilnylphenol) (PVP), polyvinyl carbazole, polymethyl methacrylate, and polyvinyl alcohol, and low-dimensional materials such as graphene oxide (GO), molybdenum disulfide (MoS_2), reduced GO, tungsten disulfide, and hexagonal boron nitride are the key contributors [Hua *et al.*, 2019; Ielmini, 2016; Jang *et al.*, 2016; Kang *et al.*, 2017; Shi *et al.*, 2018; Wang *et al.*, 2020a]. In recent times, hybrid RRAMs have gained significant attention, mainly due to their reliable and low power switching operations [Nagareddy *et al.*, 2017; Sassine *et al.*, 2019; Varun *et al.*, 2020a]. The term hybrid RRAM is attributed to the non-conventional multilayer structure of the device with either organic polymer composites or metal oxide or both, where metal oxide layer enhances the memory window, and the polymer composite contributes towards improved reliability [Lee *et al.*, 2019b; Sun and Wen, 2019; Zhao *et al.*, 2018b; Zhou *et al.*, 2018]. However, the high ON current in these devices is still a vital issue that must be addressed to make these devices more power-efficient. In the recent times, 2-dimensional (2D) materials have gained tremendous attention and growth owing to their excellent performance in applications not limited to field effect transistors, sensors, photodetectors, non-volatile memories, and solar cells [Bhattacharjee

et al., 2018; Jing *et al.*, 2020; Kumar *et al.*, 2018; Rehman *et al.*, 2016]. MoS_2 among the 2D materials, the first and the most aggressively explored transition metal dichalcogenide and its composites with polymer dielectrics have gained significant attention due to their strength to withstand mechanical stress, strain, and stretchable conditions and these are the essential characteristics for a memristive device to be integrated with a flexible and wearable electronic system [Rehman *et al.*, 2016; Zhao *et al.*, 2018a]. However, the reports on these composite thin films as a switching layer in RRAMs are scarce. Despite exhibiting excellent flexibility, the issue of higher operating voltage and larger ON current persists in these devices that obstruct their path towards a power efficient non-volatile memory device.

In this chapter, we report an ultra-low ON current forming free switching in PVP:MoS_2 composite and HfO_x bilayer flexible hybrid RRAM. The formation of multiple weak conductive filaments (CFs) in the active layer contributed towards keeping the switching currents under remarkably low levels. These devices exhibited a decent 500 cycles of DC endurance with memory window of ~3×10^2, retention time of over 10^4 sec, and set and reset powers (P_{set} and P_{reset}) of 270 nW and 0.1 nW respectively. The higher concentration of MoS_2 in the composite has amplified the leakage current in devices; however, the lower concentration has resulted in low power switching. The flexible devices demonstrated an enhanced and reliable performance under mechanical stress corresponding to bending radius of 2.5 mm and consecutive compressive and tensile strain at same radius for 100 cycles without any significant degradation in the switching performance.

7.2 PREPARATION OF PVP:MOS_2 COMPOSITE & DEVICE FABRICATION

Devices were fabricated on indium doped tin oxide (ITO) coated glass substrates. The ITO substrates were cleaned using ultrasonic bath in isopropyl alcohol (IPA), acetone, and methanol twice for 10 min each and then dried with N_2 blow. A 5 nm thin HfO_x layer was deposited over the ITO bottom electrode (BE) at 100 °C using Savannah S200 atomic layer deposition system with Tetrakis(dimethylamido)hafnium(IV) and water as precursors. MoS_2 was synthesized by hydrothermal method using MoO_3, NaoH, and CH_4N_2S precursors [Nigam *et al.*, 2020]. A composite of 2.5 wt% poly(4-vinylphenol) (PVP) and 1 wt.% MoS_2 was prepared by mixing both in IPA as solvent and the later in 25 %, 50 %, 75 %, and 100 % volume proportion and ultra-sonicated for 30 minutes. This solution was spin-coated at 4000 rpm for 45 seconds over HfO_x and annealed at 60℃ for 1 hour for complete evaporation of solvent, yielding an overall thickness of ~140 nm. A 150 nm thick Ag top electrode (TE) was thermally evaporated and circularly patterned using a shadow mask. The flexible devices were fabricated on 127 µm thick ITO/PET substrates with 25% MoS_2. The device schematic has been shown in Figure 7.1(a). The electrical characterization of devices was carried using Keithley 4200 SCS with biasing at TE and BE kept at ground potential. The topographic analysis of PVP:MoS_2 film was analyzed using scanning electron microscope EVO 18 Special Edition from Carl Zeiss. Moreover, devices were heated for 15 minutes right before the electrical characterization to study the effect of device heating temperature on switching characteristics.

7.3 FILM & ELECTRICAL CHARACTERIZATION OF FLEXIBLE RRAMS

7.3.1 PVP:MOS_2 Film & Material Characterization

Figure 7.1(b) shows the scanning electron microscopy (SEM) image confirming a smooth PVP:MoS_2 film. Figure 7.1(c-d) demonstrates the energy dispersive spectra (EDS) and SEM image of as-deposited MoS_2, substantiates the formation of 2D layered structure. The digital image of flexible devices has been displayed in Figure 7.1(e).

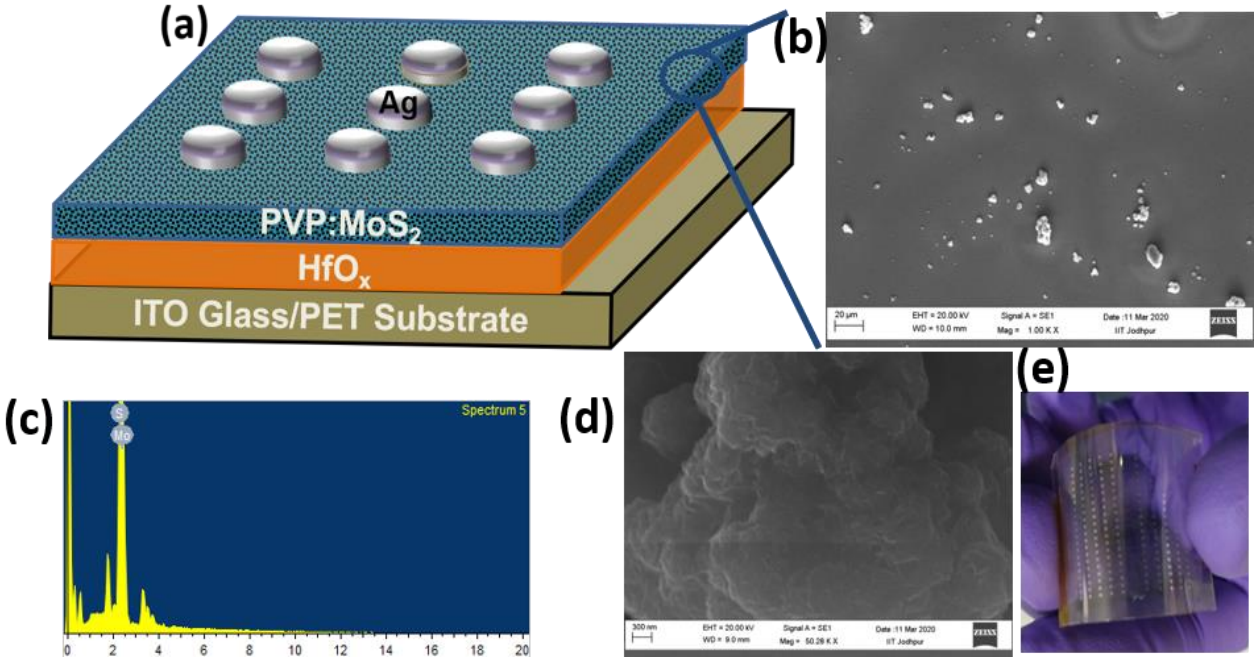

Figure 7.1: (a) Device schematic, **(b)** SEM image of PVP:MoS_2 thin film, **(c-d)** EDS and SEM image of as deposited MoS_2 confirming the layered structure. **(e)** Digital image of the fabricated devices on ITO/PET substrate.

7.3.2 Electrical Characterization & Performance Testing

The switching behavior of the devices was examined while keeping the current limited to 500 nA to prevent the permanent breakdown of devices. The voltage sweep was applied as 0 → V_{max} → 0 to examine the switching behavior of the devices. Figure 7.2(a) demonstrates the switching characteristics of the devices with 25 %, 50%, 75%, and 100% MoS_2 concentration. The 50%, 75%, and 100% MoS_2 devices could not display decent switching behavior and hence were not considered for further examination. Devices with higher MoS_2 concentration, the semiconducting behavior of MoS_2 dominated over the dielectric properties of PVP and HfO_x, and hence the higher leakage current deteriorated the memory window. The 25 % MoS_2 devices exhibited decent switching behavior with remarkably low ON current of 500 nA and V_{set} and V_{reset} of 1.18 V and 0.34 V, respectively. Primarily, the voltage was swept from 0 to 3 V and a sharprise in current was observed at V_{set} = 1.18 V, which confirms the execution of the set process due to the formation of CF between the two electrodes, without any initial forming process. When the bias is swept back to 0 V from 3 V, a gradual fall in current has been observed at V_{reset} = 0.34 V, and the device is again in the HRS state as the device could not hold such a low current of nano ampere range. After reset at 0.34 V, the bias was swept to the negative potential to confirm any switching. The inset of Figure 7.2(a) shows that there is no sign of switching when a negative voltage is applied, and the device remains in the HRS state for 25% MoS_2 devices. Moreover, Figure 7.2(b) shows the DC endurance test of the device for 500 cycles, where they exhibited decent switching behavior with excellent consistency in switching voltages. Figure 7.2(c) displays the variation of current in HRS and LRS at 1 V read voltage for 500 cycles of switching operation with minimal fluctuations and a sufficiently large memory window without any deterioration, pointing towards a reliable and repeatable switching behavior. Furthermore, the devices were tested for even lower current compliances of up to 110 nA where the devices exhibited similar switching performance; however, any variation in HRS and LRS currents was not observed, as displayed in Figure 7.2(d), and hence confirms the ability of devices to perform even a better energy-efficient switching operation. Ultra-low switching current has not affected the device performance, which was further confirmed with retention time measurement shown in Figure 7.3(a), where the HRS and LRS current levels were maintained for 10^4 s at 0.5 V read voltage, without any major fluctuation or degradation in the amplitude.

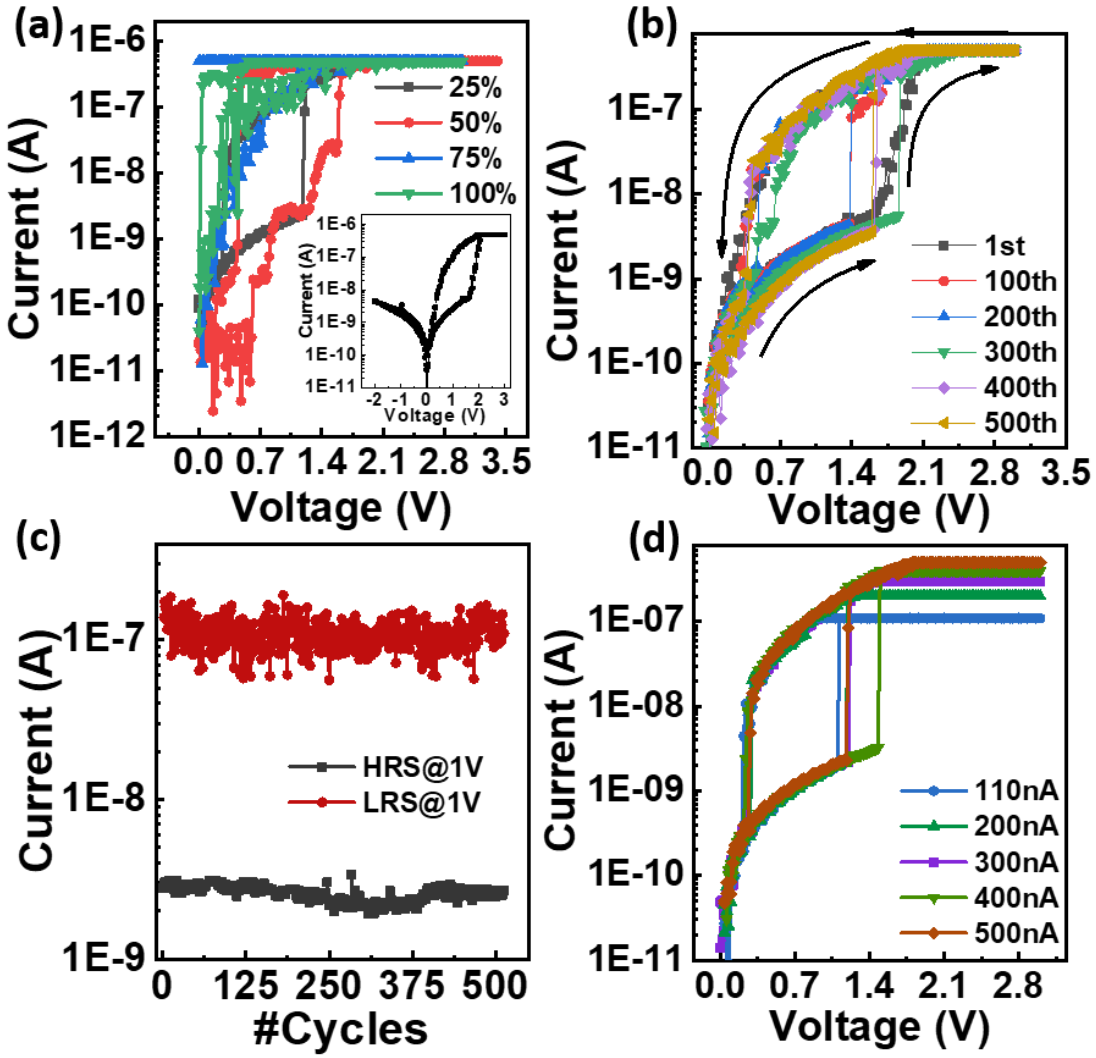

Figure 7.2: (a) Switching behavior of Ag/PVP:MoS2/HfOx/ITO with varied MoS2 concentration in the composite. Inset confirms no switching when negative potential is applied. **(b)** 500 cycles of repeatable switching operation. **(c)** Variation of HRS and LRS current at 1-V read voltage. A clear separation between the two states can be observed with any degradation with cyclic operation. **(d)** Typical I–V characteristics of RRAM device under compliance current (CC) ranging from 110 to 500 nA

A widely accepted tool to examine reliability of electronic devices has been the Weibull distribution:

$$\ln\text{-}\ln(1\text{-}f(y)) = \beta \ln(x) \qquad (1)$$

where β is shape factor. The β value, which is the slop of ln-ln(1-$f(y)$) Vs ln(x) curve, provides an outlook regarding the reliability of a microelectronic system where higher values signify better reliability [Varun *et al.*, 2020a]. Figure 3(a) shows Weibull distribution of V_{set} and V_{reset} of initial 300 cycles of repeatable switching operation. The β of 17 and 9.5 and spread (ΔV) of 0.3 V and 0.5 V in V_{set} and V_{reset} respectively again indicates a reliable switching operation. Figure 7.3(c) and Figure 7.3(d) demonstrates the conduction mechanism in devices using double ln I-ln V curve of Figure 7.2(b) for set and reset process, respectively. For the set process, conduction mechanism for lower voltages (<1) is governed by the ohm's law as curve follows almost a linear relation with voltage ($I \propto V$). This linear relation is attributed to the thermally generated minority charge carriers that currently dominate the injected charges as the trap sites inside the bulk are only partially filled. Once all the trap sites are completely filled, a further increase in potential causes a drastic rise in current confirms the execution of set process. Furthermore, once device is SET, current–voltage curve follows a square law relation ($I \propto V^{1.9}$, child's law) indicating the trap-filled space charge limited conduction (SCLC):

$$J_{sclc} = 9\varepsilon_m \mu \theta V^2 / 8d^3 \qquad (2)$$

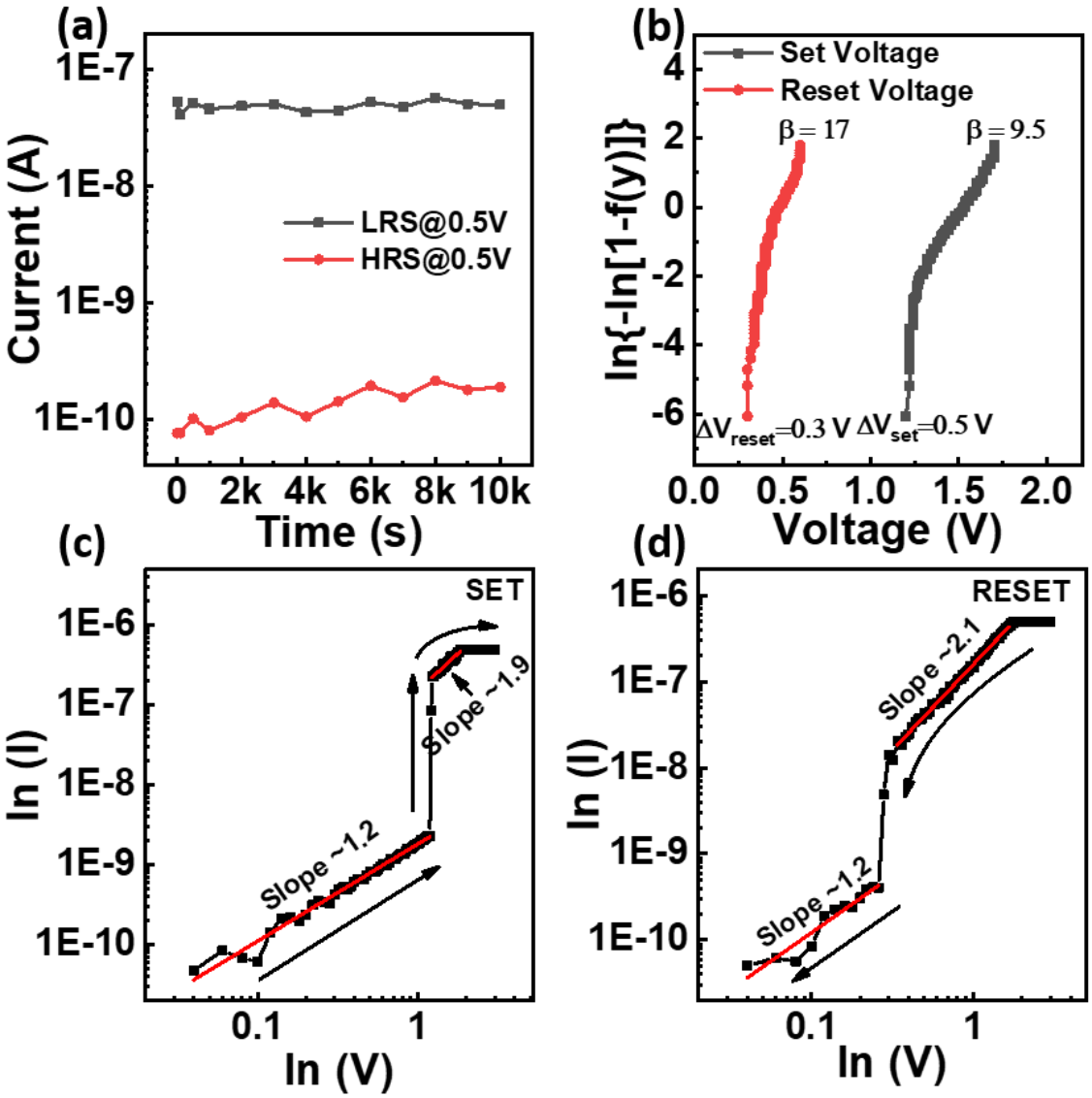

Figure 7.3: (a) Retention time for 104 s at read voltage 0.5 V. **(b)** Reliability analysis of device performance using Weibull's distribution of Vset and Vreset. **(c)** and **(d)** Conduction mechanism explanation in set and reset process using double log I–V characteristics.

where ε_m is the dielectric constant of the material, μ is the mobility of charge carriers, θ is the ratio of free to total carrier density, V the applied bias, and d the separation between two electrodes [Wright, 1961]. The current in this region has been completely controlled by the space charge, limiting the further injection of charge carriers. Similarly, Figure 7.3(d) demonstrates the conduction double log *I-V* curve to study the conduction mechanism in the reset process. Before the reset at V_{reset} = 0.34 V, the square law relation between current-voltage confirms the SCLC with $I \alpha V^{2.1}$ whereas the ohmic conduction dominates after the reset process with current following the voltage linearly.

Figure 7.4(a) demonstrates switching characteristics examined for device heating temperatures ranging from 313 K to 473 K where a decrement in V_{set} and rise in V_{reset} has been observed with increasing temperature. Moreover, Figure 7.4(b) displays the variation of current at 0.5 V with rising temperature that shows a marginal decay in HRS current. In contrast, a sharp fall in LRS current indicates positive temperature coefficient and hence the metallic behavior of CF [Siddiqui *et al.*, 2017].

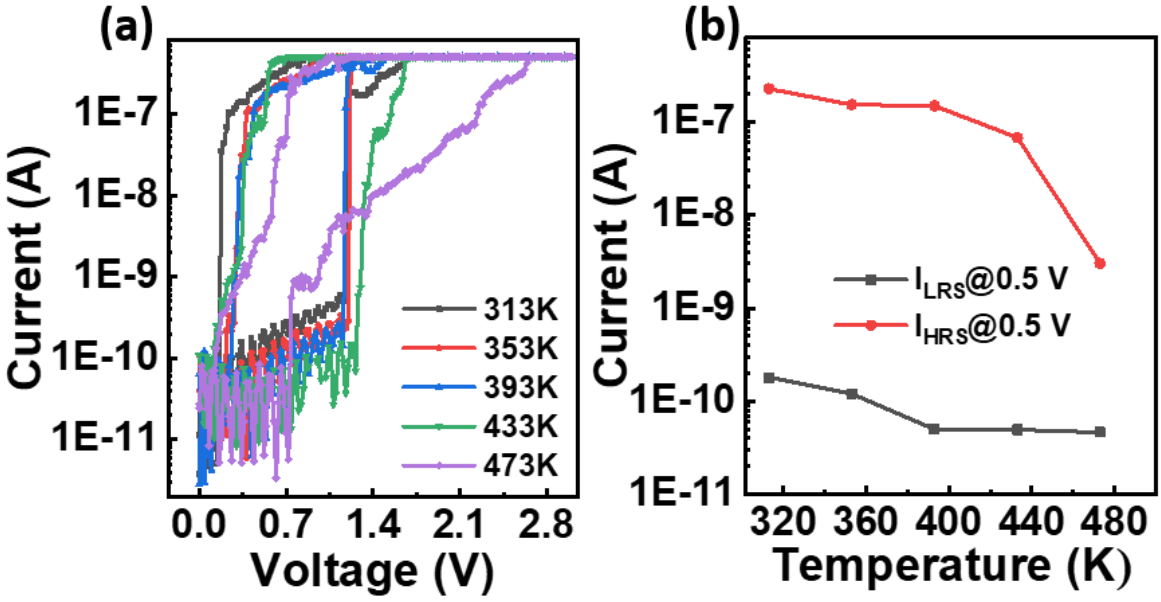

Figure 7.4: (a) and **(b)** Switching behavior after heating for 15 min at different temperatures right before characterization. Current variation in HRS and LRS with rising temperature clearly showing decrement in LRS current with rising temperature. The I–V characteristics were recorded after annealing the sample for 15 min at the respective temperatures.

7.3.3 Flexibility Study Under Various Strain Conditions

The crucial characteristic of a flexible device is its ability to withstand the mechanical stress and strain applied. Here the devices fabricated on the 127 µm thick ITO coated PET substrate were tested for their mechanical strength, initially under cyclic tensile and compressive strain, and then tensile strain at various bending radii. Figure 7.5(a) demonstrates the sequence of the bending cycle for tensile and compressive strain at bending radius ±5 mm for 5 s in each position. The effect of 25, 50, 75, and 100 cycles of cumulative compressive and tensile strain on switching characteristics has been shown in Figure 7.5(b). The major reason behind degradation in memory window or switching failure in flexible devices is the evolution of cracks switching layer and/or in the electrodes. An excellent switching performance with marginal variation in switching voltages and without any spike in the leakage current can be observed with cyclic cumulative tensile stress and strain. The inset of Figure 7.5(b) confirms the generation of cracks on the PVP:MoS_2 surface, thereby degrading the quality and uniformity of the switching layer that eventually affected the switching performance and reliability. Figure 7.5(c) displays the variation of current in HRS and LRS at read voltage 0.5 V against the number of bending cycles, where an excellent memory window is preserved after the 100 bending cycles without any visible degradation. The inset shows nearly similar switching voltage distribution with bending cycles, again confirms a reliable switching behavior. Furthermore, the device's flexibility was tested under extreme tensile strain condition for 15 min with strain 0.5%, 0.84%, 1.27%, 1.58%, and 2.54% at bending radii of 12.5 mm, 7.5 mm, 5 mm, 4 mm, 2.5 mm respectively. The strain % has been calculated using the formula:

$$\text{Strain } (\%) = \frac{d_f + d_s}{2R_{\text{bending}}} \times 100 \qquad (3)$$

where d_f and d_s are the film and substrate thickness, and R_{bending} is bending radius [Zhang *et al.*, 2016]. Figure 7.5(d) demonstrates the switching characteristics of the device at bending radii mentioned above, confirming a decent switching performance while maintaining an excellent memory window till 5 mm. The inset of Figure 7.5(d) displays the digital image of the sample under extreme bending conditions. Figure 7.5(e) displays the distribution of HRS and LRS at 0.5 V read voltage when devices were subjected to extreme bending conditions where a decent switching performance has been demonstrated up to the 4 mm bending radius. However, the degradation in I_{on}/I_{off} to 75 at 2.5 mm radius still confirms the device's ability to withstand

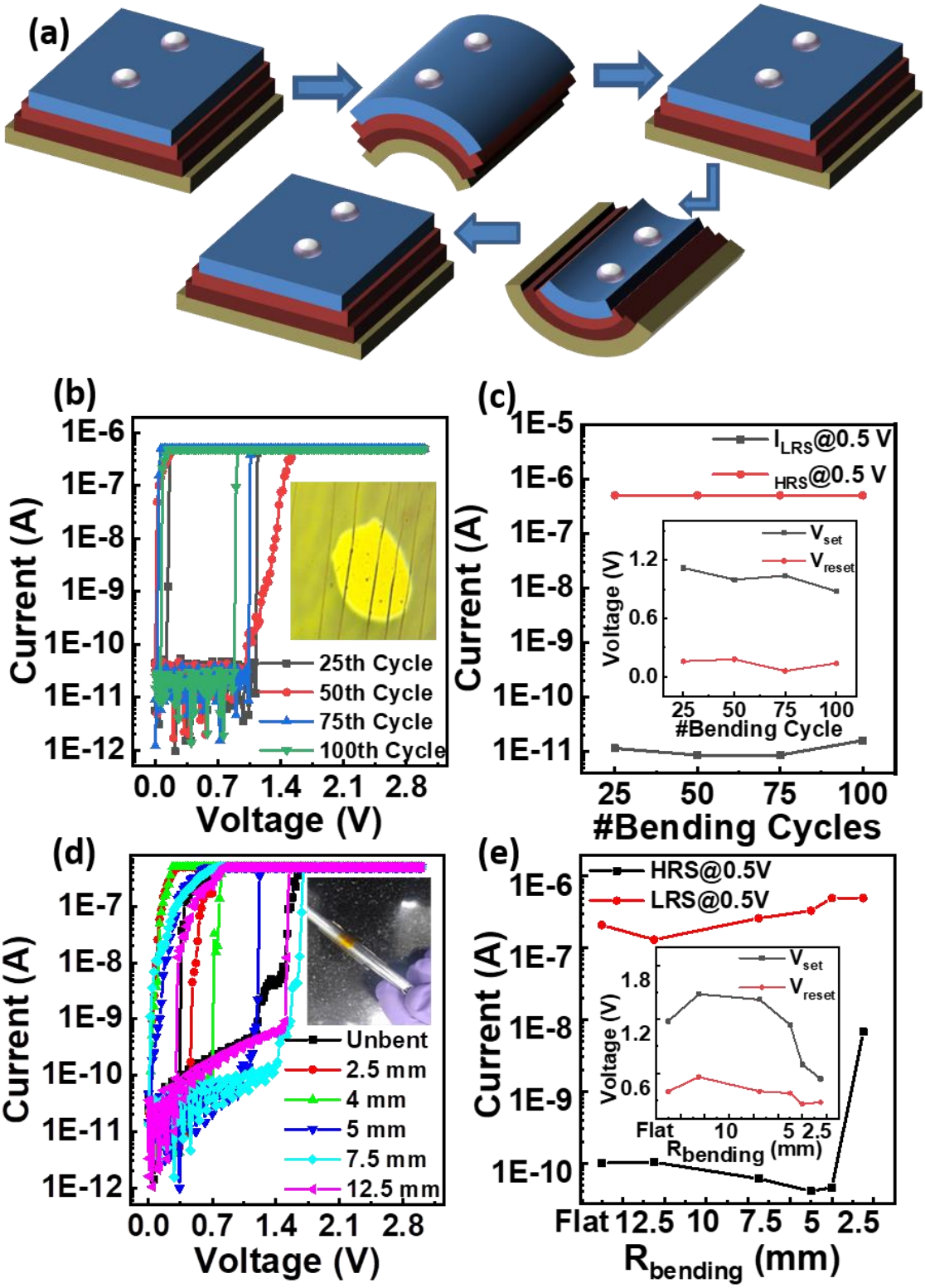

Figure 7.5: **(a)** Sequence of single compressive and tensile strain cycle with bending radius of ±5 mm. **(b)** Digital image of the fabricated devices on ITO/PET substrate. **(c)** I–V characteristics of device after 100 consecutive bending cycles. Inset shows the evolution of cracks on the film and electrodes. **(d)** Variation of current in HRS and LRS at 0.5-V read voltage after 25, 50, 75, and 100 bending cycles, confirming no degradation in the memory window. Inset shows the variation of switching voltages with bending cycles. **(e)** RS performance of device with bending radius ranging from ∞ to 2.5 mm. Inset shows the sample in bent condition. **(f)** Current variation in HRS and LRS at 0.5 V with bending radius. Rise in HRS current at 2.5 mm radius; however, a decent memory window is still preserved. Inset shows the variability of switching voltages against the bending radius.

mechanical strain under extreme bending conditions. The effect of the evolution of cracks in the switching layer surface and at the electrodes is visible in the switching voltage distribution versus the bending radii curve shown in the inset of Figure 7.5(e) where the device maintains the uniformity in V_{set} and V_{reset} till 5 mm bending radius and tends to fluctuate as the radius is further reduced to 4 mm and 2.5 mm. High flexibility in these devices, when subjected to stress and strain, has been attributed to the layer by layer deformation in MoS_2 thin films that results in slow degradation in performance, unlike the metal oxide or polymer films where the breakdown occurs at the bulk level, and suddenly, the device failure happens.

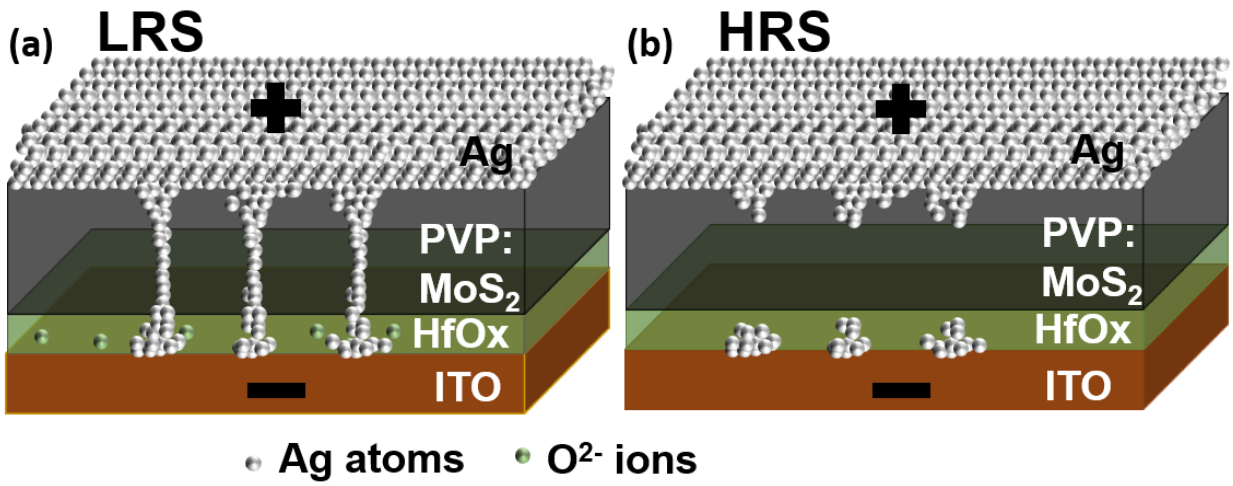

Figure 7.6: (a) Schematic diagrams demonstrating the switching mechanism in LRS and **(b)** HRS demonstrating the formation and rupture of multiple weak CFs of Ag atoms.

Considering the discussion made so far and switching characteristics under various test conditions, it indicates the filament type switching mechanism in these devices. Figure 7.6(a) and (b) demonstrate schematically the switching mechanism where formation and rupture of multiple weak Ag CF between TE and BE by electromigration of Ag atoms, switches the device from HRS to LRS and vice versa. The application of positive bias (0 V to 3V) on TE oxidizes the Ag electrode to Ag^+ ions ($Ag \rightarrow Ag^+ + e^-$), and these ions under the effect of the electric field start migrating towards the BE. At the same time, the electrons injected from the BE starts traversing towards TE. These electrons will reduce the Ag^+ ions to Ag atoms, and the accumulation of Ag atoms at BE will be initiated. As soon as all the Ag^+ ions electromigrated from TE are reduced to Ag atoms, a CF will be formed the two electrodes, and a sharp rise in current will be observed at voltage V_{set}. The device is switched from HRS to LRS, termed as the WRITE operation and set process, as shown in Figure 7.6(a). As reported earlier, the formation of multiple weak nano-sized Ag filaments in the switching layer can be considered as the primary reason for the ultra-low switching current [Hua *et al.*, 2019; Qian *et al.*, 2014]. When the potential is swept back from 3 V to 0 V, the LRS of the device was maintained; however, after a specific voltage V_{reset}, the weak filaments could not sustain between the two electrodes as the strength of filament was not enough to hold such a low on current. The breakage of filament results in a decrement in current that switches the device back to HRS, and the execution of the reset process is confirmed. Such type of reset operation has been earlier explained using the Gibbs-Thomson effect or the Nanobatteries effect also, where the electrochemically active metals such as Ag or Cu based filaments have assisted in switching the device [Hua *et al.*, 2019; Zhang *et al.*, 2016].

Table 7.1 enlists some of the recent reports on power consumption trend in the switching events of an RRAM memory device. This comparison mainly comprises of metal oxides, perovskites, and 2D materials switching layer based memory devices. The switching power has been calculated by considering the current once the set or reset operation is completed. This comparison ascertains the outperformance of Ag/PVP:MoS_2/HfO_x/ITO devices, owing to its ultra-low current and low voltage switching operation.

Table 7.1 Performance comparison of recently reported memory devices in terms of power consumption.

Switching Layer	I_{set}	I_{reset}	P_{set} & P_{reset}	Ref.
TiO_x	5 μA	-1 μA	3 μW, 94 μW	[Qian *et al.*, 2014]
Gd:Ta_2O_5	200 μA	-1.4 μA	~0.4 mW, 0.7 μW	[Shi *et al.*, 2017]
MoS2-PVA	85 μA	~1 μA	255 μW, 3 μW	[Rehman *et al.*, 2016]
$CH_3NH_3PbI_3$	10 mA	-10 mA	12 mW, 32 mW	[Kim *et al.*, 2019a]
HfO_2/MoS_2–Pd	-10 mA	10 mA	0.8 mW, 1 mW	[Wang *et al.*, 2018a]
ZnO	30 μA	-10 μA	9 μW, 20 μW	[Wu *et al.*, 2019]
PVP:MoS_2/HfO_x	500 nA	0.4 nA	0.27 μW, 0.1 nW	This work

7.4 CONCLUSION

In summary, an ultra-low switching current flexible hybrid memory device with PVP:MoS_2/HfO_x switching layer has been presented where different proportions of 1 wt.% MoS_2 was mixed with 2.5 wt%. PVP. The device with a quarter part of MoS_2 mixed with PVP exhibited low current threshold switching and lower power consumption in the nanowatt range, whereas the higher MoS_2 concentration results in higher leakage current and poor memory window. These devices exhibited a decent DC endurance of 500 cycles and maintain a sufficient memory window for 10^4 s of retention time. The *I-V* characteristics and HRS LRS resistances at elevated temperatures confirm the metallic nature of the CF. Weibull's distribution of switching voltages further confirms the reliable switching performance of the device with a comparatively wider distribution of set voltages. The flexible devices fabricated on the PET substrates were subjected to various flexibility tests to study their electromechanical stability. The devices endured the consecutive 100 cycles of tensile and compressive strain at 5 mm bending radius, with similar switching voltages and without any degradation in the memory window. Furthermore, these devices preserved a decent memory window of ~75 when bent to an extreme tensile strain of 2.5 mm radius with the evolution of cracks on the PVP:MoS_2 surface. The low switching current has been attributed to the formation and rupture of multiple weak Ag CFs. Finally, the ultra-low current and low voltage switching operations have been attributed to the formation and rupture of multiple weak Ag CFs. In summary, the hybrid bilayer RRAMs could be an excellent choice for power-efficient and high-performance flexible memory devices.