

List of Figures

Figures	Title	Page
1.1	Memory hierarchy in computer system. As we move up from mechanical drives to CPU registers, the pricing is too high; however, the speed becomes faster. In contrast, as we move down the storage becomes denser and cheaper.	2
1.2	A typical conventional 6T SRAM cell architecture (a) . Schematic diagram of a DRAM cell (b) .	3
1.3	Schematic diagrams demonstrating the Flash memory (a) and SONOS memory cells (b) .	3
1.4	Categorization of standard semiconductor memories and emerging NVM technologies.	4
1.5	(a) Device schematic of a FeRAM device. (b) Development of polarization against the voltage applied across the top and bottom electrode (BE). The positive and negative polarization saturation at positive and negative voltages indicates the '1' and '0' states, respectively.	5
1.6	(a) Device schematic of a STT-MRAM cell. (b) The curve shows the magnetoresistance variation with applied voltage, depending upon the direction of polarization of the bottom ferromagnetic layer with respect to the top.	5
1.7	(a) Device schematic of a PCM cell. (b) Programming scheme of a PCM cell where a transition to amorphous phase happens when a shorter pulse at high temperature is applied that drives the cell to HRS. A longer pulse at low temperature convert the switching layer into crystal phase that switches the cell to LRS.	6
1.8	Schematic diagram of RRAM metal-insulator-metal structure with single switching layer (a) and bi-layer switching layer (b) . Schematic diagram representing current-voltage characteristics of unipolar and bipolar resistive switching.	7
2.1	Schematic demonstrating the resistive switching mechanism with the demonstration of forming, set, and reset processes in a typical bipolar RRAM cell.	13
2.2	Schematic demonstration of unipolar resistive switching using device <i>I-V</i> characteristics.	14
2.3	Typical <i>I-V</i> characteristics of Bipolar resistive switching characteristics in F8 (a) , and cF8 modes (b) .	15
2.4	Switching behavior of a threshold switch demonstrated using typical <i>I-V</i> characteristics indicating the positive and negative threshold switching and threshold voltage V_T and the hold voltage V_H	15
2.5	Schematic demonstration of resistive switching mechanism in a VCRAM.	16
2.6	Demonstration of switching mechanism in a CBRAM device using typical current-voltage characteristics and related movement of ions and atoms during each transition (1-4) between the HRS and LRS.	17
2.7	Schematic diagram of the commonly used RRAM device architectures. (a) The BE is common to every cell and the switching layer and TEs were patterned. (b) Cross-point structure provides the isolation between each device with separate bottom and TEs. (c) Cross-bar structure forms multiple cross-point cells interconnected to each other, providing higher device density and advantage of 3D architecture fabrication.	19
2.8	(a) Displays endurance test using the continuous <i>I-V</i> sweep method for 100 cycles in ITO based RRAM device. (b) Demonstration of pulsed voltage stress method for endurance test using the voltage pulse shown in the inset.	20
2.9	The retention time measurement of ITO based RRAM for 10^4 s at 125°C .	21
2.10	(a) Schematic diagram of setup for high-speed switching measurements. (b) Switching speed of a Ti/HfO _x (Ar plasma treated)/Pt RRAM device using a voltage pulse.	21
2.11	(a) Histogram formation for forming voltage distribution of 100 W/Al ₂ O ₃ /TaO _x /TiN RRAM devices. (b) Cumulative probability distribution of IRS, LRS, and HRS for 100 W/Al ₂ O ₃ /TaO _x /TiN RRAM devices. Weibull's distribution of V_{set} and V_{reset} of initial 200 cycles for Ag/PVP:GO/HfO _x /ITO RRAM devices.	22
2.12	(a) X-HRTEM image of TiN/Ta ₂ O ₅ /Ta/TaN RRAM devices on 5 nm scale. (b) Reset voltage variation with TaO _x thickness with increasing targeted HRS resistance. (c) Pulse endurance characteristics of TaO _x based device with varied thickness.	23
3.1	(a) Schematic diagram shows one complete cycle of atomic layer deposition.	27
3.2	(a) Savannah S-200 ALD system from Cambridge nanotech used for research. (b) Schematic demonstrating the design of a process flow of ALD.	28

3.3	(a) Schematic demonstration of spin coating process. (b) WS-650 MHz-BNPP/LITE spin coating system from Laurell used in experiments.	29
3.4	(a) Schematic demonstration of thermal/e-beam evaporation process. (b) SC-Triaxis physical vapor deposition system from Semicore used for this research.	30
3.5	(a) Schematic diagram of surface profiler scanning the line profile using the stylus. (b) Digital image of DektakXT surface profiler system from Bruker.	31
3.6	(a) Working principle explanation of the AFM. (b) Digital image of the XE-70 AFM from Park Systems used in this research.	31
3.7	(a) Schematic representation of SEM with an electron gun, condenser lens, scanning and deflection coils as the main components. (b) EVO-18 special edition SEM from Carl Zeiss used in this research for surface and compositional characterizations.	32
3.8	(a) Schematic representation of the working principle of UV-visible spectrometer. (b) Lambda 750 UV-visible spectrometer by Perkin Elmer used in this characterization.	33
3.9	(a) Schematic demonstration of FTIR working principle. (b) FT-IR Spectrum 2 from Perkin Elmer used in this research.	34
3.10	(a) Instrumental schematic of Raman spectroscopy. (b) STR 500 Raman spectrometer by Airix Corp used in this research.	35
3.11	(a) 4200-SCS from Keithley used for electrical characterization of RRAM devices. (b) PM-5 probe station from Cascade Microtech used for housing and probing sample during electrical characterization.	36
3.12	(a) Switching characteristics of RRAM device with V_{set} and V_{reset} of 0.6 V and -2.78 V, respectively. (d) Shows the DC endurance (repeatability) successfully exhibiting 800 cycles of switching operation.	36
4.1	(a-d) AFM images of STD1, MTD1, MTD2, and STD2, respectively, demonstrating surface roughness of each film.	40
4.2	(a-d) Schematic representation of AlO _x based RRAM devices fabricated with four different deposition schemes.	42
4.3	I-V characteristic of devices showing resistive switching behavior of (a) STD1, (b) STD2, (c) MTD1, and (d) MTD2 schemes respectively. Inset of Figure 4.3(a) showing the DC endurance test of STD1 device exhibiting 12 cycle of repeatable operation.	43
4.4	Data retention properties of (a) STD1, (b) STD2, (c) MTD1, and (d) MTD2 devices measured at 0.1 V read voltage.	44
4.5	(a) I-V characteristic of MTD2 RRAM device over 75 cycles of operation, showing typical bipolar resistive behavior. Inset shows the forming process in the device with forming voltage of $V_f = 6.45$ V and (b) displaying the variation in resistance of device in HRS and LRS (DC endurance test) at read voltage of 0.1 V. Separation of 16 Ω is maintained throughout the operation of 75 DC cycles.	45
4.6	(a) The double logarithmic plot of I-V characteristic for positive, and (b) for negative voltage to analyze the ohmic and SCLC conduction mechanisms. Red line indicates the curve fitting for ohmic and SCLC conduction.	45
4.7	(a) and (b) Schematic diagram of switching mechanism in STD2, (c) and (d) for MTD2 devices.	46
4.8	Weibull's distribution of set and reset voltages showing marginal variation in V_{set} and V_{reset} and reliable switching operation.	47
5.1	(a) Device schematic with thicknesses of respective layers, (b) X-FESEM image of PVP/HfO _x /ITO, (c-e) AFM image of 2.5 wt.%, 3.5 wt.%, and 4.5 wt.% PVP film with scan area of $5 \times 5 \mu\text{m}^2$ showing RMS roughness of 3.05 nm, 1.33 nm, 0.42 nm respectively, and (f-h) shows the corresponding line profiles of encircled region indicating pinhole formation with depth of ~42 nm and ~13.5 nm at x and y locations respectively in 2.5 wt.%, ~4.2 nm in 3.5 wt.%, and ~1.6 nm in 4.5 wt.% respectively.	51
5.2	(a) I-V curve showing switching behavior of CBRAM device. Inset shows the forming process at $V_f = 1.94$ V in 2.5 wt.% device and $V_f = 2.58$ V in 3.5 wt.% device. Also, the I-V curve of 4.5 wt.% is shown in inset demonstrating no resistive switching till 12 V. (b) 300 cycles of repeatable switching operation, (c) variation in V_{set} and V_{reset} , and (d) switching parameters of 10 devices illustrating the device-to-device variability.	52
5.3	(a) Plot of Retention time measurement by applying read voltages of -0.2 V and 0.2 V in HRS and LRS respectively, showing retention time of 72000 sec without degradation in current levels, (b) AC endurance of device showing the capability to withstand continuous switching for more than 2000 cycles. (c) Weibull's distribution for reliability test of the	53

	CBRAM device, and (d) double log I-V curve showing ohmic and TF-SCLS conduction mechanisms.	
5.4	(a) Schematic illustrating the device structure with pinholes in PVP layer filled with Ag. (b)(i) Oxidation of Ag to Ag ⁺ ions and diffusion of Ag ⁺ ions into PVP layer through the pinholes, (ii) reduction of Ag ⁺ ions to Ag atoms and formation of CF by Ag atoms. (c) On reversal of bias polarity, electrochemical joule-heating assisted rupture in CF at the pinholes tip due to high current density and electric field concentration.	54
6.1	(a) Device schematic and fabrication process of each layer with their processing conditions, (b-e) AFM images of Dev.A, Dev.B, Dev.C, Dev.D respectively with 2μm × 2μm scan area representing the root mean square roughness of each sample.	59
6.2	(a) The Raman spectroscopy of PVP:GO with different GO concentrations indicating the presence of signature D and G bands of GO at 1338 cm ⁻¹ and 1612 cm ⁻¹ alongwith the four peaks of PVP, (b) FTIR spectroscopy of PVP:GO film with different GO concentrations indicating different functional groups attached GO sheets and PVP, (c) the FESEM topography of PVP:GO composite over HfO _x film, and (d) the UV-visible spectroscopy of 1 mg/ml GO solution. Inset shows the molecular structure of GO with different functional groups attached.	60
6.3	(a) Displays I-V characteristics of a device of all the four samples with different GO concentration, (b) retention time characteristics showing the I _{on} /I _{off} of all samples. This confirms degradation on I _{on} /I _{off} after initial I-V cycles, (c) switching characteristics of Dev.B with V _{set} and V _{reset} of 0.64 V and -2.42 V respectively, and (d) shows the DC endurance (repeatability) of Dev.B successfully exhibiting 800 cycles of switching operation.	62
6.4	(a) The variation of HRS and LRS current at 0.2 V read voltage. A visible rise in HRS current after 400 cycles is observed, (b) AC endurance with test -4 V/2 V pulse and 20 ms width was performed to continuously turn on and off the device, (c) reliability of the device was examined with weibull's distribution of first 200 cycles showing shape factor of 6 and 4.7 for V _{reset} and V _{set} distribution, and (d) a similar reliability study with distribution of I _{set} and I _{reset} at 0.2 V read voltage.	63
6.5	(a) V _{reset} and V _{set} data of 17 devices fabricated on Dev.B sample displaying 100% device yield, (b,c) logI-logV curve of switching characteristics to study the conduction mechanism in positive and negative voltages. The slops in regions A, B, C, and D shows ohmic and SCL conduction mechanisms governing during set and reset process.	64
6.6	(a) Demonstration of switching characteristics after bending the device with bending radius ranging from 12.5 mm to 2.5 mm. Inset shows the digital image in bent condition, (b) variation of current at 0.2 V read voltage in HRS and LRS at different bending radius with failure at 2.5 mm radius. Inset shows the digital image of cracks evolved at ITO surface after bending and ITO in the unbent condition. (c) Variation in V _{set} , V _{reset} , and I _{on} /I _{off} with bending condition varying from unbent to 2.5 mm radius.	65
6.7	(a) The sequence of single tensile stress and strain cycle with bending radius of ±5 mm, (b) I-V characteristics of device after the test for 150 cycles. Inset shows the digital image of fabricated sample, (c) retention characteristics upto 10 ⁴ s at 0.2 V in LRS and -0.2 V in HRS. Inset shows the variation in HRS and LRS current at 0.2 V read voltage with number of bending cycles. (d) Variation in V _{set} , V _{reset} , and I _{on} /I _{off} with 150 bending cycles at 5 mm radius.	66
7.1	(a) Device schematic, (b) SEM image of PVP:MoS ₂ thin film, (c-d) EDS and SEM image of as deposited MoS ₂ confirming the layered structure. (e) Digital image of the fabricated devices on ITO/PET substrate.	71
7.2	(a) Switching behavior of Ag/PVP:MoS ₂ /HfO _x /ITO with varied MoS ₂ concentration in the composite. Inset confirms no switching when negative potential is applied. (b) 500 cycles of repeatable switching operation. (c) Variation of HRS and LRS current at 1-V read voltage. A clear separation between the two states can be observed with any degradation with cyclic operation. (d) Typical I-V characteristics of RRAM device under compliance current (CC) ranging from 110 to 500 nA.	72
7.3	(a) Retention time for 10 ⁴ s at read voltage 0.5 V. (b) Reliability analysis of device performance using Weibull's distribution of V _{set} and V _{reset} . (c) and (d) Conduction mechanism explanation in set and reset process using double log I-V characteristics.	73
7.4	(a) and (b) Switching behavior after heating for 15 min at different temperatures right before characterization. Current variation in HRS and LRS with rising temperature clearly showing decrement in LRS current with rising temperature. The I-V characteristics were recorded after annealing the sample for 15 min at the respective temperatures.	74

- 7.5 (a) Sequence of single compressive and tensile strain cycle with bending radius of ± 5 mm. (b) Digital image of the fabricated devices on ITO/PET substrate. (c) I–V characteristics of device after 100 consecutive bending cycles. Inset shows the evolution of cracks on the film and electrodes. (d) Variation of current in HRS and LRS at 0.5-V read voltage after 25, 50, 75, and 100 bending cycles, confirming no degradation in the memory window. Inset shows the variation of switching voltages with bending cycles. (e) RS performance of device with bending radius ranging from ∞ to 2.5 mm. Inset shows the sample in bent condition. (f) Current variation in HRS and LRS at 0.5 V with bending radius. Rise in HRS current at 2.5 mm radius; however, a decent memory window is still preserved. Inset shows the variability of switching voltages against the bending radius. 75
- 7.6 (a) Schematic diagrams demonstrating the switching mechanism in LRS and (b) HRS demonstrating the formation and rupture of multiple weak CFs of Ag atoms. 76