7

Adaptive-SMC based Output Impedance Shaping in DC Microgrids Affected by Inverter Load

In the previous chapter, an robust primary and secondary control was presented to handle uncertain operating condition. In this chapter a adaptive sliding mode control is presented to regulate the output impedance of the interfacing converter. The proposed control is designed using local parameters. This simplifies the design process. The robust primary impedance control is integrated with a dynamic consensus based secondary control, which provides adequate voltage reference to achieve proportional load sharing.

A microgrid consists of distributed generation units, energy storages, dc and ac loads, interconnected through dc and ac power converters to a common dc bus. In a DC Microgrid, proportional load sharing among sources and dc bus voltage regulation is important. When a single-phase AC load is connected to the DC Microgrid, the dc bus voltage and source current oscillate at twice the ac supply frequency f_{ac}. The voltage magnitude of the dc bus is tightly controlled to be within the regulation limits. This leads to larger $2f_{ac}$ oscillations in inverter input current than the dc bus voltage. This oscillating input current is called second order ripple currents SRCs. In distributed power generation environment like microgrid, the SRC distribution among sources is affected by the line impedance of the cable connecting the source converter to the dc bus.

The SRCs have various detrimental effects on the power quality, efficiency, and component's reliability. The SRC, when propagates to the PV source, causes a rise in its temperature Kim *et al.* [2013]. The SRCs affect maximum power point tracking (MPPT) mechanism Liu *et al.* [2014]. In the case of wind turbines, SRCs lead to ripple torque in it Xia *et al.* [2011]. In terms of energy storage, batteries such as Valve Regulated Lead Acid (VRLA), Vented Lead Acid (VLA), Lithium-ion, and Nickel Cadmium (Ni-Cd) are used. All types of batteries heat up when ripple currents are drawn from it. This results in degradation of battery and affects its performance in the long run.

In terms of SRC absorption capacity, different sources and, storages have different ability to cater to the ripple current demand. A photovoltaic cell is more affected by the SRCs than the wind turbines as in wind turbines ripple in torque can be reduced using adequate speed control gears Parker *et al.* [2016]. In terms of wind turbines, Vertical Axis Wind Turbines (VAWTs) are more affected than a Horizontal Axis Wind Turbines (HAWTs)Xia *et al.* [2011]. In terms of batteries, Ni-Cd batteries have a relatively lesser rise in temperature compared to the lead-acid batteries when ripple currents are drawn from it IEE [2006]; siz [2016]. Hence, different sources and storages can be made to share the different magnitude of SRCs. Along with this, in literature, different active and passive filters have been proposed to absorb ripple current Vitorino *et al.* [2017]. In a microgrid, all source nodes may not consist of such filters, instead, the ripple should be propagated to the nodes having ripple filters. This will reduce the component count and cost of the microgrid.

Several methodologies have been proposed to reduce SRC propagation in two-stage dc-ac inverters in literature. In active control methodologies, linear controllers are used to increase the output impedance at $2f_{ac}$. Based on the virtual impedance based SRC reduction approaches,

methods such as Bandpass Filter Inserted Current Feedback Scheme (BPF-ICFS), Notch Filter Inserted Load Current Feedforward Scheme (NF-LCFFS),Notch Filter and Virtual Resistance Load Current Feedforward Schem (NF+VR-LCFFS) exist as discussed in Zhang *et al.* [2018b], and references therein. The virtual impedance control methodologies for SRC suppression is proposed in Yang *et al.* [2017]; Zhang *et al.* [2014]; Zhu *et al.* [2015]. In these methods, the inductor current is fedback to the control loop through a bandpass or double bandpass filter to improve dynamics and reduce SRCs. However, such methodologies are good for single converters. The distributed control environment in DC Microgrid requires robust controller which is capable of sharing dc load proportionally and reduce or manage SRC at the same time. The dc bus voltage must also be within permissible limits. The ripple sharing technique proposed in Hamzeh *et al.* [2015] shares ripple according to the converter's rated power, however, it may lead to source heating or source failure. An active filter is proposed in Kyritsis *et al.* [2008] to reduce SRCs to PV sources. However, there is an increase in device count, which further increases the cost of the system. It will be beneficial if such active filters are installed at a node, and SRCs from all other nodes is propagated to this ripple absorbing node which works as a centralized ripple energy storage node as in Shen *et al.* [2017]. This will lead to an increase in the energy density of the active filter. In Jia *et al.* [2017b], virtual impedance is introduced using a linear control and ripple is managed according to the state of charge (SoC) of battery. However, the load current is not shared proportionally. In terms of multiple ac loads, the SRCs reflected in the dc side can be reduced by the introduction of adequate phase shift in carriers of the parallel-connected inverters. In Krein *et al.* [2012], authors use phase shifting in carriers to absorb the ripple energy in an extra ripple port, however, such configuration requires extra elements to reduce ripple and for an unknown number of VSCs finding the phase shift angle may not be feasible. In Siva Prasad and Narayanan [2014] and Zhang *et al.* [2011] it is recommended that to operate parallel inverters with reduced ripple, there should be $2\pi/\mathrm{N}$ angle between carrier signals for N inverters. Hence, for ripple cancellation with phase shift, the number of inverters must be known before-hand.

This chapter proposes a non-linear sliding mode control based SRC sharing methodology, such that along with the dc component of current, the second-order current is also shared. The SRC is shared irrespective of the interfacing converter ratings. By using the proposed ASMC-OIS control, the output impedance of the converter is increased at twice the ac supply frequency as shown in Figure 7.1. This leads to reduction of ripple current propagating through the converter. Instead it is programmably shared among the nodes having some ripple filtering circuits or to the dc link capacitor. The secondary consensus control is used to incorporate proportional load sharing by dynamic droop control. A sparse communication network is used for per unit load current data exchange between the neighboring control nodes. The communication topology may not be similar to the physical interconnection topology. The salient features of the proposed control are:

1) The output impedance of converter is increased at $2f_{ac}$ using ASMC-OIS. The proposed control is robust against modeling uncertainties.

2) The proposed controller is fully distributed in nature. The proposed control is capable mitigating the SRC and proportional current sharing is achieved at the same time.

3) SRC sharing does not affect proportional dc load sharing among sources. This makes the proposed control applicable to dc and hybrid microgrid.

The chapter is organized as follows: Section 7.1 consists of the analysis of ripple sharing among converters. Section 7.2 consists of an explanation of the proposed control law. The bounds on the controller variables are derived in this section. A small-signal analysis of output impedance shaping is presented in Section 7.3. In Section 7.4, the stability of the system is analyzed using Lyapunov's approach. The secondary consensus control is presented in Section 7.5. Sections 7.6 and 7.7 consists of simulation and experimental verification of the proposed controller,

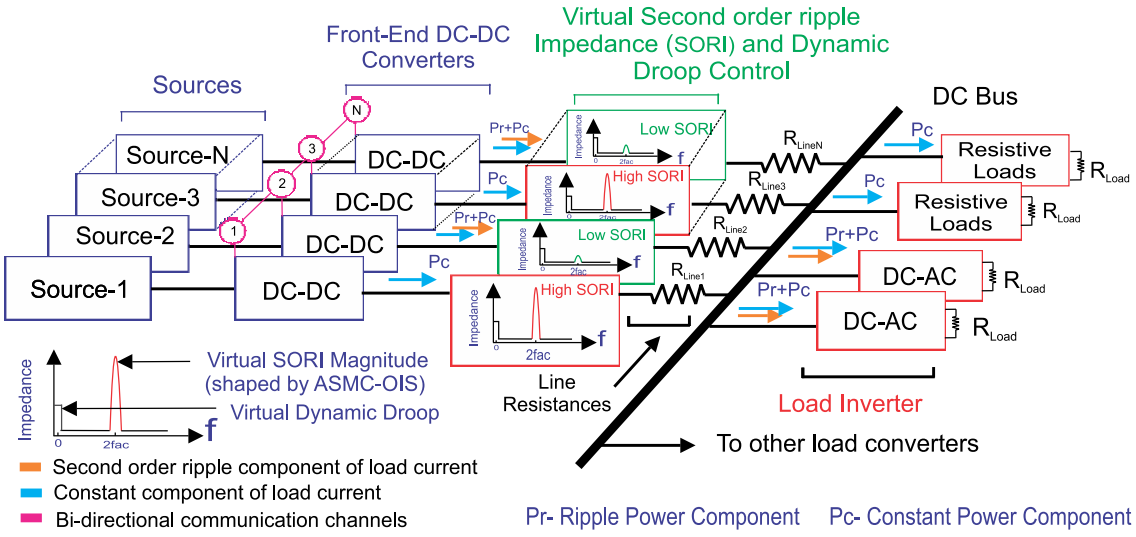

Figure 7.1 : Proposed power sharing scheme: High and low impedance at $2f_{ac}$ is achieved by output impedance shaping

respectively.

7.1 SECOND ORDER RIPPLE SHARING

The instantaneous output power of a single-phase inverter consists of a constant component P_c and a ripple component P_r. The output power P_{ac} = V_{ac} I_{ac}

$$V_{ac}I_{ac} = V_m cos(\omega t) I_m cos(\omega t) \tag{7.1a}$$

On further expanding above equation and dividing power into the constant dc component P_c and ripple component P_r:

$$P_{ac} = \frac{1}{2}V_m I_m + \frac{1}{2}V_m I_m cos(2\omega t) = P_c + P_r \tag{7.1b}$$

This ripple power has to be shared by N parallel connected interfacing converters.

$$(P_{c1} + P_{r1}) + .. + (P_{cn} + P_{rn}) = \frac{1}{2}V_m I_m + \frac{1}{2}V_m I_m cos(2\omega t) \tag{7.1c}$$

where, $P_{ci} = V_{dc}I_{ci}$ is constant power component and $P_{ri} = V_{dc}I_{ri}$ is ripple power component supplied by i^{th} converter, where I_{ci} is constant component and I_{ri} is ripple component of load current respectively. By separating the constant and ripple components and substitute $V_m = V_{dc}$ and normalizing by a suitable base current value I_b so as to obtain per unit current $I_{ci}^{pu} = \frac{I_{ci}}{Ib}, I_{ri}^{pu} = \frac{I_{ri}}{Ib}, I_{mi}^{pu} = \frac{I_{mi}}{Ib}$:

Let

$$\gamma_1 = \frac{I_{r1}^{pu}}{I_m^{pu}} \qquad \gamma_2 = \frac{I_{r2}^{pu}}{I_m^{pu}} \quad ... \qquad \gamma_n = \frac{I_{rn}^{pu}}{I_m^{pu}}$$

$$\gamma_1 + \gamma_2 + ...\gamma_n = \frac{1}{2}cos(2\omega t) = \sum_{i=1}^{N}\gamma_i = \frac{1}{2}cos(2\omega t) \tag{7.1d}$$

If the SRC of first converter is controlled, the γ_1 would tend to be 0.

$$\sum_{i=2}^{N} \gamma_i = \frac{1}{2} cos(2\omega t) \tag{7.1e}$$

Hence, all γ_i's has to increase to satisfy the above equation, and ripple sharing is achieved.

7.2 PROPOSED CONTROL METHODOLOGY

A decentralized ASMC-OIS methodology is proposed to implement ripple sharing and proportional sharing of dc component of load current. In this, the primary control consists of adaptive sliding mode control (SMC). It is responsible for maintaining a constant dc bus voltage, and ripple control. The ripple is controlled by increasing the output impedance at $2f_{ac}$ frequency. A dynamic consensus-based secondary control adjusts the voltage reference for proportional current sharing among all sources as shown in Figure 7.3. The per unit load of each converter is communicated to its neighboring converters. The proposed control methodology is explained in the following subsections:

7.2.1 Model of i^{th} boost converter in error co-ordinates

The state space average model of i^{th} boost converter connected to a dc bus can be written as:

$$L_i \dot{i}_{Li} = -r_{L_i} i_{Li} - (1-u_i) v_{ci} + V_{dci} \tag{7.2a}$$

$$C_i \dot{v}_{ci} = (1-u_i) i_{Li} - I_{oi} - \sum_{j \varepsilon N_i} I_{ij}$$

where, L_i, C_i is the inductor and terminal capacitance of i^{th} converter, u_i is the duty cycle, V_{dci} is supply voltage, r_{L_i} is inductor resistance. In 7.2a, substitute the value of $i_{Li} = (e_{ii} + I_i^{ref})$ and $v_{ci} = (e_{vi} + V_i^{ref})$ to obtain the dynamics in error co-ordinates as:

$$L_i \dot{e}_{ii} = -r_{L_i}(e_{ii} + I_i^{ref}) - (1-u_i)(e_{vi} + V_i^{ref}) + V_{dci} \tag{7.2b}$$

$$C_i \dot{e}_{vi} = (1-u_i)(e_{ii} + I_i^{ref}) - I_{oi} - \sum_{j \varepsilon N_i} I_{ij}$$

where,$e_{vi} = v_{ci} - V_i^{ref}$, $e_{ii} = i_{Li} - I_i^{ref}$, I_{o_i} is the output terminal current, V_i^{ref}, and I_i^{ref} are voltage and current references, v_{ci} is output voltage, I_{Li} is inductor current. The equations in error dynamics are used to design the control law. The voltage reference consists of a global desired dc bus value. This reference is common to all converters connected to the dc bus. The voltage reference is changed depending on the desired voltage regulation to implement droop for load sharing.

7.2.2 Sliding Mode Control based Adaptive Voltage Control

The primary controller consists of individual sliding mode controllers that receive voltage references from the secondary controller. The switching function is adaptive in nature as in Gautam *et al.* [2018]. However, an additional control parameter ρ_i has been used to increase $2f_{ac}$ impedance. The proposed switching function for i^{th} converter is:

$$s_i = \rho_i (i_{Li} - I_i^{ref}) + \alpha_i (v_{ci} - V_i^{ref}) = \rho_i e_{ii} + \alpha_i e_{vi}, \tag{7.3a}$$

$$V_i^{ref} = V_o^{ref} + k_i I_i^{\bar{p}u} I_r - d_i I_i,\ \alpha_i = \eta_i (v_{ci} - V_i^{ref})^{\beta_i}$$
$$d_i = d_o + g_i \int (I_i^{pu} - I_i^{\bar{p}u})$$

The variables β_i, ρ_i and η_i are positive constants, $I_i^{\bar{p}u}$ is average microgrid load, I_i is the load current

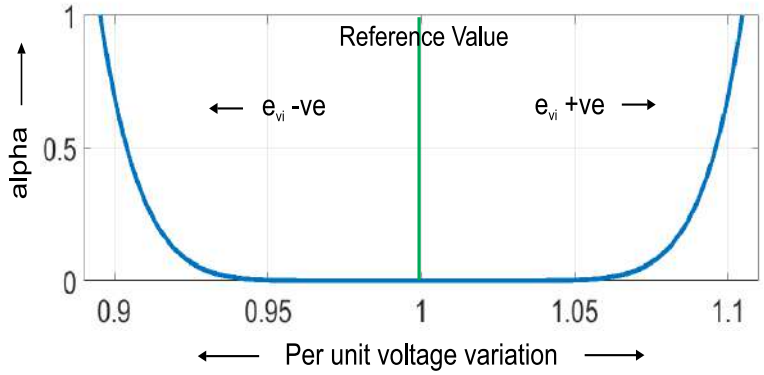

Figure 7.2 : Variation of alpha with voltage error

of i^{th} converter and I_r is its current rating. The parameter d_i is dynamic droop, d_o is constant droop and g_i is dynamic droop gain. These are used to control the dynamics of individual converter. The controller is in voltage control mode, when the voltage error finite. When the voltage error becomes negligible, the control shifts to the current regulating mode. The parameter α_i is responsible for maintaining dc bus voltage, while the component ρ_i is used to increase the output impedance. The profile of α variation with respect to the per-unit variation of converter's output voltage with V^{ref} = 150V, η=10^{-8}, β = 6, and output voltage variation of $\pm$ 5% of the reference voltage is shown in Figure 7.2. The parameter α is designed be zero when the output voltage is at $\pm$ 5 % of the reference voltage, and finite otherwise. This means that when the voltage is outside the voltage regulation range, the sliding surface primarily consists of voltage error component, while when the voltage error is negligible the surface consist of current error term. In (7.3a), the constant k_i is a positive constant and its limits are derived as in Anand *et al.* [2013] and d_i is the dynamic droop, derived in Section 7.5.

7.2.3 Control Law

To ensure that the dynamics reach the sliding surface, the time differentiation of sliding surface should be Edwards and Spurgeon [1998]:

$$\dot{s}_i = -\Gamma_i s_i - Q_i sgn(s_i)\ \ \Gamma_i \ and\ Q_i\ \varepsilon\ \mathbb{R}^{(+)} \tag{7.3b}$$

Also, from (7.3a), the time differentiation of sliding surface is:

$$\dot{s}_i = \rho_i \dot{e}_{ii} + \alpha_i \dot{e}_{vi} + \dot{\alpha}_i e_{vi} = \rho_i \dot{e}_{ii} + \alpha_i (\beta_i + 1)\dot{e}_{vi} \tag{7.3c}$$

Equate (7.3b) and (7.3c) and substitue values from (7.2b) to solve for the control law,

$$(1 - u_i) = \left(\frac{\alpha_i \mu_i (I_{oi} + \sum I_{ij}) + \rho_i r_{Li} (e_{ii} + I_i^{ref}) - \rho_i V_{dci}}{\alpha_i \mu_i (e_{ii} + I_i^{ref}) - \rho_i (e_{vi} + V_i^{ref})} \right) \tag{7.3d}$$
$$- \left(\frac{L_i (\Gamma_i s_i + Q_i sgn(s_i)}{\alpha_i \mu_i (e_{ii} + I_i^{ref}) - \rho_i (e_{vi} + V_i^{ref})} \right)$$

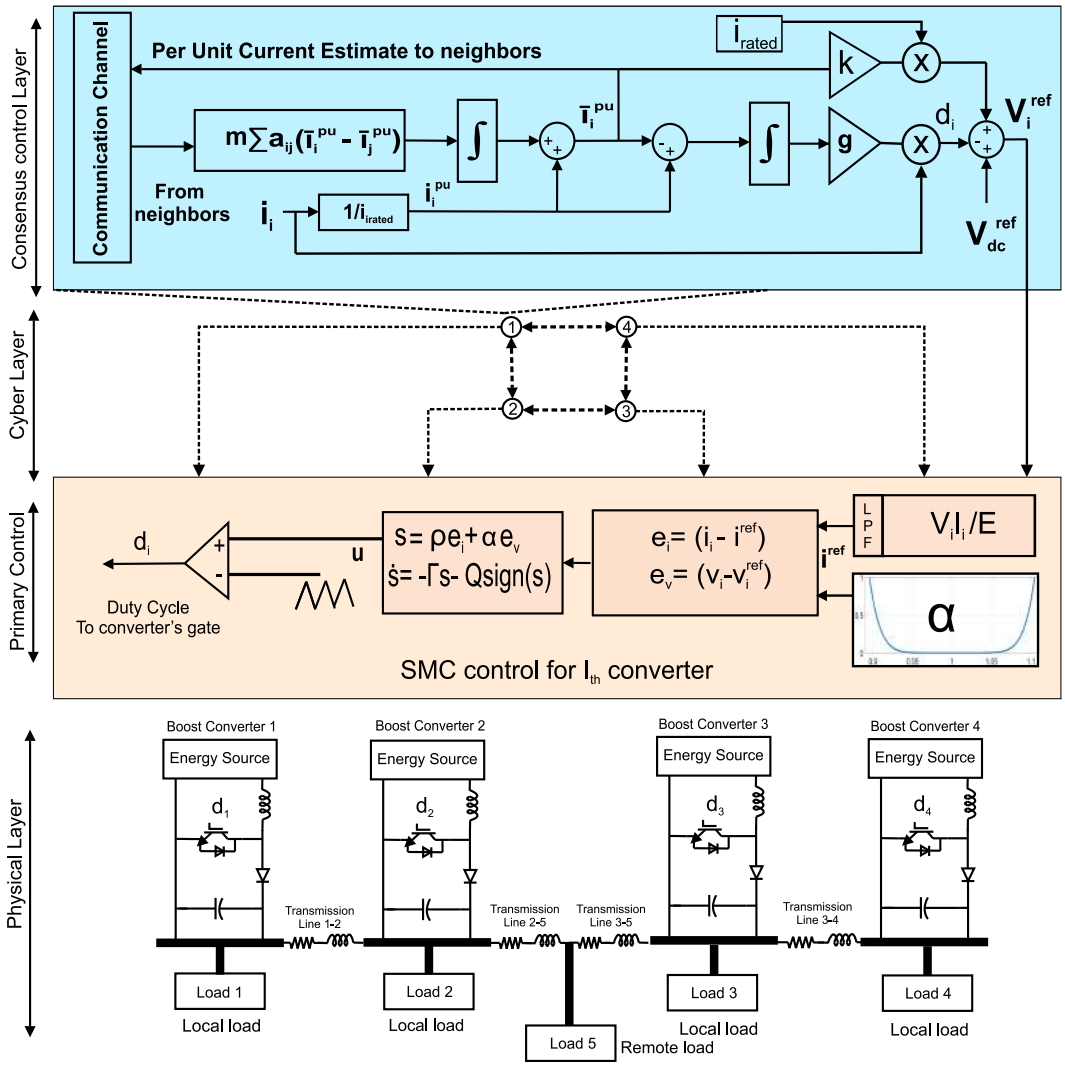

Figure 7.3 : Proposed Control Strategy with Primary and Secondary Control layers

where, $\mu_i = \frac{L_i(\beta_i+1)}{C_i}$ From (7.3d) it is observed that branch currents affect the duty value however, branch current is limited by secondary control that maintains a maximum voltage difference between any two nodes i.e. $(V_i - V_j) \leq \varepsilon_{vLim}$.

7.2.4 Bounds and selection of the control parameters

For proper operation of controller, the limits of the value of α must be defined. On the sliding surface, $s = 0$ and hence, $e_{ii} = -\frac{\alpha_i}{\rho_i} e_{vi}$ On sliding surface the control law, the second term of (7.3d) goes to zero.

Substitute, $r_{Li} = 0$ for simplicity. Also, $(I_{oi} + \sum I_{ij}) = \frac{e_{vi}+V_i^{ref}}{Z_o}$. The steady state duty cycle $D_o = (1 - \frac{V_{dci}}{V_i^{ref}}) = (1 - \frac{V_i^{ref}}{Z_o I_i^{ref}})$. Substitute these values in (7.3d) and divide numerator and denominator by ρ_i:

$$(1-u_i) = \left(\frac{-(\alpha_i/\rho_i)\mu_i(\frac{e_{vi}+V_i^{ref}}{Z_o}) + V_i^{ref}(1-D_o)}{(e_{vi}+V_i^{ref}) + (\alpha_i/\rho_i)^2 \mu_i e_{vi} - (\alpha_i/\rho_i) I_i^{ref}} \right) \tag{7.4a}$$

Now, club all the known constants to a single one,

$$\kappa_i = (\alpha_i/\rho_i) \quad \lambda_1 = (\kappa_i \mu_i / Z_o)$$

$$\lambda_2 = (V^{ref} - \kappa_i \mu_i I_i^{ref}) \quad \lambda_3 = (1 + \kappa_i^2)$$

Substitute above values to (7.4a) :

$$(1-u_i) = \left(\frac{(1-D_o)\lambda_2 - \lambda_1 e_{vi}}{\lambda_3 e_{vi} + \lambda_2} \right) \tag{7.4b}$$

Now, the value of $(1-u_i)$ remains within 0 and 1 i.e. $0 < (1-u_i) < 1$, so the range of κ_i is derived to be:

$$\frac{V_i^{ref}}{I_i^{ref}\mu_i} < \kappa_i < \frac{D_o V_i^{ref}}{\mu_i (D_o I_i^{ref} + \varepsilon_1)} \tag{7.4c}$$

To select α value, take value of ρ to be unity. Corresponding to this value, the output impedance is maximum. The output impedance is maximum as the current error term e_{ii} in the surface is unity. Corresponding to this value find out the value of α using the bounds defined above. Once α is obtained, the parameter ρ is varied below unity to obtain higher or lower output impedance. When the value of ρ is reduced, the current error term e_{ii} in the surface (7.3a). Hence, output impedance is regulated.

7.2.5 Existence of sliding mode

Existence of sliding mode is guaranteed by η - reachability condition as Edwards and Spurgeon [1998]:

$$s_i \dot{s}_i < \eta |s_i| \qquad \eta > 0 \tag{7.5a}$$

from (7.3b),

$$s_i \dot{s}_i = s_i(-\Gamma_i s_i - Q_i sgn(s_i))$$

$$s_i \dot{s}_i = (-\Gamma_i |s_i| - Q_i)|s_i| \qquad s_i sgn(s_i) = |s_i|$$

As, Γ_i and Q_i are both chosen to be negative hence, $(-\Gamma_i|s_i| - Q_i) < \eta$ and hence the reachability condition is satisfied and sliding mode exists. To reduce the effect of chattering, a constant plus proportional rate reaching law 7.3b is used. Here, the value of Q will regulate the chattering such that lower value of Q will lead to longer reaching time while a higher value of Q leads to severe chattering. Hence, a value of Q is chosen so as to reduce chattering as well as have acceptable reaching time. The parameter Γ is used to add a proportional rate term such that higher the value, faster will be the rate of reaching to the surface Hung *et al.* [1993].

7.3 SMALL SIGNAL OUTPUT IMPEDANCE ANALYSIS

The variation of output impedance with control parameters is analyzed by small signal modelling around some operating point. The output impedance analysis presented here is similar to the one proposed in Spiazzi and Mattavelli [2002]. The small signal averaged model of a converter with state variables at operating point is derived as:

$$x_i = [I_{Li} \;\; V_{ci} \;\; I_i^{ref}], \;\; \dot{I_i^{ref}} = \frac{1}{\tau_i}(I_{Li} - I_i^{ref}) \tag{7.6a}$$

Consider small perturbations:

$$\hat{x_i} = [\hat{i_{Li}} \;\; \hat{v_{ci}} \;\; \hat{i_i^{ref}}] \tag{7.6b}$$

The state space small signal model becomes, To reduce order of system, substitute the equation corresponding to i_i^{ref} in terms of other two state variables when $s(\hat{x}) = 0$, i.e.

$$\hat{i_i^{ref}} = \frac{\rho_i \hat{i_{Li}} + \alpha_i \hat{v_{ci}}}{\rho_i} \tag{7.6c}$$

The reduced small signal model in terms of $\hat{i_{Li}}$ and $\hat{v_{ci}}$ becomes,

$$x_{\hat{R}i} = [\hat{i_{Li}} \;\; \hat{v_{ci}}] \quad \dot{x_{\hat{R}i}} = A_R x_{\hat{R}i} + B_R \hat{v_{dci}} \tag{7.6d}$$

The output impedance, $\frac{\hat{v_{ci}}}{\hat{i_{Li}}}$ is derived to be,

$$\frac{\hat{v_{ci}}}{\hat{i_{Li}}} = \frac{sL_i}{(1-u_i)^2} + \frac{m_3 m_1}{(1-u_i)(s^2 - m_4 s - m_3 m_2)} \tag{7.6e}$$

$$m_1 = -m_3, m_2 = \frac{-\alpha_i u_i(\tau_i - C_i R_L + \tau_i(\beta_i + C_i^2 + \beta_i C_i^2)}{K\tau_i}$$

$$m_3 = \frac{-\rho_i u_i^2 R_L}{K}, m_4 = \frac{\rho_i u_i \tau_i C_i^2 - \alpha_i L_i + \rho u_i \tau_i}{K\tau_i}$$

$$K = \alpha_i(L_i + \beta_i L_i) - \rho_i C_i u_i R_L$$

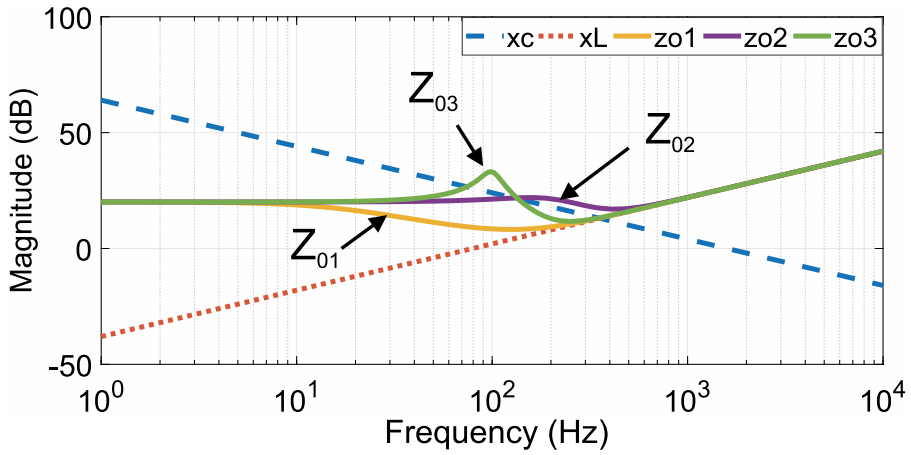

Figure 7.4 : Frequency response of X_c, X_L and Z_o with impedance shaping, $\rho_3 > \rho_2 > \rho_1$ and $Z_{o3} > Z_{o2} > Z_{o1}, Z_{o1}$ is impedance without control

The impedance of bus capacitance X_c is higher than the impedance of converter's input inductor X_L at $2f_{ac}$ as shown in Figure 7.4. Due to this the SRC propagates to the source rather than being absorbed by bus capacitor. To mitigate SRC propogation through the converter, the impedance of inductor is virtually increased at $2f_{ac}$.

7.4 STABILITY OF PROPOSED CONTROLLER

In this section, the stability of the proposed ASMC-OIS control will be analyzed using Lyapunov approach. Let us choose a Lyapunov function consisting of voltage error e_{vi}. During sliding mode, s = 0 or $e_{ii} = -(\alpha_i/\rho_i)e_{vi}$ also, total current output of a converter $I_{oi} = (e_{vi} - V_i^{ref})/Z_i$, where Z_i is the load impedance as seen by i^{th} converter. As output voltage becomes equal to the reference voltage, the e_{vi} converges to zero. The convergence of e_{vi} to zero leads to the convergence of current e_i to zero. The current reference can furthur be simplified as $I_i^{ref} = V_i^{ref}/(Z_i(1 - D_{oi}))$, where duty cycle $D_{oi} = 1 - (V_{dci}/V_i^{ref})$, also $u_i = 1 - (V_{dci}/V_i)$. Consider the following Lyapunov function for N converter system as shown in Figure 7.5 :

$$V = \frac{e_{v1}^2}{2} + \frac{e_{v2}^2}{2} + \frac{e_{v3}^2}{2} + ... + \frac{e_{vn}^2}{2} \tag{7.7a}$$

differentiate above equation with respect to time,

$$\dot{V} = \dot{e_{v1}} e_{v1} + \dot{e_{v2}} e_{v2} + ... + \dot{e_{vn}} e_{vn} \tag{7.7b}$$

For stability $\dot{V} < 0$.

$$\dot{V} = \dot{V}_1 + \dot{V}_2 + ... + + \dot{V}_n \tag{7.7c}$$

where, V_i is Lyapunov function for i^{th} node such that i=1,2,..n.

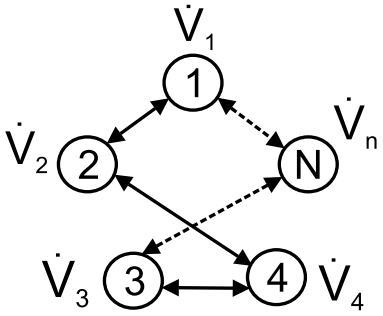

Figure 7.5 : Stability analysis of voltage variation at N converter nodes

On substituting the value of e_{vi} and $\dot{e_{vi}}$ from (7.2b) , the value of Lyapunov function $\dot{V_n}$ at n^{th} node becomes:

$$\dot{V_n} = \dot{V_a} + \dot{V_b} \tag{7.7d}$$

$$\dot{V_a} = \frac{-e_{vn}^2}{C_n}\left((1-u_n)\alpha_n + \frac{1}{Z_{on}}\right) - e_{vn}\frac{V_n^{ref}}{Z_{on}}\left(1 - \frac{(1-u_n)}{(1-D_{on})}\right) \tag{7.7e}$$

$$\dot{V_b} = -e_{vn}\sum_{j\varepsilon N_1} I_{1n} \tag{7.7f}$$

Negative definite V_a

In this section V_a is proved to be negative definite. The first term of V_a is negative definite as the value of $(1-u_n)$ remains within zero and one. Also, C_n and Z_{on} are positive constants. The control variable for dc bus control is also a positive constant. The next term of V_a consists of ratio $(1-u_n)$ and $(1-D_{on})$. In case of some voltage error e_{vn} , $(1-u_n) > (1-D_{on})$ for $e_{vn} > 0$, and $(1-u_n) < (1-D_{on})$ for $e_{vn} < 0$. This makes the second term negative denite Gautam *et al.* [2018]. Hence, overall V_a will always be negative definite.

Negative definite V_b

The V_b term in above equations depends on the branch circulating current among converters.

$$\dot{V_b} = -e_{v1}\sum_{j\varepsilon N_1} I_{1j} - e_{v2}\sum_{j\varepsilon N_2} I_{2j} \ldots - e_{vn}\sum_{j\varepsilon N_n} I_{nj} \tag{7.7g}$$

The branch current between i^{th} and j^{th} node will be :

$$I_{ij} = \frac{V_i - V_j}{r_{ij}} = \frac{\varepsilon_{vLim}}{r_{ij}}$$

where, ε_{vLim} is the maximum voltage difference between any two nodes.

$$\dot{V}_b = -\sum_{n=1}^{N}\left(\sum_{m=1,m\neq n}^{N} e_{vn}\left(\frac{V_n - V_m}{r_{nm}}\right)\right) \tag{7.7h}$$

for simplicity consider all line resistance between two nodes be r. The mean of all the node voltages will be (or the voltage at the dc bus is) :

$$\bar{V} = \frac{(V_1 + ... + V_n)}{N} = \sum_{i=1,i\neq j}^{N} V_i = N\bar{V} - V_j; \qquad j = 1..n \tag{7.7i}$$

Substitute in (7.7h)

$$\dot{V}_b = -\sum_{n=1}^{N} e_{vn}\left(\frac{(N-1)V_n - (N)\bar{V}}{r}\right) \tag{7.7j}$$

The maximum allowable deviation is ε_{vLim} as discussed earlier. This voltage deviation varies as the voltage error varies, as the voltage reference to each converter is the desired dc bus voltage which is $\bar{V}$. Hence, (7.7j) reduces to,

$$\dot{V}_b = -\sum_{n=1}^{N} e_{vn}\left(\frac{e_{vn}}{r}\right) \tag{7.7k}$$

Hence, $\dot{V}_b$ is negative definite. Also, V_a has been proved to be negative definite. As a result of this, $\sum_{i=1}^{N}\dot{V}$ in (7.7c) is negative definite. Hence, the proposed control methodology is stable. The proposed control methodology is shown in Figure 7.3. Futhur in multi-agent sense the stability can be analyzed as in Cucuzzella *et al.* [2018]. The overall microgrid system and the sliding surface can be written as:

$$L\dot{I}_L = -R_L I_L - U.V_c + Vdc \tag{7.7l}$$

$$C\dot{V}_c = U.I_L - GZ^{-1}G^T V_c - I_{Ld}$$

$$S = \rho(I_L - I_{ref}) + \alpha(V_c - V_{ref}) \tag{7.7m}$$

where, inductor current I_L=$[i_{L1},...,i_{Ln}]^T$, terminal voltage V_c=$[v_c1,...,v_{cn}]^T$, inductor resistance R_L=diag $[r_{L1},....,r_{Ln}]$, inductance L=diag $[L_1,....,L_n]$, capacitance C=diag $[C_1,....,C_n]$, V_{dc}=$[v_{dc1},...,v_{dc2}]^T$, control law U=$[(1-u_1),...,(1-u_n)]^T$, control parameter ρ=diag$[\rho_1,...,\rho_n]$, load current I_{Ld}=diag$[i_{Ld1},...,i_{Ldn}]$, load impedance Z=diag$[z_{o1},...z_{on}]$, reference current I_{ref}=diag$[i_{ref1},..,i_{refn}]$, reference voltage V_{ref}=diag$[v_{ref1},...,v_{refn}]$, α=diag$\alpha_1,...,\alpha_n$ and G is the incidence matrix of network topology. Linearize (7.7l) around (I_{ref}, V_{ref}),

$$L\dot{\hat{I}}_L = -R_L(I_L - I_{ref}) - (U - U_{ref}).V_c + U_{ref}(V_c - V_{ref}) \tag{7.7n}$$

$$C\dot{\hat{V}}_c = (U - U_{ref}).I_{ref} + U_{ref}(I_L - I_{ref}) - GZ^{-1}G^T(V_c - V_{ref})$$

When the dynamics are on sliding surface then, S=0 and $\dot{S}$=0, which implies that,

$$\rho(I_L - I_{ref}) + \alpha(V_c - V_{ref}) = 0 \tag{7.7o}$$

$$\rho(\dot{I}_L) + \alpha(\beta + 1)(\dot{V}_c) = 0 \tag{7.7p}$$

Substitute values from (7.7n) to (7.7p) and simplify to obtain U as,

$$U = U_{ref} + M_1^{-1}\Bigg((C^{-1}\alpha(\beta+1)(U_{ref}.\hat{I_L} + GZ^{-1}G^T\hat{V}_c) \tag{7.7q}$$

$$-L^{-1}\rho(R_L\hat{I_L} + U_{ref}.\hat{V}_c)\Bigg)$$

where, $M_1 = \left(V_{ref}L^{-1}\rho - C^{-1}\alpha(\beta+1)I_{ref}\right)^{-1}$

In above equation, $\hat{I_L} = (I_L - I_{ref})$, $\hat{V}_c = (V_c - V_{ref})$. The U obtained in (7.7q) is the equivalent control matrix. Now, substitute the value of U from (7.7q) to (7.7l), and use (7.7o) to reduce the order of system and simplify,

$$C\dot{\hat{V}_c} = \Bigg(U_{ref}.\alpha\rho^{-1}(1_n + C^{-1}\alpha(\beta+1)) - I_{ref}M_1^{-1}L^{-1} \tag{7.7r}$$

$$(R_L\alpha + U_{ref}.\rho) + GZ^{-1}G^T(C^{-1}\alpha(\beta+1) - 1_n)\Bigg)\hat{V}_c = M\hat{V}_c$$

Now, let the Lyapunov function be $V = \hat{V_c}^T\hat{V}_c$, for stability, $\dot{V} < 0$, hence, $\hat{V}_c^T\hat{V}_c + \hat{V}_c^T\hat{V}_c < 0$. Hence, to ensure stability, the matrix M must be designed to be sufficiently negative so as to ensure $M + M^T < 0$ Cucuzzella *et al.* [2018].

7.5 PROPORTIONAL CURRENT SHARING

A DC Microgrid is usually designed so that the sources share load in proportional to their rating Augustine *et al.* [2015]. In this section, a distributed consensus based control is proposed by means of which the converters at different nodes communicate their per unit load current values with their neighbors to reach consensus in per unit load sharing.

7.5.1 Dynamic consensus control

Each converter's controller is connected to a cyber layer (responsible for data exchange between nodes) which may not be similar to the physical layer (electrical connections between nodes). The p.u. current values received from neighbors are averaged and the current reference is estimated for droop calculations. The final per unit loading of all converters must reach a consensus Olfati-Saber and Murray [2004]. A reduced order communication is used for data exchange between the nodes. In this, the data is exchanged only between neighboring nodes.

To estimate average current for j^{th} converter :

$$\bar{I}_j^{pu} = I_j^{pu} + \int \sum_{i=1}^{N} m a_{ij}(\bar{I}_i^{pu} - \bar{I}_j^{pu}) \tag{7.8a}$$

where, a_{ij} is an element of adjacency matrix of the communication topology and m is a positive constant, $\bar{I}_j^{pu}$ is the per unit microgrid loading estimated by j^{th} converter, I_j^{pu} is the per unit load of j^{th} converter, $\bar{I}_j^{pu}$ is the per unit microgrid loading estimated by neighbors of j^{th} converter.

$$I_j^{pu} = I_{cj}^{pu} + I_{rj}^{pu}cos(2\omega t), \quad \bar{I}_j^{pu} = I_{cj}^{pu} \tag{7.8b}$$

Where, I_{cj}^{pu} is the per unit dc component of j^{th} converter, and I_{rj}^{pu} is per unit ripple current of j^{th} converter. The converter's current is written in vector form as:

$$I^{pu} = [I_1^{pu}, I_2^{pu}, .., I_n^{pu}]^T, \quad \bar{I}_c^{pu} = [I_{c1}^{pu}, I_{c2}^{pu}, .., I_{cn}^{pu}]^T \tag{7.8c}$$

$$\bar{I}_r^{pu} = [I_{r1}^{pu}, I_{r2}^{pu}, ..., I_{rn}^{pu}]^T \tag{7.8d}$$

Due to dynamic consensus, steady state value of per unit current estimated of by all converters should be the same. Let $\mathscr{L}$ represent the Laplacian matrix of balanced communication graph, the steady state value is

$$\bar{I}^{pu}(s) = s(s1_n + m\mathscr{L})^{-1}(I_c^{pu}(s) + I_r^{pu}(s)) \tag{7.8e}$$

$$\bar{I}_{ss}^{pu} = \frac{1}{N}[1_N, 1_N...., 1_N](I_{css}^{pu} + I_{rss}^{pu}) \tag{7.8f}$$

Where 1_N is a 1×N unit matrix. Steady state value would consist of sum of averaged constant dc term I_{css}^{pu} Olfati-Saber and Murray [2004] and averaged second-order ripple term I_{rss}^{pu}. Hence, steady state current reference would reach consensus for all converters.

7.5.2 Dynamic droop control

Dynamic droop control is implemented for proportional current sharing.The value of droop constant is calculated by :

$$d_i = d_o + g_i \int (I_i^{pu} - I_i^{\bar{p}u}) \tag{7.9a}$$

where g_i is a positive constant and d_o is the initial droop constant. I_i^{pu} is inductor current of the dc-dc converter and $I_i^{\bar{p}u}$ is the reference current estimated by the converter by consensus control.The global local voltage reference is adjusted as in Anand *et al.* [2013]. The voltage reference is obtained by reducing the actual reference by output current times the droop calculated in (7.9a).

7.6 SIMULATION RESULTS

A DC Microgrid consisting of three parallel connected boost converter is simulated. A resistive load and an inverter load is connected to the dc bus. The parameters of converters and loads used for simulation is given in Table 7.1. A balanced communication graph is chosen so as to facilitate the nodes to exchange per unit load current value with its neighboring nodes. The simulation plots with dc and ac load loading is shown in Figure 7.6. The proposed controller was disabled during time interval t_1. Due to unequal line resistances, different sources are loaded differently. During the time interval t_2, the dynamic droop control is enabled. In this time interval, a constant resistance load is applied on the DC Microgrid. As a result, all sources share equal current as shown in Figure 7.6. During the time interval t_3, the inverter load is turned on. Due to ac load, the SRC can be seen.

Once the inverter load is applied the parameter ρ_i is adjusted to reduce the SRC passing through the converter by increasing the output impedance at $2f_{ac}$ frequency, when $\rho_i = 1$, the SRC propagating through it is minimum, as shown in Figure 7.7. Initially, ρ for all converters is 0.2. Hence, all sources share equal ripple during T_2 in Figure 7.7. The ac load is doubled during T_3. This leads to an increase in SRCs. During T_4, the ρ_1 is increased. This increases the impedance of converter-1. The SRC reduction can be seen in T_4. Similarly, during T_5, impedance of converter -2 is also increased. The reduced SRCs can be observed in converter 1 and 2. The SRC through converter 3 increases due to low value of impedance. Hence, SRC sharing is achieved. The dc value of load current remains the same. The FFT analysis of current waveform of converter-1 and

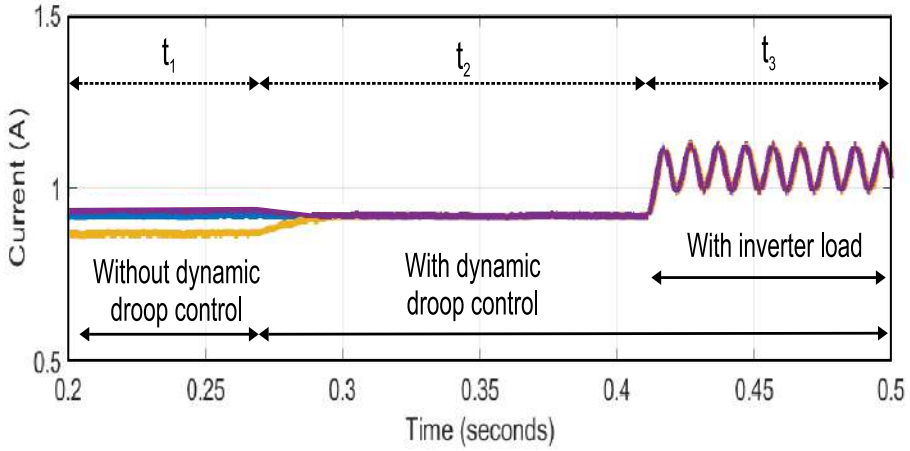

Figure 7.6 : Current sharing among sources

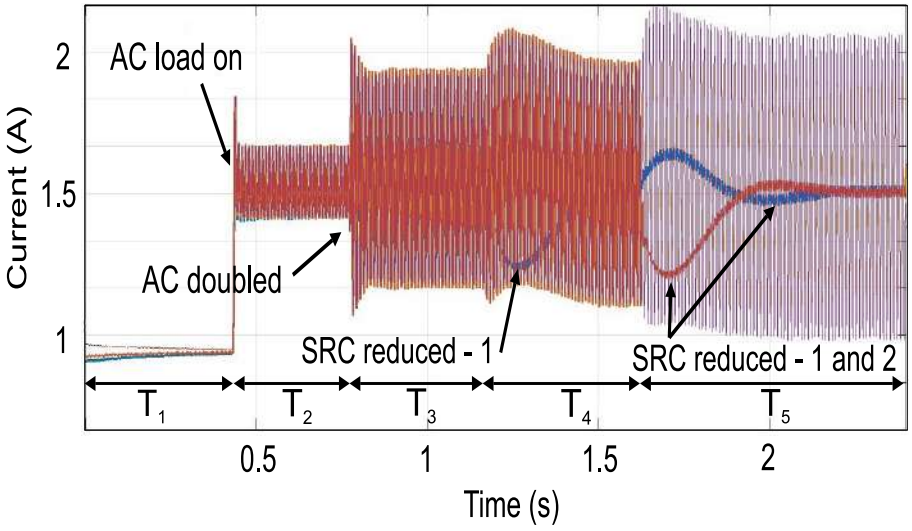

Figure 7.7 : Reduced ripple through sources

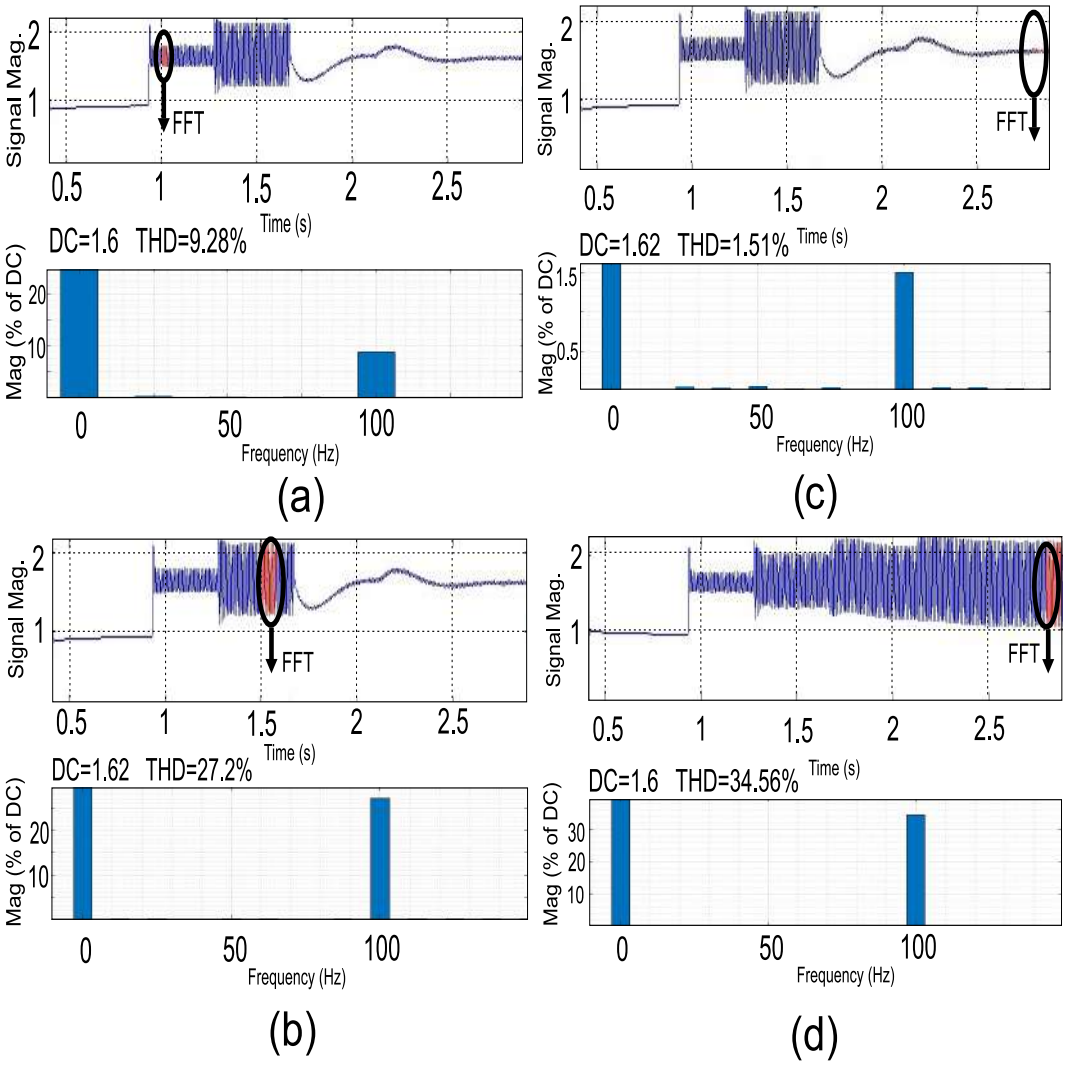

Figure 7.8 : FFT analysis of current- (a) Converter 1 (b) Converter 1 when ac load is doubled (c) Converter 1 after ASMCOIS is implemented (SRC mitigated) (d) Converter 3 (increased SRC due to low output impedance)

3 during different stages is shown in Figure 7.8. The FFT of converter 1 during T_2 and T_3 and T_5 of Figure 7.7 is shown in Figure 7.8a, Figure 7.8b and Figure 7.8c respectively. It can be observed that the THD increases from 9.28% to 27.2% due to increase in ac load. Further, THD reduces to 1.51% when the control is implemented. Hence, SRC is reduced significantly. On the other hand, FFT of converter 3 during interval T_5 of Figure 7.7 is shown in Figure 7.8d. The THD increases to 34.56% as the SRC now propagates through converter 3.

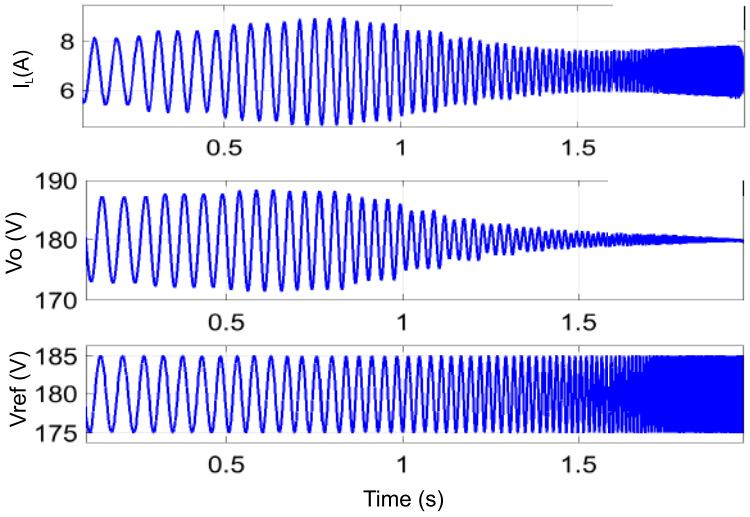

Figure 7.9 : The output impedance estimation using frequency sweep (10 to 10^4 Hz)

Further, the effect of variation of ρ on output impedance is analysed by frequency sweep from 10 to 10^4 Hz. The voltage and current waveform obtained from frequency sweep is shown in Figure 7.9. It can be seen that the magnitude diminishes as frequency increases. The frequency response of $\hat{v}_c/\hat{i}_L$ for different ρ value is shown in Figure 7.10. In Figure 7.10, the dots represent the impedance obtained from frequency sweep, and the solid line is the frequency response of estimated transfer function with best fit. It can be observed that the impedance with ρ=1 is 30 dB more compared to dc bus capacitance. Hence, output impedance is increased and SRC propagates to the bus capacitor. On the other hand, when ρ=0.1, the impedance is 5dB less than the dc bus capacitance. Hence, the SRC propagates to the source through the converter due to lower impedance path. Hence, the proposed control is verified to reduce SRC.

7.7 EXPERIMENTAL RESULTS

The proposed control law is validated by experimentation on a 1.5kW laboratory setup shown in Figure 7.11. Three boost converters were connected in parallel to form a DC Microgrid. Three regulated power supplies with maximum rating of 50V, 10A were connected as power source to the converters. The control algorithm is implemented on Opal-RT Real Time Digital Simulator. The individual control signal is given from Opal-RT to the three parallel connected boost converter setup. An open loop SPWM inverter and a resistance is connected to dc bus as load. The parameters for each converter is given in Table 7.1. The communication routine for data exchange between nodes is implemented on Matlab. The delay in communication has not been addresses in present work, however methods proposed in Zhang and Hredzak [2019] and references therein can be used.

The parameters for designing α, i.e. η, β are same for all three converters. The adjacency

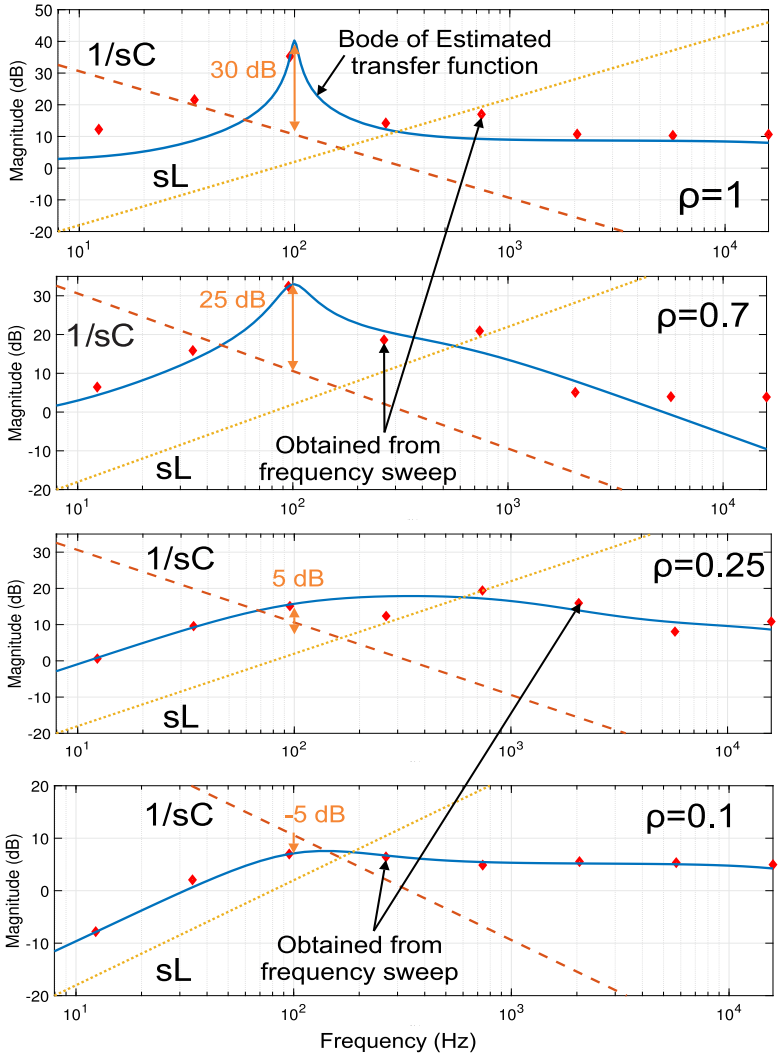

Figure 7.10 : Frequency response of $\hat{v}_c/\hat{i}_L$ obtained from frequency sweep to verify effect of ρ on impedance at 100 Hz

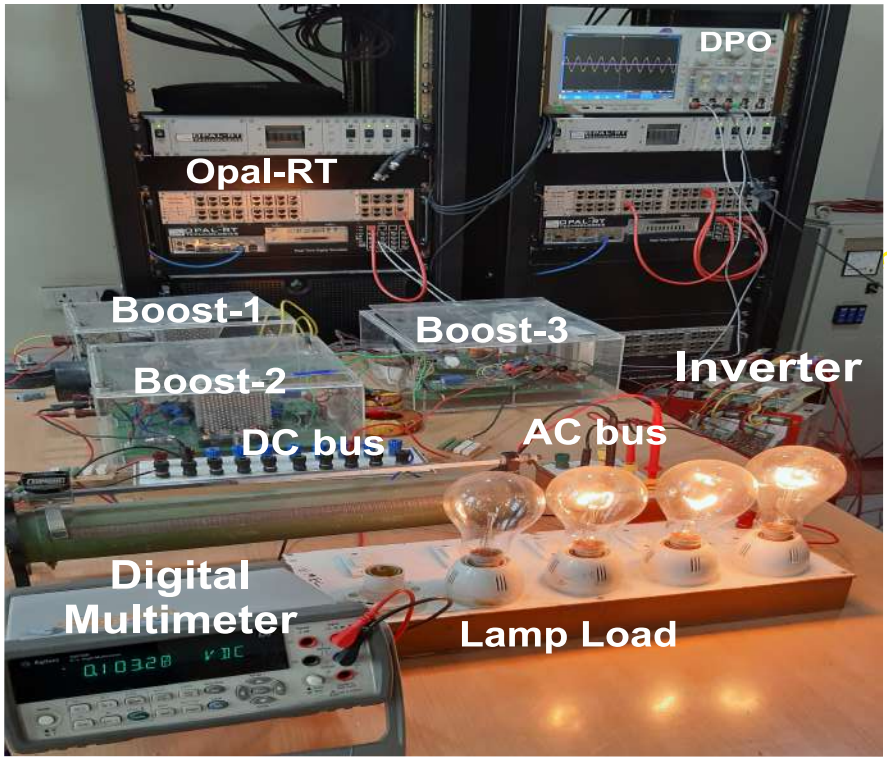

Figure 7.11 : Experimental setup

$\mathscr{A}$, in-degree $\mathscr{D}$, and Laplacian matrix $\mathscr{L}$ for communication topology is:

$$\mathscr{A} = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \mathscr{B} = \begin{bmatrix} 2 & 0 & 0 \\ 0 & 2 & 0 \\ 0 & 0 & 2 \end{bmatrix} \mathscr{L} = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

7.7.1 DC component sharing

Three equally rated boost converters are connected in parallel and controlled using the proposed method so as to have dc bus voltage of 140 $\pm$ 5 % V. DC load is increased from 400 W to 600 W and then back to 400 W. Equal load sharing is observed from Figure 7.12. The figure shows the output current of parallel connected converters. Dynamic variation of droop is shown in Figure 7.13.

7.7.2 Equal second order ripple sharing

The inverter fed resistance load of 300 W is connected to the dc bus, along with a resistance load of 120 W. The maximum voltage at inverter output terminals is 110V. Initially, ρ_1, ρ_2, ρ_3 are equal to 0.2. Due to equal value of control parameter ρ, the output impedance at $2f_{ac}$ of all the converters is same. Hence, they share equal ripple as shown in Figure 7.14 and dc component of load is shared proportionally as shown in Figure 7.15.

7.7.3 Ripple reduction through Converter-1 and 3

In this section, the ripple is now made to propagate only through converter-2. The ripple control parameter of converters are: ρ_1 = 0.7, ρ_3 = 0.7 while ρ_2 = 0.1. Due to low value of ρ_2, the SRCs primarily propagate through this converter, as shown in Figure 7.16. Although the SRCs through converter-2 is increased, this converter still supplies the proportional dc component of

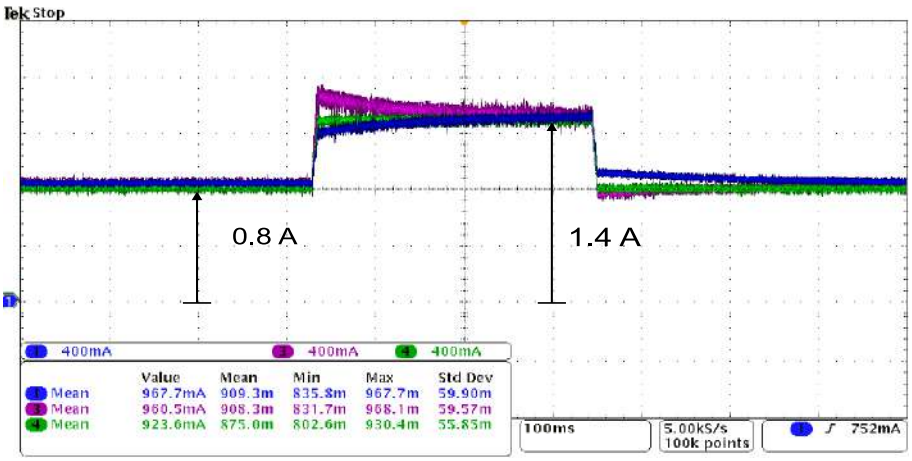

Figure 7.12 : Equal load current sharing among converters

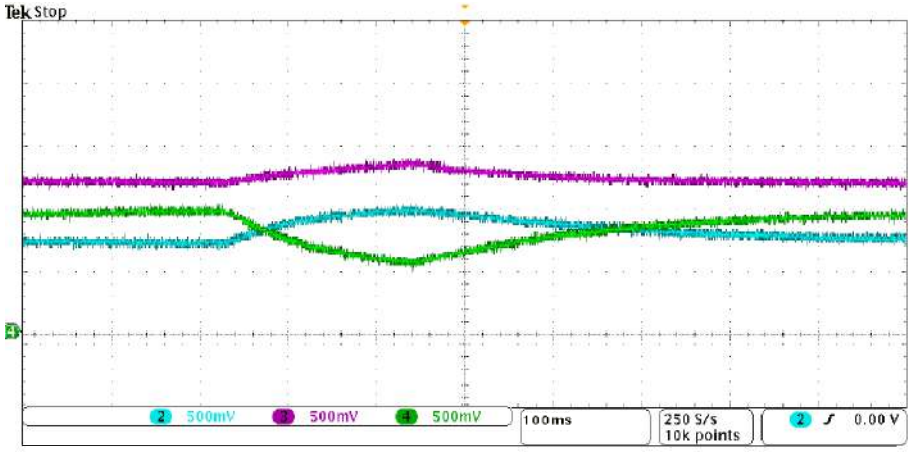

Figure 7.13 : Dynamic variation in droop during load changes

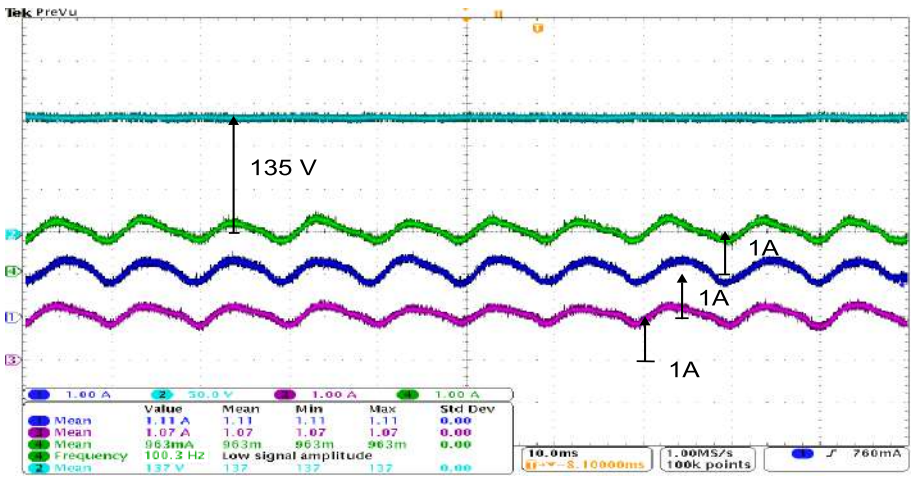

Figure 7.14 : SRC when inverter is turned on

Table 7.1 : Simulation and Experimental parameters

Parameters	Conv. 1	Conv. 2	Conv. 3
DC source voltage (V)	50	50	50
L (mH)	2	2.2	2.4
C (μF)	100	200	100
β	6	6	6
η	1×10^{-8}	1×10^{-8}	1×10^{-8}
R_{line} (Ω)	1	1.5	2
d_o (Ω)	1	1	1
k (Ω)	0.8	0.8	0.8
m,g	50,0.1	50,0.1	50,0.1
Switching Frequency (KHz)	20	20	20
Converter input voltage	50	50	50

LPF time constant τ	0.5 ms
Γ_i,Q_i, $(i = 1-3)$	170000,2000
Inverter Switching Frequency	5 KHz
Resistive load (Ω)	100
Inverter fed load	4x100W bulbs

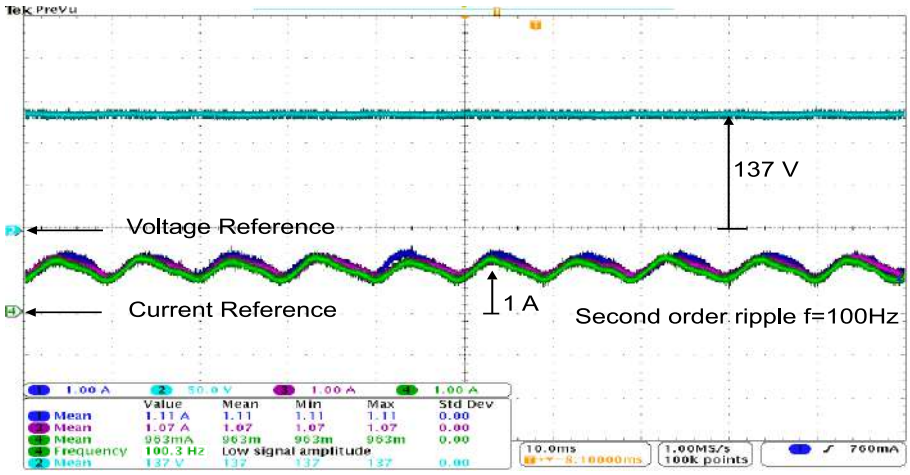

Figure 7.15 : Equal dc component sharing among sources

Table 7.2 : Comparison

Parameters	Hamzeh *et al.* [2015]	Jia *et al.* [2017b]	Proposed
Type of Controller	PI	PI	SMC
Type of droop	Constant	Constant	Dynamic
SRC sharing dependence on converter rating	Depends	Depends	Does not depend
Proportional load sharing	No	No	Yes
DC component sharing	Yes	No	Yes

load current as shown in Figure 7.17. The dc bus voltage also remains constant.

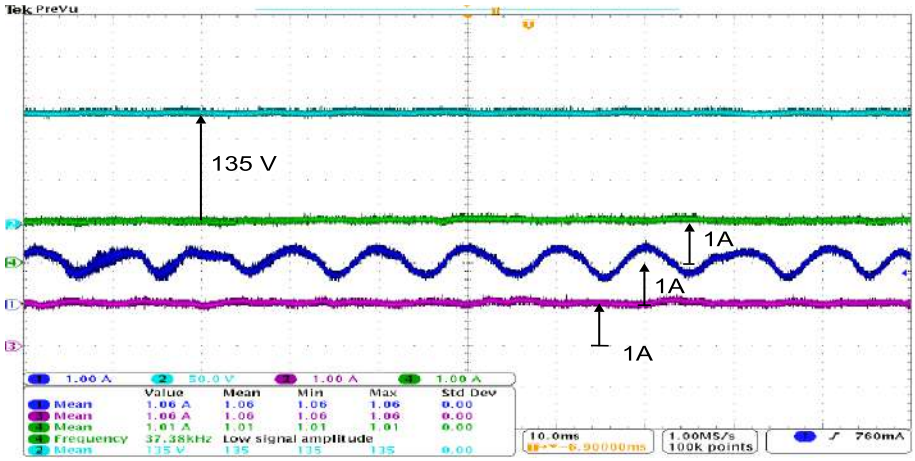

Figure 7.16 : Reduced ripple propagating through converter 1 and 3

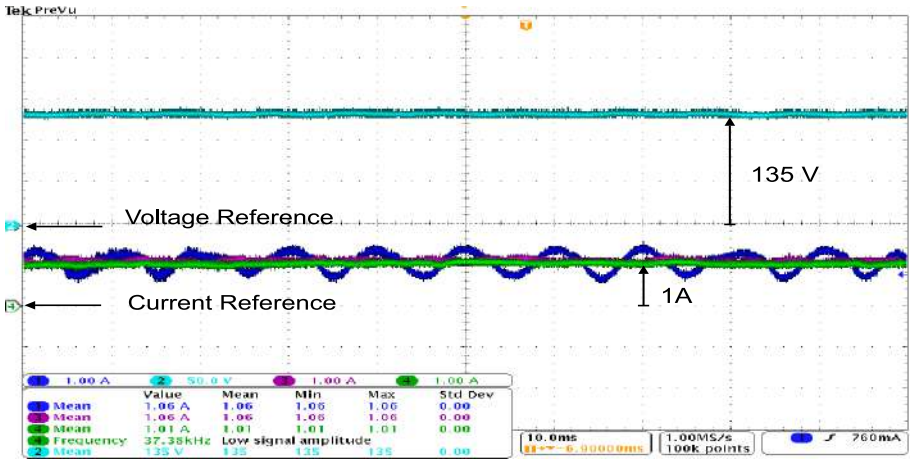

Figure 7.17 : Proportional dc component sharing

7.7.4 Ripple sharing among nodes

In this section, ripple sharing among converters shown in Figure 7.19, with changes in ρ is explained. The parallel connected converters have the same α_i and different values of ρ_i. During section A, the impedance of converter 2 is more converters 1 and 3. As a result, SRC in converter 3 is more than SRC in other converters. In section B, the ρ_2 is kept same while that of ρ_1 is made less than ρ_3. As a result, the SRC in converter 1 increases and becomes more than converter 3, and SRC reduces in converter 3. During section C, the ρ_1 and ρ_3 is made same as in section A. The SRC distribution becomes same as in section A. Hence, the SRC sharing is achieved. The dc load current value remains same in all the sections while SRC is shared. Hence, the proposed control is verified through experiments. Comparison of proposed methodology with other methods is given in Table 7.2.

7.7.5 Ripple sharing among nodes with different ripple references

In this section, ripple sharing among converters with immediate changes in ρ is explained. The parallel connected converters have the same α_i and different values of ρ_i. The observations is discussed under the following sections:

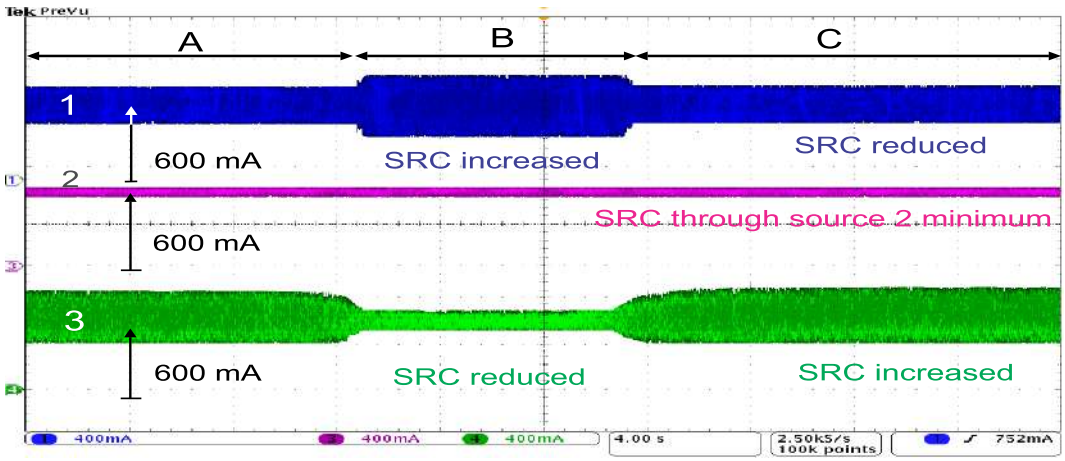

Figure 7.18 : Ripple component sharing among converters

S_A

Before section S_A, the value of ρ_1, ρ_2, ρ_3 are equal to 0.5. Due to equal value of ripple control parameter, all the nodes share equal SRCs and dc component of load current.

$S_A - S_B$

: In this interval, the values of ρ_3 is increased such that the ripple in converter-3 reduces, and its SRC is propagated to converter-2. In the mean time, the SRC in converter-1 remains unaffected. The values of control parameters used are: $\rho_1 = 0.5, \rho_2 = 0.4, \rho_3 = 0.6$.

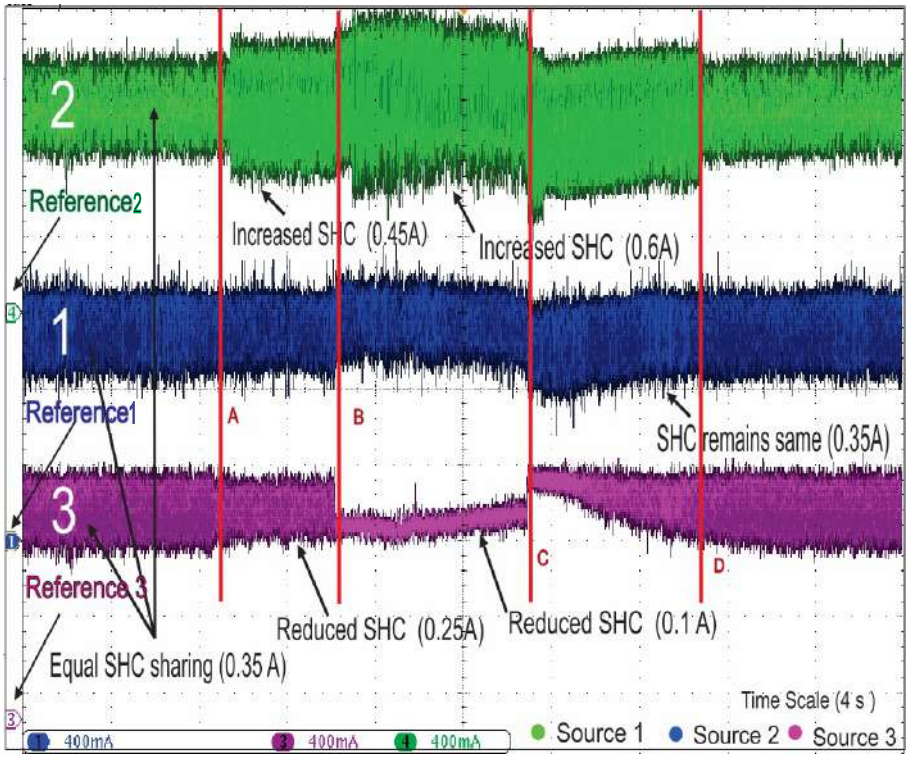

Figure 7.19 : Ripple component sharing among converters

$S_B - S_C$

: Now, the SRC in converter-3 is further reduced by further increasing ρ_3, while the ripple in converter-1 remains the same. It is observed that during this section, the ripple in converter-2 increases due to the lower value of ρ_1, and hence lower $2f_{ac}$ impedance. Due to high capacitance at converter-2 output terminals, the SRC is absorbed at this node. Hence, the objective of diverting ripple from one node to other has been achieved. During this section, $\rho_1 = 0.5, \rho_2 = 0.1, \rho_3 = 0.9$.

$S_C - S_D$

: In this interval, the ρ values are made similar to section $S_A - S_B$ and hence the SRC distribution is the same as in $S_A - S_B$. SRC in converter-1 reduces and increases in converter-3. During this section,$\rho_1 = 0.5, \rho_2 = 0.4, \rho_3 = 0.6$.

S_D

: After Section D, all ρ values are again made same and hence, SRC is equally shared among all three converters. Values of is $\rho_1 = 0.5, \rho_2 = 0.5, \rho_3 = 0.5$.
Hence, converters with higher ρ have lesser SRC than the ones which have lower ρ. The dynamic voltage control parameter α remains the same for all converters. So, if the SRC is to be prevented from propagating through the converter to the source, it should have higher ρ. On the other hand, in case of availability of filters in a node, a lower ρ will be used, so that more ripple can propagate to this node.

7.8 CONCLUSION

The chapter has proposed a solution to share or reduce SRCs while maintaining good voltage regulation and proportional load sharing among sources and energy storages. The proposed ASMC-OIS methodology reduces second order ripple propagating through a converter by increasing the converter's output impedance at $2f_{ac}$. From experimentation it has been verified that the dynamic parameter α maintains the dc bus voltage within $\pm 5\%$ of rated voltage. The ripple reduction has been achieved, such that for increase of ρ from 0.2 to 1, the SRC gets reduced from 0.4A to 0.1A for 1A dc component. Hence, ρ has been increased or decreased to adjust the output impedance and regulate ripple propagation at different nodes. Using the proposed controller, the SRC is propagated to nodes having higher capacitance or ripple absorption ports. This will improve the energy density in ripple absorption circuits and improve the overall efficiency of the microgrid. As the ripple is propagated to nodes having ripple filters, a smaller capacitance can be used in the active filtering circuits. This allows the usage of non-electrolytic capacitors which have higher life time compared to the electrolytic ones. By using the proposed controller, the dc component is shared proportionally even in the absence of any inverter load. Hence, the proposed controller has been verified for DC Microgrid with only dc loads or dc and inverter fed ac loads. The proposed controller has been validated using simulation and experimentation.

In the next Chapter, the conclusion of this thesis work and future challenges and scopes will be discussed.