

Robust Control Techniques for Virtual Impedance Shaping to Mitigate and Share the Double Line Frequency Ripple in Microgrids

A Thesis submitted by
Shivam Chaturvedi

in partial fulfillment of the requirements for the award of the degree of
Doctor of Philosophy



॥ त्वं ज्ञानमयो विज्ञानमयोऽसि ॥

Indian Institute of Technology Jodhpur
Department of Electrical Engineering
August 2020

Declaration

I hereby declare that the work presented in this Thesis titled *Robust Control Techniques for Virtual Impedance Shaping to Mitigate and Share the Double Line Frequency Ripple in Microgrids* submitted to the Indian Institute of Technology Jodhpur in partial fulfillment of the requirements for the award of the degree of Doctor of Philosophy, is a bonafide record of the research work carried out under the supervision of Professor Deepak M. Fulwani. The contents of this thesis in full or in parts, have not been submitted to, and will not be submitted by me to, any other Institute or University in India or abroad for the award of any degree or diploma.

Shivam Chaturvedi
P15EE004

Certificate

This is to certify that the thesis titled *Robust Control Techniques for Virtual Impedance Shaping to Mitigate and Share the Double Line Frequency Ripple in Microgrids*, submitted by *Shivam Chaturvedi (P15EE004)* to the Indian Institute of Technology Jodhpur for the award of the degree of *Doctor of Philosophy*, is a bonafide record of the research work done by him under our supervision. To the best of my knowledge, the contents of this report, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Deepak M. Fulwani
Ph.D. Thesis Supervisor

Acknowledgments

I would like to express my sincere gratitude to my Ph.D. Thesis Supervisor, Professor Deepak M. Fulwani. He always had time for the empirical and constructive discussion from his schedule, tightly packed with academic and administrative responsibilities. I am thankful to him for his continuous efforts to inculcate the positive motivation in me and his continual guidance, generous support and patience, especially during the times of my slow progress. He introduced me to the field of sliding mode control and its use in the power applications. He gave me ample opportunities for the relevant exposure at conferences, despite limited resources. Professor Fulwani, has been my continuous source of inspiration in shaping up my world of academic and research, morals and ethics.

It's always been a pleasure and opportunity to work with my seniors Dr. Aditya Raw Gautam, and Dr. Ram Niwas Mahia who have been my constant source of inspiration through their 'can do' attitude and perseverance. My special thank goes to my laboratory colleagues, Rammohan, Poonam, Mohit, Sandeep, Arpita, Jitendra for their motivation and support throughout my research work. I thank Rohit, Aniket, Amrik, Abhishek, Dr. Dileep for their wonderful company and for all the liveliness they infused into the non-academic portion of the days at IIT Jodhpur. I thank my all friends who made my days at IIT Jodhpur a truly memorable experience.

Finally, I acknowledge and express my deepest gratitude to my Family for the patience, support and love which they ushered on me, and for bearing with me even when I was not spending any time with them. I pay utter regards to my parents, and sisters for all their love, sacrifices and blessings.

Shivam Chaturvedi
Ph.D. Student

List of Figures

| Figure | Title | page |
|--------|--|------|
| 1.1 | Concept of impedance shaping | 5 |
| 1.2 | q-Z Source Inverter | 6 |
| 1.3 | eq-Switched Boost Inverter | 6 |
| 1.4 | Virtual impedance shaping for SSIs | 6 |
| 1.5 | Proposed power sharing scheme: High and low impedance at $2f_{ac}$ is achieved by output impedance shaping | 7 |
| 1.6 | Without impedance control | 9 |
| 1.7 | Virtual impedance control | 9 |
| 1.8 | A two node microgrid | 9 |
| 1.9 | Proposed dual loop with SRC control loop | 10 |
| 1.10 | Proposed dual loop with ISM control | 12 |
| 1.11 | Sliding mode control (a) Constant Surface (b) Dynamic Surface | 12 |
| 1.12 | System Dynamics: (a) With $u^+(x,t)$, (b) With $u^-(x,t)$, (c) Dynamics with sliding mode control | 14 |
| 2.1 | Series interfacing of APDC | 22 |
| 2.2 | Parallel interfacing of active power APDC | 22 |
| 2.3 | Active power filter for CSIs | 22 |
| 2.4 | Active power buffer for CSI | 23 |
| 2.5 | Active filter for qZSIs | 23 |
| 2.6 | High frequency flyback based utility interactive topology | 24 |
| 2.7 | Flyback type single phase grid interactive inverters | 24 |
| 2.8 | Flyback inverter for PV applications | 25 |
| 2.9 | Single phase pulse width modulation voltage source rectifier | 25 |
| 2.10 | Series interfacing of active power APDC | 26 |
| 2.11 | ACRC proposed in Mellincovsky <i>et al.</i> [2018] | 26 |
| 2.12 | Doubly ground inverter topology proposed in Xia <i>et al.</i> [2017] | 27 |
| 2.13 | Configuration proposed in Ohnuma and Itoh [2014] | 27 |
| 2.14 | SRC control configuration proposed in Zhu <i>et al.</i> [2016] | 28 |
| 2.15 | Configuration proposed in Serban [2015] | 28 |
| 2.16 | Configuration proposed in Ohnuma <i>et al.</i> [2015] | 29 |
| 2.17 | Symmetrical half bridge configuration proposed in Tang <i>et al.</i> [2015] | 29 |
| 2.18 | Half bridge split capacitor proposed in Yao <i>et al.</i> [2017] | 30 |
| 2.19 | Load current feed-forward methodology | 30 |
| 2.20 | An feed-forward control scheme Yang <i>et al.</i> [2014] | 32 |
| 2.21 | Resonant controller based dual loop control ZhengWei <i>et al.</i> [2012] | 32 |
| 2.22 | Virtual resistance scheme | 33 |
| 2.23 | Band pass filter inductor current feedback scheme | 33 |
| 2.24 | BPFICF with parallel impedance loop | 34 |
| 2.25 | Notch-Filter-Inserted Load-Current Feedforward Scheme (NF-LCFFS) | 34 |
| 2.26 | NF-LCFFS with VRS | 35 |
| 2.27 | Conventional PWM for SSIs | 35 |
| 2.28 | PWM strategy proposed in Nguyen <i>et al.</i> [2019] | 36 |

| | | |
|------|--|----|
| 2.29 | PWM strategy proposed in Ravindranath <i>et al.</i> [2013] | 37 |
| 2.30 | PWM strategy proposed in Yu <i>et al.</i> [2011a] | 38 |
| 2.31 | Concept of centralized and decentralized control | 39 |
| 2.32 | Control hierarchy for microgrids | 40 |
| 2.33 | Communication: (a) All to All (b) Neighboring (c) Sparse | 41 |
| 2.34 | Tertiary Control | 41 |
| | | |
| 3.1 | A conventional inverter | 45 |
| 3.2 | eqSBI | 45 |
| 3.3 | DC-AC converters | 45 |
| 3.4 | A Quasi-Z-source Inverter (qZSI) | 46 |
| 3.5 | Embedded Quasi Switched Boost Inverter (eqSBI) | 46 |
| 3.6 | Single stageDC-AC converters | 46 |
| 3.7 | The maximum power point oscillates due to second order ripple in DC voltage and currents | 47 |
| 3.8 | A capacitor with a larger value is required to reduce the SRCs | 47 |
| 3.9 | Switching logic for qZSI | 53 |
| 3.10 | Switching logic for eqSBI | 53 |
| 3.11 | Simulation of gate pulses for shoot through in qZSI | 53 |
| 3.12 | Simulation of gate pulses for shoot through in eqSBI | 54 |
| 3.13 | An instance of SPWM with shoot through for switches S_1 , S_4 and S_5 for qSBI converters | 54 |
| 3.14 | An instance of SPWM with shoot through for switches S_2 , S_3 and S_5 for qSBI converters | 54 |
| 3.15 | Simulation of qZSI | 56 |
| 3.16 | Simulation of eqSBI | 56 |
| 3.17 | Hardware setup | 57 |
| 3.18 | Output inverter voltage and inductor current with SRC | 57 |
| 3.19 | Output inverter voltage and inductor current with SRC control | 58 |
| 3.20 | Waveforms with and without impedance control | 58 |
| 3.21 | Waveforms with low pass filter time constant variation | 59 |
| | | |
| 4.1 | Single stage inverter operation stages- (a) shoot through stage qZSI (b) non-shoot through stage qZSI (c) shoot through stage eqSBI (d) non-shoot through stage eqSBI | 63 |
| 4.2 | Bode plots with and without dual loop control: (a) Current control loop qZSI, (b) Voltage control loop qZSI, (c) Impedance bode plot qZSI, (d) Current control loop eqSBI, (e) Voltage control loop eqSBI, (f) Impedance bode plot eqSBI | 66 |
| 4.3 | Proposed ISMRM with dual loop control | 68 |
| 4.4 | Waveforms of d_o , and estimated magnitude of d_{2f} -(a) with constant d_o , (b) with varying d_o | 70 |
| 4.5 | Voltage and current waveforms and control parameters for qZSI | 71 |
| 4.6 | Voltage and current waveforms and control parameters for qZSI | 72 |
| 4.7 | Voltage and current waveforms with perturbed voltage reference for (a) qZSI and (b)eqSBI | 73 |
| 4.8 | FFT analysis: (a) THD plot of inductor current without control-11% of load current at $2f_{ac}$, (b) THD plot of inductor current with control-1.2% of the load current at $2f_{ac}$ | 74 |
| 4.9 | Frequency sweep response for output impedance Z_o for qZSI | 74 |
| 4.10 | Hardware setup for qZSI and eqSBI | 75 |
| 4.11 | Waveforms of qZSI with control activation | 76 |
| 4.12 | Waveforms of qZSI with control deactivation | 77 |
| 4.13 | qZSI with inductive load and control deactivated | 77 |
| 4.14 | qZSI with inductive load and control activated | 78 |
| 4.15 | eqSBI waveforms without control | 78 |
| 4.16 | eqSBI waveforms without control | 79 |
| 4.17 | SRC reduction with load variation for qZSI | 79 |
| 4.18 | Waveforms of eqSBI with load variations | 80 |
| 4.19 | Waveforms with sinusoidal disturbance | 80 |

| | | |
|------|---|-----|
| 4.20 | Cancellation of disturbance using the proposed control | 81 |
| 5.1 | Proposed SRC and DC component sharing (a) Without any virtual impedance control, (b) With DVI control- The virtual impedance $Z_{v1} > Z_{v2}$ hence, $SRC_1 < SRC_2$. Similarly, $R_{d1} < R_{d2}$ to share DC component equally. | 85 |
| 5.2 | (a) Proposed DVI control, (b) Proposed DVI with Δi_L as reference, (c) Proposed DVI with $i_{ref_{puN}}$ as reference | 86 |
| 5.3 | Bode plot of \hat{i}_L/\hat{d} with Z_v | 88 |
| 5.4 | Output impedance with different Z_v | 88 |
| 5.5 | Bode plot of \hat{v}_o/\hat{d} | 89 |
| 5.6 | A two node DC microgrid | 90 |
| 5.7 | Proposed SRC control with Primary and Secondary control | 90 |
| 5.8 | Response time- variation in τ, C | 91 |
| 5.9 | Response time- variation in Z_v, C | 91 |
| 5.10 | Response time- variation in τ, Z_v | 92 |
| 5.11 | SRC with variation in L, Z_v | 92 |
| 5.12 | Root locus of $\hat{v}_{io}/\hat{v}_{refo}$ with Z_v | 93 |
| 5.13 | Variation of \hat{i}_L/\hat{i}_{Load} with Z_v at $2f_{ac}$ | 93 |
| 5.14 | Equal DC load sharing and SRC control | 95 |
| 5.15 | Variation of Z_v with load changes | 95 |
| 5.16 | Experimental setup | 96 |
| 5.17 | Source currents- $C_{bus} 1.36mF$ | 98 |
| 5.18 | Equal DC load sharing | 98 |
| 5.19 | SRC with inverter load turned on | 99 |
| 5.20 | SRC mitigation- $C_{bus} 1.36mF$ | 99 |
| 5.21 | SRC reduced at one node | 100 |
| 5.22 | SRC sharing between two nodes | 100 |
| 5.23 | Constant SRC with varying AC | 101 |
| 5.24 | Constant SRC with varying DC | 101 |
| 5.25 | Ripple sharing and mitigation | 102 |
| 5.26 | SRC in a three node microgrid | 102 |
| 5.27 | SRC mitigation at nodes 1 and 3 | 103 |
| 5.28 | With AC loads turned- on and off | 103 |
| 6.1 | Proposed ISMSC and SMPC control | 109 |
| 6.2 | Phase plane plot: showing voltage and current error convergence to zero- (a) With constant $\lambda=0.01$, (b) With dynamic λ and $\gamma=0.01$, (c) With dynamic λ and $\gamma=0.05$, (d) With dynamic λ and $\gamma=0.2$ | 110 |
| 6.3 | Existence region in phase plane for j^{th} node | 113 |
| 6.4 | Sliding surfaces: (a) Constant λ (b) Dynamic λ | 114 |
| 6.5 | Lyapunov's function at different nodes | 119 |
| 6.6 | Proposed voltage and current control waveform | 122 |
| 6.7 | Plug-in and out of node 1 (a) Node-1 to be connected, no communication with nodes-2 and 3 (b) Node-1 plugged in (c) Node-1 plugged out | 122 |
| 6.8 | Plug in and out with high loaded incoming node | 123 |
| 6.9 | Plug in and out with less loaded incoming node | 123 |
| 6.10 | Proportional load sharing with external disturbance in communicated per unit load current | 124 |
| 6.11 | Hardware setup | 125 |
| 6.12 | With Proposed Control | 126 |
| 6.13 | Plug in and out with less loaded node-1 | 127 |
| 6.14 | Proportional load sharing with plug in and out of a less loaded incoming node (of higher rating) | 127 |
| 6.15 | Plug in and out with more loaded incoming node-1 | 128 |

| | | |
|------|---|-----|
| 6.16 | Proportional load sharing with plug in and out of a high loaded incoming node (of higher rating) | 129 |
| 6.17 | Proportional load sharing in presence of disturbance | 130 |
| 7.1 | Proposed power sharing scheme: High and low impedance at $2f_{ac}$ is achieved by output impedance shaping | 133 |
| 7.2 | Variation of alpha with voltage error | 135 |
| 7.3 | Proposed Control Strategy with Primary and Secondary Control layers | 136 |
| 7.4 | Frequency response of X_c, X_L and Z_o with impedance shaping, $\rho_3 > \rho_2 > \rho_1$ and $Z_{o3} > Z_{o2} > Z_{o1}$, Z_{o1} is impedance without control | 139 |
| 7.5 | Stability analysis of voltage variation at N converter nodes | 140 |
| 7.6 | Current sharing among sources | 144 |
| 7.7 | Reduced ripple through sources | 144 |
| 7.8 | FFT analysis of current- (a) Converter 1 (b) Converter 1 when ac load is doubled (c) Converter 1 after ASMCOIS is implemented (SRC mitigated) (d) Converter 3 (increased SRC due to low output impedance) | 145 |
| 7.9 | The output impedance estimation using frequency sweep (10 to 10^4 Hz) | 146 |
| 7.10 | Frequency response of \hat{v}_c/\hat{i}_L obtained from frequency sweep to verify effect of ρ on impedance at 100 Hz | 147 |
| 7.11 | Experimental setup | 148 |
| 7.12 | Equal load current sharing among converters | 149 |
| 7.13 | Dynamic variation in droop during load changes | 149 |
| 7.14 | SRC when inverter is turned on | 149 |
| 7.15 | Equal dc component sharing among sources | 150 |
| 7.16 | Reduced ripple propagating through converter 1 and 3 | 151 |
| 7.17 | Proportional dc component sharing | 151 |
| 7.18 | Ripple component sharing among converters | 152 |
| 7.19 | Ripple component sharing among converters | 152 |

List of Tables

| <i>Table</i> | <i>Title</i> | <i>page</i> |
|--------------|---|-------------|
| 2.1 | Summary of active control methodologies | 31 |
| 2.2 | Summary of Control methodologies | 43 |
| 3.1 | Simulation and experimental parameters | 55 |
| 4.1 | Simulation and experimental parameters | 72 |
| 5.1 | Simulation and Experiment Parameters | 97 |
| 5.2 | Comparison of components for SRC mitigation | 104 |
| 6.1 | Simulation and Experimental Parameters | 121 |
| 6.2 | Comparison | 128 |
| 7.1 | Simulation and Experimental parameters | 150 |
| 7.2 | Comparison | 150 |

List of Symbols

| Symbol | Description |
|----------------|--|
| P_c | Power dc component |
| P_r | Power ripple component |
| ω | ac supply frequency |
| ϕ | Load power factor angle |
| V_m | Voltage maximum values |
| I_m | Current maximum values |
| i_L | Inductor current |
| v_c | Capacitor terminal voltage |
| d_{st} | Shoot through duty cycle |
| e_i | Inductor current error |
| e_v | Voltage error |
| κ | Positive constant |
| L | Inductance |
| C | Capacitance |
| i_{ref} | Current reference |
| v_{ref} | Voltage reference |
| τ | Low pass filter time constant |
| 2ω | Angular frequency of second-order ripple |
| V_c | Steady state values of capacitor voltage |
| I_L | Steady state values of inductor current |
| D | Steady state values of duty cycle |
| E | Source voltage |
| r_L | Inductor resistance |
| G_{vd} | Capacitor voltage to control |
| G_{id} | Inductor current to control |
| G_{vi} | Capacitor voltage to inductor current |
| G_i | Inductor Current Controller |
| G_v | Capacitor Voltage Controller |
| T_{pi} | Control to inductor current transfer function |
| T_{pv} | Control to voltage transfer function |
| G_{iLio} | Inductor current to output current transfer function |
| G_{vcio} | Capacitor voltage to output current transfer |
| $\phi_m(t)$ | Matched uncertainty |
| $\phi_u(t, x)$ | Unmatched uncertainty |
| d_o | Nominal control law |
| d_{2f} | Second order oscillations in the control law |
| d_n | Non-linear control law |
| d_{pi} | Control law from PI controller |
| d_{neq} | Equivalent control law |
| H_1, H_2 | Current and voltage sensor gain |
| Z_v | Virtual Impedance |

| Symbol | Description |
|---------------------------------------|--|
| v_{refo} | DC bus voltage reference |
| k_1, k_2 | Current share proportions |
| v_{refi} | Voltage reference of i^{th} converter |
| G_D | Communication delay |
| G_{com} | PI controller for secondary control |
| I_i^{pu} | Per-unit loading of i^{th} converter |
| I_j^{pu} | Per-unit loading of j^{th} converter |
| V_{dcj} | The source voltage |
| v_{cj} | Voltage across output capacitor |
| i_{Lj} | Inductor current of j^{th} converter |
| u_{1j} | Duty cycle of j^{th} converter |
| \mathcal{N}_j | Number of electrically connected neighbors of j^{th} converter |
| r_{Lj} | the inductor resistance |
| i_{oj} | total current flowing out of j^{th} converter |
| ΔV_{ref} | the voltage reference variation due to ISMSC control |
| d_i | Dynamic droop |
| d_o | Constant droop |
| $k_i, \beta_i, \alpha_i, \rho_i, \mu$ | Positive Constants |
| Γ_i, Q_i | SMC reaching Design parameters |
| \bar{I}_i^{pu} | Average microgrid load |
| I_i | The load current of i^{th} converter |
| I_r | Converter's current rating |

List of Abbreviation

| Abbreviation | Full form |
|-------------------|---|
| <i>ASMCOIC</i> | Adaptive Sliding Mode Control based Output Impedance Shaping |
| <i>AACC</i> | Adaptive Active Capacitor Converter |
| <i>APDC</i> | Active Power Decoupling Scheme |
| <i>APF</i> | Active Power Filter |
| <i>BMS</i> | Battery Management System |
| <i>BPFICF</i> | Band-Pass Incorporated Inductor Current Feedback |
| <i>CSI</i> | Current Source Inverter |
| <i>CPD</i> | Combinational Power Decoupling |
| <i>eqSBI</i> | Embedded Quasi Switched Boost Inverter |
| <i>FCs</i> | Fuel Cell |
| <i>ISMC</i> | Integral Sliding Mode Control |
| <i>LED</i> | Light Emitting Diode |
| <i>Li – ion</i> | Lithium Ion |
| <i>MPPT</i> | Maximum Power Point Tracking/Tracker |
| <i>MPP</i> | Maximum Power Point |
| <i>MOSFET</i> | Metal-Oxide Semiconductor Field Transistor |
| <i>MMCs</i> | Modular Multilevel Converters |
| <i>NF</i> | Notch Filter |
| <i>NF – CR</i> | Notch Filter inserted Current Reference |
| <i>NF – LCFFS</i> | Notch Filter inserted Load Current Feed Forward Scheme |
| <i>Na – S</i> | Sodium Sulphur |
| <i>Ni – Cd</i> | Nickel Cadmium |
| <i>NFVRLCFFS</i> | Notch Filter Cascading Voltage Regulator Load Current Feed-Forward Scheme |
| <i>PEMFC</i> | Proton Exchange Membrane based Fuel Cell |
| <i>PMU</i> | Power Management Unit |
| <i>PV</i> | Photo Voltaic |
| <i>PWM</i> | Pulse Width Modulation |
| <i>qZSIs</i> | Quasi-Z Source Inverters |
| <i>SSIs</i> | Single Stage Inverters |
| <i>SLZSI</i> | Switched Inductor Switched Boost Inverter |
| <i>SMC</i> | Sliding Mode Control |
| <i>SMPC</i> | Sliding Mode Based Primary Control |
| <i>SRCs</i> | Second Order Ripple Currents |

| Abbreviation | Full form |
|--------------|--------------------------------------|
| <i>SORI</i> | Second Order Ripple Impedance |
| <i>SMM</i> | Sequential Magnetization Modulation |
| <i>SCC</i> | Stacked Switched Capacitor |
| <i>TZSI</i> | Trans-Z Source Inverter |
| <i>THD</i> | Total Harmonic Distortion |
| <i>TMM</i> | Time Shared Magnetization Modulation |
| <i>VLA</i> | Vented Lead Acid |
| <i>VRLA</i> | Valve Regulated Lead Acid |
| <i>VAWT</i> | Vertical Axis Wind Turbines |
| <i>VRS</i> | Virtual Resistance Scheme |
| <i>VSI</i> | Voltage Source Inverter |
| <i>WT</i> | Wind Turbines |
| <i>ZVS</i> | Zero Voltage Switching |
| <i>ZSN</i> | Z-Source Network |