3

Control of Single Stage Inverters and Second Order Ripple Regulation Using Sliding Mode Control

In the previous chapter, a comprehensive review of various SRC mitigation methodologies have been presented. The active, passive and based control methodologies have been discussed. The control based methodology is preferred over other methodologies as it does not require any additional component to mitigate the SRCs. In this chapter, a robust sliding mode control based methodology is presented to regulate the SRC propagation to the source for the single stage inverter topology. The SRC is mitigated by regulating the current reference to the controller. The effect of low pass filter time constant variation on SRC is presented. The proposed control is verified for qZSI and eqSBI single stage inverters.

The conventional inverters are used in industrial drives, uninterrupted power supplies, grid interfacing of renewable sources, electric vehicles. These are usually called the voltage source inverters (VSIs) . A typical circuit of VSI is shown in Figure3.1. These have a limitation that the peak output AC voltage cannot be greater than the input DC voltage of the inverter. Peak output AC voltage depends on the modulation index. In contrast, the wide applications of inverter need output AC voltage to be higher than the input DC voltage. For this, a two-stage topology is adopted, in which the input DC voltage if first boosted using a boost converter and then it is fed to an inverter stage. This meets the desired output AC voltage magnitude demand, with the cost of increased component count and a bulkier integrated DC-AC converter system. To reduce the component count and size of DC-AC conversion, the concept of Z-source inverter (ZSIs) is proposed in Fang Zheng Peng *et al.* [2005].

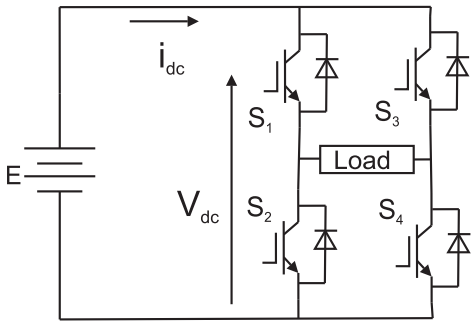

Figure 3.1 : A conventional inverter

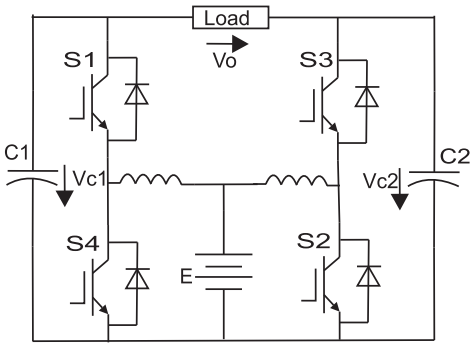

Figure 3.2 : eqSBI

Figure 3.3 : DC-AC converters

It consists of a 'X' shaped connection of two inductors and capacitor as shown in Figure3.2, and uses a shoot through stage of inverter to boost the input voltage. This leads to DC-AC conversion in a single stage and uses the dead time in case of a two-stage inverter. In recent years, many topologies and PWM techniques have been proposed to improve the performance

of ZSIs. The topologies proposed in the literature have main focus on the following objectives: a. Improve input current profile, b. Obtain higher boosting factor, c. Reducing the voltage and current stress on converter components, d. Reducing second-order ripple to the source, e. Reducing the converter component count. The component selection in a single-stage DC-AC conversion depends on the application. A low power application does not need the Z impedance configuration. This led to the topologies of quasi Z -source inverters, shown in Figure 3.4, and Switched Boost Inverters (SBIs), shown in Figure 3.5. The q-ZSIs have the advantage of improved boosting factor and current profile compared to ZSIs Sun *et al.* [2014]. The SBIs consists of an extra active switch compared to ZSIs. These are feasible for nanogrid and low power applications. Different topologies such as Embedded type qSBI and DC-link type qSBI have been proposed Nguyen *et al.* [2015b].

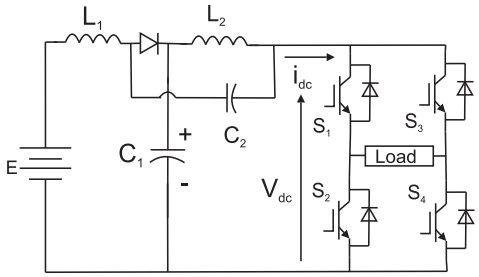

Figure 3.4 : A Quasi-Z-source Inverter (qZSI)

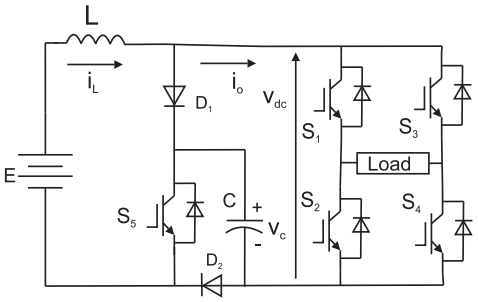

Figure 3.5 : Embedded Quasi Switched Boost Inverter (eqSBI)

Figure 3.6 : Single stageDC-AC converters

Single stage DC-AC conversion causes second order ripples in DC side voltages and currents. The voltage of the inverter DC terminals is usually tightly controlled as a result of this, the ripple is primarily in the DC current. The constant DC power demand and ripple power can be derived as: Instantaneous output power of an inverter $P_{ac} = V_{ac}\, I_{ac}$

$$P_{ac} = V_{ac}I_{ac} = V_m cos(\omega t) I_m cos(\omega t - \phi) \tag{3.1}$$

On further expanding above equation and dividing power into the constant DC component P_c and ripple component P_r:

$$P_{ac} = \frac{1}{2} V_m I_m cos(\phi) + \frac{1}{2} V_m I_m cos(2\omega t - \phi) = P_c + P_r \tag{3.2}$$

Where, ω is the AC supply frequency, ϕ is load power factor angle, V_m and I_m are voltage and current maximum values. This second order ripple current (SRCs) propagates to the source and causes reduction in efficiency by affecting maximum power point extraction mechanism Liu *et al.* [2014], as shown in Figure 3.7. SRCs increases the temperature of PV panels Kim *et al.* [2013] and causes ripple torques in wind turbinesPeña-Alzola *et al.* [2017]. Also, a large electrolytic capacitor is required to absorb the SRCs, as shown in Figure 3.8. These electrolytic capacitor are not reliable Falck *et al.* [2018]. In terms of batteries, it causes rise in temperature in lead acid or Nickel Cadmium batteries and degrades the electrode lifetime. Any ripple more than 8% of the rated value Dong *et al.* [2013] has detrimental effect on battery's life span. Hence, the SRCs must be mitigated from propagating to the source to improve efficieny and life span of conponents and sources Hamzeh *et al.* [2015].

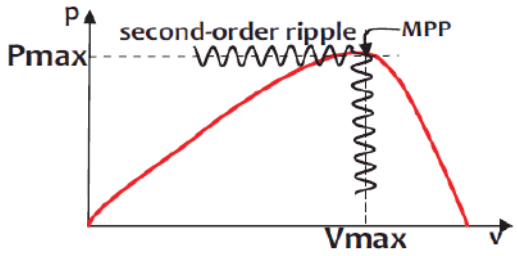

Figure 3.7 : The maximum power point oscillates due to second order ripple in DC voltage and currents

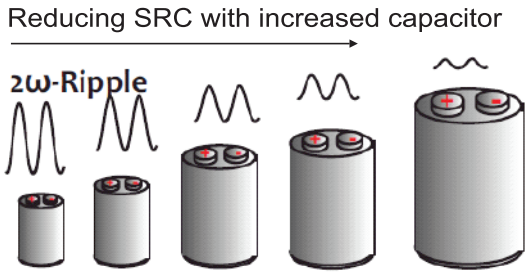

Figure 3.8 : A capacitor with a larger value is required to reduce the SRCs

In literature, various methods have been proposed to mitigate the SRCs. The methods can be categorized as passive methods, active methodologies and virtual control methodologies. In passive methodologies, the SRCs are mitigated by increasing the capacitance at the input terminals of the inverter as proposed in Krein *et al.* [2012] and reference therein. High-value low-cost capacitors are electrolytic. However, the electrolytic capacitors are not reliable Falck *et al.* [2018]. Hence, such methodologies lead to an increase in the cost and weight of the system and are lesser reliable. In terms of active methods, various actively controlled filters are presented in Vitorino *et al.* [2017] and references therein. These circuits consist of some capacitor or inductor to store and provide the ripple energy at different cycles, thereby reducing the SRCs. These are efficient compared to passive methodologies; however, extra circuitry is needed, which may lead to complex control and increase in cost. The third methodology focuses on regulating the output impedance of converter by control methodologies, as proposed in Zhang *et al.* [2018b],Zhang *et al.* [2015]. This method requires the inductor current or load current feedback and varies the control signal so as to increase the output impedance. This method is efficient as it does not requires any extra circuit. However, in some cases, a small value capacitor is needed to maintain the DC bus voltage within permissible limits.

3.1 PROPOSED METHODOLOGY

In this chapter, an SMC based control of single-stage inverters is proposed. Along with this, the inductor impedance shaping methodology is proposed by means of which the SRCs propagating to the source gets reduced. The proposed control is robust against modeling uncertainties. The inductor impedance shaping is presented for two single-stage dc-ac converters, which are - qZSI and eqSBI. All these converters have different topology, and they incorporate the shoot through to achieve voltage boosting. The proposed control increases the inductor impedance without affecting the boosting factor or the AC output.

3.2 CONTROL LAW FOR QZSI

A qZSI consists of a pair of inductors and capacitors. In qZSI, shoot through is achieved by turning all the switches of both the legs on at same time interval. The shoot-through state is incorporated between the dead time interval of traditional sinusoidal pulse width modulation of inverters. It is ensured that the load terminals are not shorted at any time instance. This is accomplished by keeping the sum of the shoot-through duty cycle and modulation index to be less than one. The averaged model of qZSI can be derived as:
During non-shoot through period,

$$L_1\frac{di_{L1}}{dt} = E - v_{c1} \qquad C_1\frac{dv_{c1}}{dt} = i_{L1} - i_{dc} \tag{3.3}$$

$$L_2\frac{di_{L2}}{dt} = -v_{c2} \qquad C_2\frac{dv_{c2}}{dt} = i_{L2} - i_{dc} \tag{3.4}$$

During shoot through period,

$$L_1\frac{di_{L1}}{dt} = E + v_{c2} \qquad C_1\frac{dv_{c1}}{dt} = -i_{L2} \tag{3.5}$$

$$L_2\frac{di_{L2}}{dt} = v_{c1} \qquad C_2\frac{dv_{c2}}{dt} = -i_{L1} \tag{3.6}$$

Averaging the dynamics over a switching cycle Erickson and Maksimovic [2001],

$$L_1\frac{di_{L1}}{dt} = E + d_{st}v_{c2} - (1-d_{st})v_{c1}, \quad L_2\frac{di_{L2}}{dt} = d_{st}v_{c1} - (1-d_{st})v_{c2} \tag{3.7}$$

$$C_1\frac{dv_{c1}}{dt} = -d_{st}i_{L2} + (1-d_{st})(i_{L1} - i_{dc}), \quad C_2\frac{dv_{c2}}{dt} = -d_{st}i_{L1} + (1-d_{st})(i_{L2} - i_{dc}) \tag{3.8}$$

For simplicity, let $L_1 = L_2 = L$ and $C_1 = C_2 = C$, E is the input source voltage, i_L is the inductor current, v_c is the capacitor terminal voltage, d_{st} is the shoot through duty cycle. Substitute in (3.7) and (3.8) and solve for differential of one inductor current and one capacitor voltage,

$$L\frac{di_{L1}}{dt} = (1-d_{st})E + (2d_{st}-1)v_{c1}, \; C\frac{dv_{c1}}{dt} = (1-2d_{st})i_{L1} - (1-d_{st})i_{dc} \tag{3.9}$$

Now, let the sliding surface chosen be:

$$s = e_i + \kappa e_v \tag{3.10}$$

where, e_i is the inductor current error ($i_L - i_{ref}$) and e_v is the voltage error ($v_c - v_{ref}$) and κ is a positive constant.To ensure that the dynamics reach the sliding surface, $\dot{s}$ should be Edwards and Spurgeon [1998],

$$\dot{s} = -\Gamma s - Qsgn(s) \tag{3.11}$$

Solve above equations for shoot through duty cycle,

$$d_{st} = \frac{LC(-\Gamma s - Qsgn(s)) - C(E - v_{c1}) - \kappa L(i_L - i_{dc})}{C(2v_{c1} - E) + \kappa L(i_{dc} - 2i_{L1})} \tag{3.12}$$

This shoot through duty cycle will be compared with the carrier signal to generate the signals for shorting the inverter legs to achieve voltage boosting.

3.3 CONTROL LAW FOR EQSBI

A eqSBI topology of single stage buck-boost inverter is small in size due to single inductor, and a single capacitor. It consists of an extra active switch, which is controlled with inverter switches to achieve shoot through. The averaged model of a eqSBI can be derived as:
During non-shoot through period,

$$L\frac{di_L}{dt} = E - v_c \quad C\frac{dv_c}{dt} = i_L - i_{dc} \tag{3.13}$$

During shoot through period,

$$L\frac{di_L}{dt} = E + v_c \quad C\frac{dv_c}{dt} = -i_L \tag{3.14}$$

where, L and C are the inductance and capacitance respectively, E is the input source voltage, i_L is the inductor current, v_c is the capacitor terminal voltage, d_{st} is the shoot through duty cycle. Combining above two equations to obtain averaged model of eqSBI,

$$L\frac{di_L}{dt} = E + (2d_{st} - 1)v_c \tag{3.15}$$

$$C\frac{dv_c}{dt} = (1 - 2d_{st})i_L - (1 - d_{st})i_{dc} \tag{3.16}$$

Now, let the sliding surface chosen be:

$$s = e_i + \kappa e_v \tag{3.17}$$

where, e_i is the inductor current error ($i_L - i_{ref}$) and e_v is the voltage error ($v_c - v_{ref}$). When the dynamics reach the desired references, the surface s would tend to zero. To ensure that the dynamics reach the sliding surface, $\dot{s}$ should be,

$$\dot{s} = -\Gamma s - Qsgn(s) \tag{3.18}$$

$$\dot{s} = \dot{e}_i + \kappa \dot{e}_v \tag{3.19}$$

Substitute values from (3.15) and (3.16) to (3.19),

$$\frac{1}{L}(E + (2d_{st} - 1)v_c) + \frac{1}{C}((1 - 2d_{st})i_L - (1 - d_{st})i_{dc}) = -\Gamma s - Qsgn(s) \tag{3.20}$$

From above equation, the shoot through duty cycle can be derived as:

$$d_{st} = \frac{LC(-\Gamma s - Qsgn(s)) - C(E + 2v_o) - \kappa L(i_L - i_{dc})}{\kappa L i_{dc} - 2(\kappa L i_L + 2Cv_o)} \tag{3.21}$$

This shoot through duty cycle in incorporated with the inverter modulating signal to boost the DC voltage.

3.4 CURRENT AND VOLTAGE REFERENCE AND DERIVATION OF BOUNDARY CONDITIONS

The current and voltage reference for both the qZSI and eqSBI converters is chosen depending on the converter's output AC voltage requirements. The current reference is generated by passing the inductor current through a low pass filter. Hence, the current reference is given as,

$$\frac{di_{ref}}{dt} = \frac{1}{\tau}(i_L - i_{ref}) \tag{3.22}$$

The choice of the time constant τ is necessary to ensure stability. The voltage reference is a fixed DC quantity which is required at the inverter input terminals.

3.4.1 Bounds for qZSI

The parameters of the switching surface κ and the low pass filter time constant τ is bounded to ensure reachability to the sliding surface. To ensure that the dynamics hit the sliding surface in finite time,

$$s\dot{s} < 0 \tag{3.23}$$

For the sliding surface, $s = (i_L - i_{ref}) + \kappa(v_c - v_{ref})$, when $s < 0$ then, $d_{st} = 1$ and $\dot{s} > 0$, using (3.9),

$$L\frac{di_{L1}}{dt} = v_{c1}, \;\; C\frac{dv_{c1}}{dt} = -i_{L1} \tag{3.24}$$

$$\dot{s} = \frac{di_{L1}}{dt} + \kappa\frac{dv_{c1}}{dt} > 0 \tag{3.25}$$

when $s > 0$ then, $d_{st} = 0$ and $\dot{s} < 0$, using (3.9),

$$L\frac{di_{L1}}{dt} = E + v_{c1}, \;\; C\frac{dv_{c1}}{dt} = i_{L1} - i_{dc} \tag{3.26}$$

$$\dot{s} = \frac{di_{L1}}{dt} + \kappa\frac{dv_{c1}}{dt} < 0 \tag{3.27}$$

Solve (3.25) and (6.4f) for the limits of κ,

$$0 < \kappa < \frac{CV_{ref}}{LI_{ref}} \tag{3.28}$$

3.4.2 Bounds for eqSBI

The κ for the sliding surface of eqSBI converter is derived as for qZSI converter. For the sliding surface, $s = (i_L - i_{ref}) + \kappa(v_c - v_{ref})$, when $s < 0$ then, $d_{st} = 1$ and $\dot{s} > 0$, using (3.15), and (3.16),

$$L\frac{di_L}{dt} = E + v_c, \;\; C\frac{dv_c}{dt} = -i_L \tag{3.29}$$

$$\dot{s} = \frac{di_{L1}}{dt} + \kappa\frac{dv_{c1}}{dt} > 0 \tag{3.30}$$

when $s > 0$ then, $d_{st} = 0$ and $\dot{s} < 0$, using (3.15), and (3.16),

$$L\frac{di_L}{dt} = E + -v_c, \;\; C\frac{dv_c}{dt} = i_L - i_{dc} \tag{3.31}$$

$$\dot{s} = \frac{di_{L1}}{dt} + \kappa\frac{dv_{c1}}{dt} < 0 \tag{3.32}$$

Solve (3.30) and (3.32) for the limits of κ,

$$0 < \kappa < \frac{C}{L}\frac{(V_{ref} - E)}{(I_{ref} - i_{dc})} \tag{3.33}$$

3.5 STABILITY OF PROPOSED CONTROL

The stability of proposed control can be analyzed using the Lyapunov's approach. Let the Lyapunov's function be,

$$V = \frac{1}{2}e_v^2 \tag{3.34}$$

During sliding mode, $s = 0$, i.e. $e_i = -\kappa e_v$. Hence, convergence of e_v to zero will ensure convergence of current error to zero. Differentiate (3.34) with respect to time and substitute value from (3.16),

$$\dot{V} = e_v((1-2d_{st})(e_1 + i_{ref}) - (1-d_{st})i_{dc}) \tag{3.35}$$

The value of shoot though duty cycle d_{st} lies between 0.5-1, also $(1-2d_{st}) < 1$ and $(1-d_{st}) > 0$,

$$\dot{V} = (1-2d_{st})i_{ref}e_v - \kappa e_v^2 - (1-d_{st})(v_c/Z) \tag{3.36}$$

where, Z is the load impedance. The term $(1-2d_{st})i_{ref}e_v$ is negative definite as when $e_v > 0$, $(1-2d_{st})i_{ref} < 0$ and when $e_v < 0$, $(1-2d_{st})i_{ref} > 0$. Hence, the function $\dot{V}$ is negative definite and the voltage and current error asymptotically converge to zero Edwards and Spurgeon [1998]. Hence, the system with proposed controller is stable.

3.5.1 Derivation of low pass filter time constant for current reference generation

The low pass filter time constant τ has a significant role for system stability and impedance shaping. The bounds on the value is derived by deriving the small signal model of the converter. Here, the small signal modelling, and τ of a eqSBI is derived. Similar derivation can be carried out for qZSIs. The state space model with small perturbations in i_L, v_c and i_{ref} as $\hat{i}_L$, $\hat{v}_c$ and $\hat{i}_{ref}$, and duty cycle perturbation is $\hat{d}$ is,

$$\dot{\hat{x}} = A\hat{x} + B\hat{d} + C \tag{3.37}$$

where, $\hat{x} = [\hat{i_L} \quad \hat{v_c} \quad \hat{i_{ref}}]^T$, $A = \begin{bmatrix} 0 & \frac{2D-1}{L} & 0 \\ \frac{1-2D}{C} & 0 & 0 \\ \frac{1}{\tau} & 0 & -\frac{1}{\tau} \end{bmatrix}$, $B = \begin{bmatrix} \frac{2V_C}{L} \\ \frac{-2I_L}{C} \\ 0 \end{bmatrix}$, $C = \begin{bmatrix} \frac{E-V_c}{L} \\ \frac{I_L}{C} \\ 0 \end{bmatrix}$, and V_c,I_L and D are steady state values of capacitor voltage and inductor current and duty cycle respectively. When the system is in sliding regime i.e. $s = (i_L - i_{ref}) + \kappa(v_c - v_{ref}) = 0$, $\dot{s} = (\dot{i_L} - \dot{i_{ref}}) + \kappa\dot{v_c} = 0$ and then the third order system can be reduced to a second order system. Also, the duty cycle perturbation can be written in terms of the small signal voltage and current perturbations.

$$\hat{d} = \frac{1}{\beta}\left(\frac{\hat{i}_L - \hat{i}_{ref})}{\tau} - \frac{\kappa(I_L + (1-2D)\hat{i}_L)}{C} - \frac{(E-V) + (2D-1)\hat{v}_c}{L}\right) \tag{3.38}$$

where, $\beta = \frac{2V}{L} - \frac{2\kappa I_L}{C}$.

Finally, substituting all values and deriving condition of τ such that the coefficients of characteristic equation is always positive gives,

$$\tau < \frac{\kappa}{\frac{2\kappa V(1-2D)}{LI_L} - \frac{(2D-1)}{L}} \tag{3.39}$$

The above equation is used to determine the time constant of the low pass filter.

3.6 EFFECT OF LOW PASS FILTER TIME CONSTANT ON INDUCTOR IMPEDANCE

In this section, the effect of time constant τ of low pass filter on input inductor impedance will be analyzed for a eqSBI converter. Similar method can be used to derive the effect on input inductor of a qZSI. Using (3.16) and (3.15), the inverter input voltage v_{dc} and current through the inductor in Laplace domain can be derived as,

$$i_L(s) = \frac{E + (2d_{st} - 1)v_c(s)}{sL}, \quad i_{ref} = \frac{i_L}{(s\tau + 1)} \tag{3.40}$$

$$v_c(s) = \frac{(1 - 2d_{st})i_L(s) - (1 - d_{st})i_{dc}}{sC}, \quad v_{dc} = d_{st}E + v_c(s) \tag{3.41}$$

Using above equations, the impedance at the inverter input DC terminals is derived as,

$$\frac{v_{dc}}{i_L} = \frac{L}{C}\left(\frac{(1 - 2d_{st})i_L(s) - (1 - d_{st})i_{dc} + d_{st}E}{E + (2d_{st} - 1)v_c(s)}\right) \tag{3.42}$$

During steady state, the inductor current $i_L(s)$ and $v_c(s)$ will become i_{ref} and v_{ref}.

$$\frac{v_{dc}}{i_L} = \frac{L}{C}\left(\frac{(1 - 2d_{st})i_{ref}(1 + s\tau) - (1 - d_{st})i_{dc} + d_{st}E}{E + (2d_{st} - 1)v_{ref}}\right) \tag{3.43}$$

Hence, from (3.43) it can be observed that as the parameter τ increases, the impedance of the DC terminals will increase and prevent the second order ripple currents from entering the source. However, the parameter τ must be increased upto the bounds defined in the earlier section.

3.7 PWM GENERATION LOGIC

The gate pulses required to drive the shoot through based DC-AC inverters consists of incorporating a stage in which all the switches of two legs are turned on during shoot though interval. At other time intervals, it is similar to the sine wave pulse width modulation. The shoot-through duty cycle d_{st} is generated by the SMC controller such that $d_{st} + m < 1$ so that the power stage does not gets shorted. The modulation index regulates the maximum value of reference sine wave, which is compared with the repeating sequence. The magnitude of m must be regulated to obtain lower harmonic content in output voltage. The logic used to generate gate pulses for qZSI is shown in Figure 3.9, and for eqSBI is shown in Figure 3.10. An instance of simulation of gate pulse is shown in Figure 3.11 for qZSI and in Figure 3.12 for eqSBI. The shoot-through states can be observed in switch signals $S_1 - S_4$. In eqSBI, five switching signals are required $S_1 - S_5$. The shoot-through signal is common between switches $S_1 - S_4$ and S_5. In this case, the logic similar to Ravindranath *et al.* [2013] is used. An instance of gate pulses for experimentation on eqSBI is shown in Figure 3.13, and Figure 3.14.

3.8 SIMULATION RESULTS

A qZSI and eqSBI is simulated in Matlab to verify the proposed control law for output AC voltage control and ripple reduction. The parameters for simulation in given in Table-I. The parameters similar to Nguyen *et al.* [2015c] are used for simulation and experimentation.

3.8.1 SRC control for qZSI

The simulated waveforms of input voltage E, inverter output AC voltage v_{ac} and inductor current I_L is shown in Figure 3.15. Before the time interval t_1, the SRC is not regulated and the

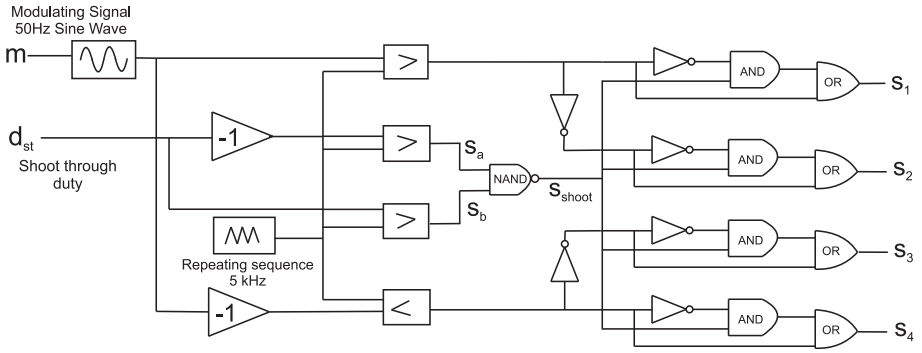

Figure 3.9 : Switching logic for qZSI

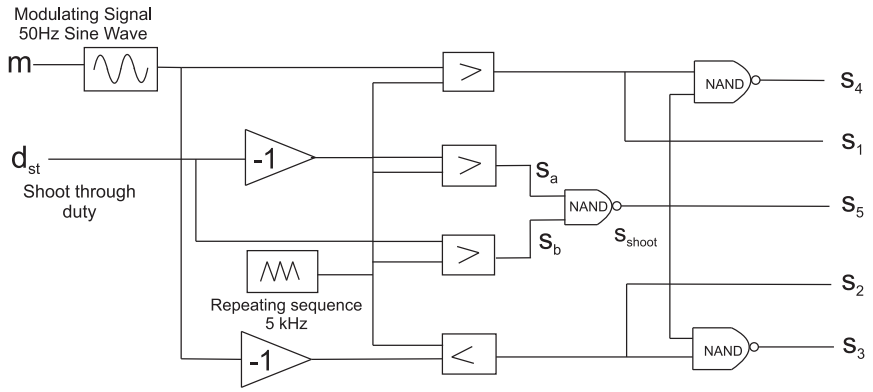

Figure 3.10 : Switching logic for eqSBI

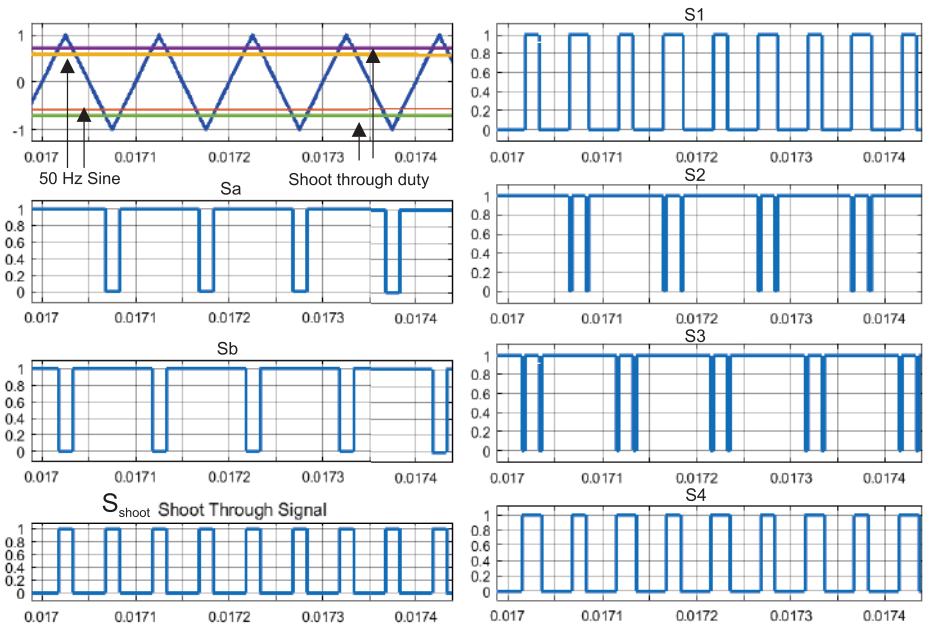

Figure 3.11 : Simulation of gate pulses for shoot through in qZSI

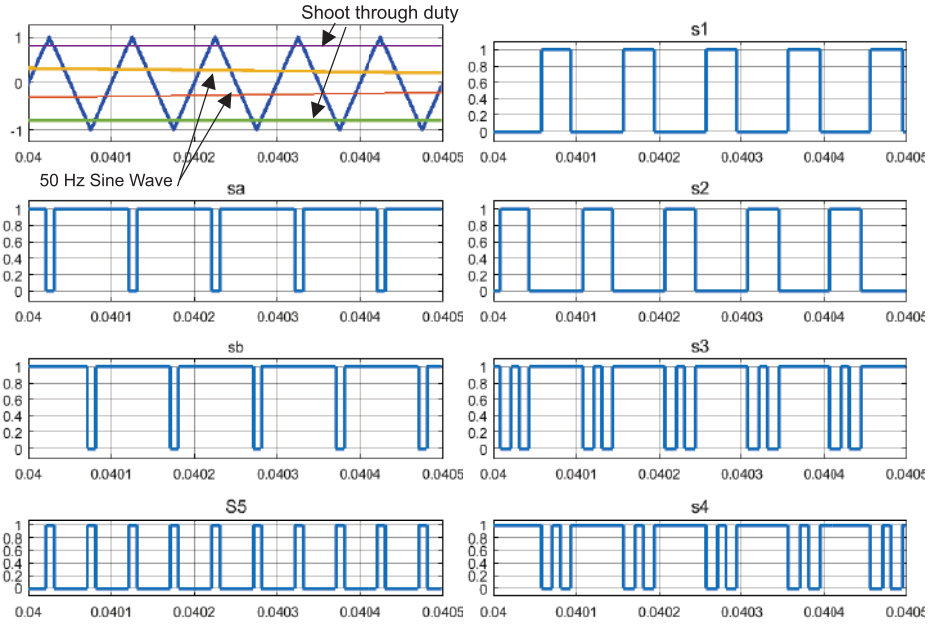

Figure 3.12 : Simulation of gate pulses for shoot through in eqSBI

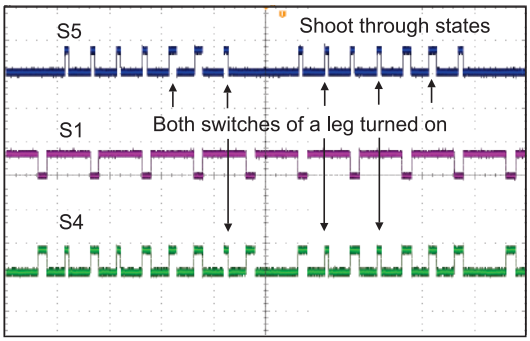

Figure 3.13 : An instance of SPWM with shoot through for switches S_1, S_4 and S_5 for qSBI converters

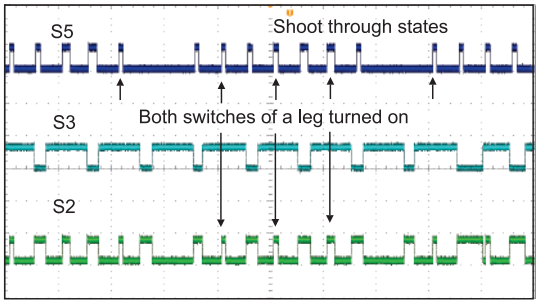

Figure 3.14 : An instance of SPWM with shoot through for switches S_2, S_3 and S_5 for qSBI converters

Table 3.1 : Simulation and experimental parameters

Parameters	Symbol (Unit)	qZSI	eqSBI
Inductor	L (mH)	1.5	3
Capacitor	C (μF)	1000	470
Carrier Frequency	f_c (kHz)	10	10
Inverter Output frequency	f_{ac} (Hz)	50	50
AC inverter load	r_{ac} (Ω)	100-50	100-50
Voltage reference	v_{ref} (V)	110	110
Time constant	τ (ms)	0.04	
Reachability parameters	Γ, Q	20000,2000	

value of low pass filter time constant is Γ. During the time interval t_2 and t_3, the time constant is increased and the SRC can be seen to be reduced from 2A to 1A to 0.7A. However, the time constant can be increased upto a bound defined in earlier sections. The output AC voltage remains constant irrespective of SRC regulation.

3.8.2 SRC control of eqSBI

The simulated waveforms are shown in Figure 3.16. It can be observed that as the filter time constant in varied, the SRC propagating through the inverter reduces from 2A to 0.8A to 0.2A, and the output AC voltage remains as desired. During time interval t_1 time constant is 2Γ and during t_2 time constant is 4Γ. Hence, the proposed impedance increase using a low pass filter is verified using simulation.

3.9 EXPERIMENTAL RESULTS

The proposed SMC based control strategy is verified for a 200W eqSBI, as shown in Figure 5.16. The inverter input voltage and inductor currents are measured and fed through an analog to digital converters pins of the OPAL-RT Real-Time Digital Simulator. The ACS 709T and Lem 25-P sensors are used to measure current and voltage, respectively. The IGBT module FGH40N120ANTU is used as switch S_5, and SKM75GB128D are used for inverter legs. A controlled DC source is of 60V, 10A is used to supply input power to the eqSBI. In similar way, the controller can be verified for qZSI. The results are discussed under following subsections-

3.9.1 DC voltage boost, without impedance control

The desired voltage reference is set to $\sqrt{2}\ V_{rms}$ to obtain the required AC output voltage of 90V rms. The input DC voltage is 40V. The inductor current consists of 100 Hz second order ripple of 0.35A as shown in Figure 3.18. This SRC has to be reduced. Hence, the required voltage boosting is achieved.

3.9.2 With Impedance control

The impedance of the inductor is increased virtually using the proposed control. This leads to the reduction in SRC as shown in Figure 3.19. The SRC gets reduced to 0.35A to 0.05A. The ripple power is provided by the capacitor. The output voltage remains constant and is not affected by

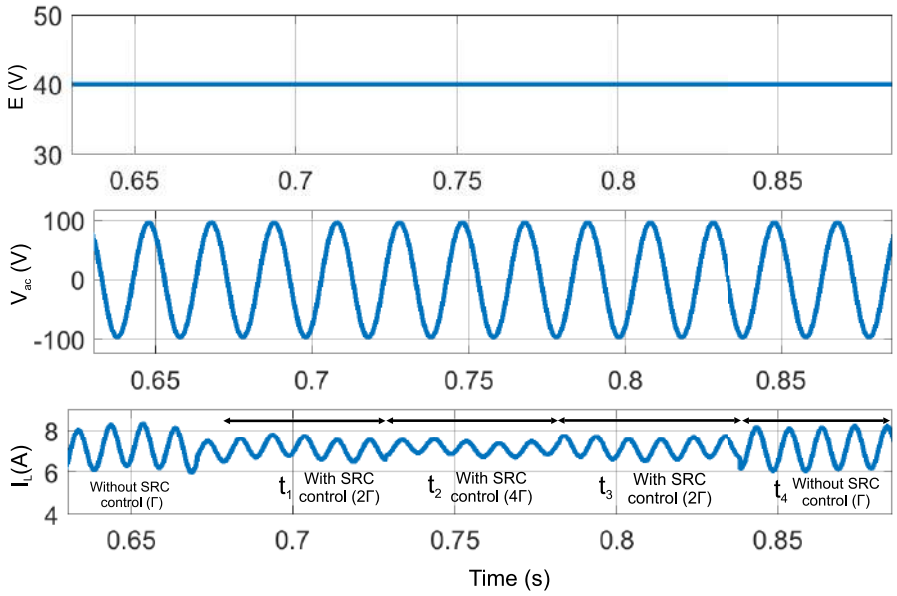

Figure 3.15 : Simulation of qZSI

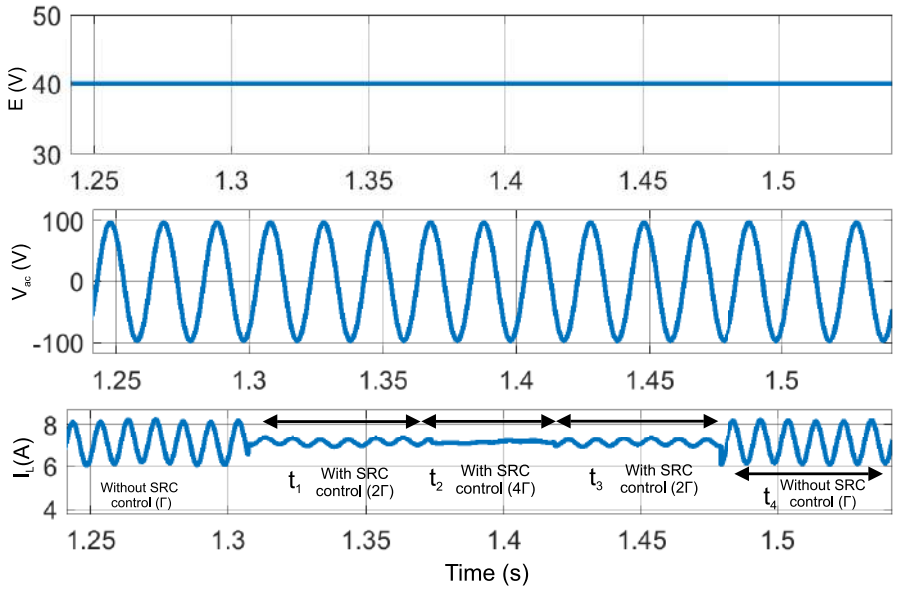

Figure 3.16 : Simulation of eqSBI

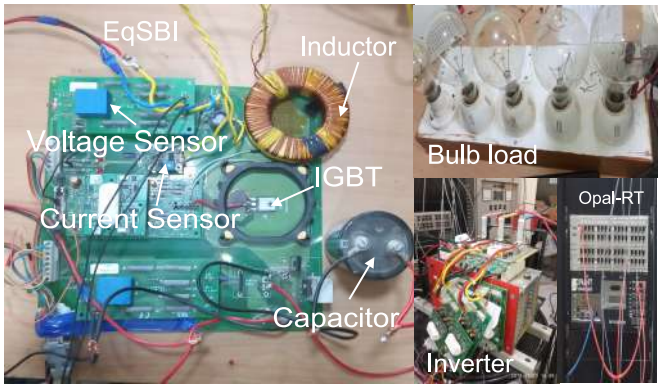

Figure 3.17 : Hardware setup

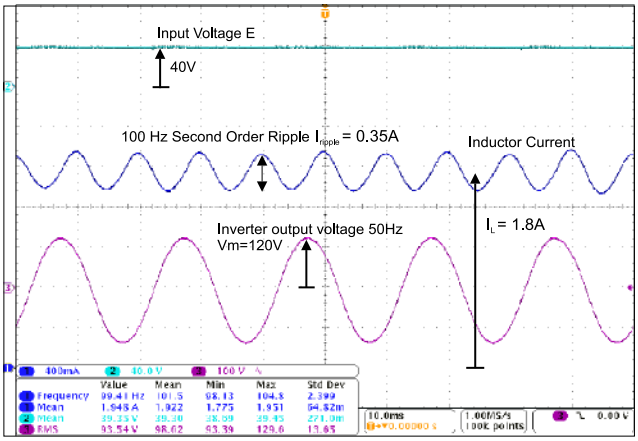

Figure 3.18 : Output inverter voltage and inductor current with SRC

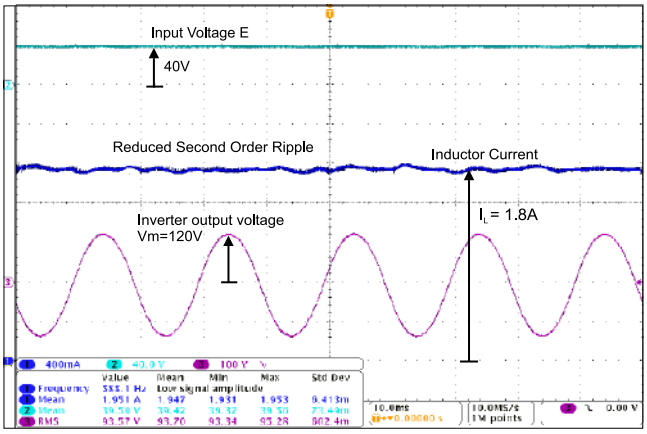

Figure 3.19 : Output inverter voltage and inductor current with SRC control

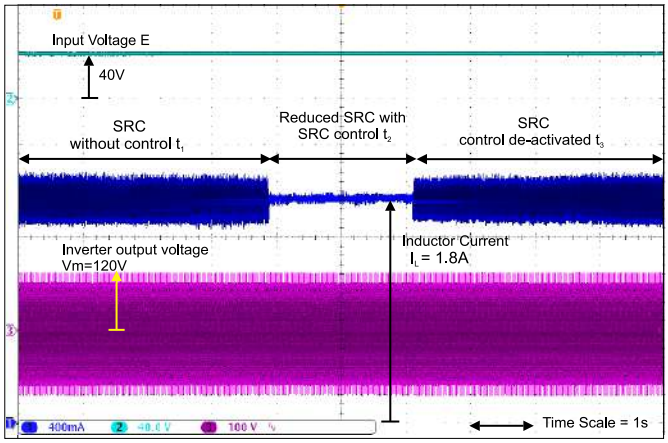

Figure 3.20 : Waveforms with and without impedance control

the impedance control.

3.9.3 Ripple control explaination

During the time interval, t_1 the impedance control is not implemented. The inductor current consists of SRC as shown in Figure 3.20. During the time interval t_2, the control is implemented, and the SRC starts to reduce. The control is again de-activated during a time interval of t_3. The SRC again increases. This shows that the ripple control effectively reduces the ripple propagating to the source while keeping the inverter output voltage constant. The SRC reduction with slow variation of the low pass filter time constant is shown in Fig. 3.21. It can be observed that as the low pass filter time constant is reduced the ripple keeps on reducing and when it is increased, the ripple restores to initial value. The time constant value is varied within the range defined in the earlier Sections.

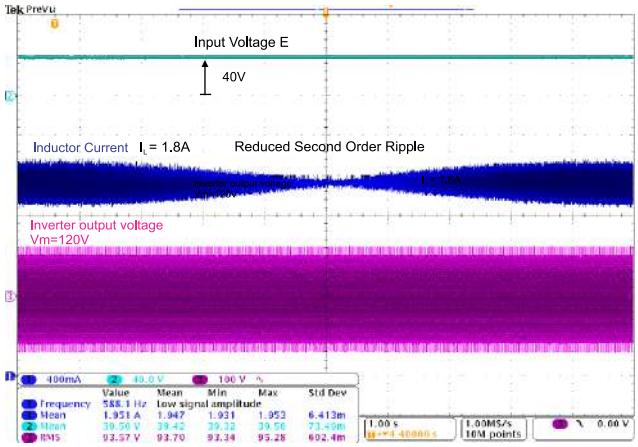

Figure 3.21 : Waveforms with low pass filter time constant variation

3.10 CONCLUSION

A sliding mode control based AC voltage control of single-stage qZSI and eqSBI has been presented. The proposed controller effectively reduces the second-order ripple currents while keeping the desired AC voltage level. The effect of using a low pass filter for the current generation to increase the impedance of inductor is verified. The simulation and experimental results verify that the ripple gets reduced from 2A to 0.7A in qZSI and from 2A to 0.2A in eqSBI without the addition of any external circuitry and 90V rms AC voltage. Hence, the proposed controller is applicable for control and SRC reduction in low power single-stage qZSI and eqSBIs.

The SRCs must be mitigated from the source currents in presence of any uncertainties. To achieve this, an integration of a non-linear control with a nominal control is proposed in next chapter. The control consists of a dual loop voltage and current control and an integral sliding mode control (ISMC). The ISMC control mitigates the SRCs and also makes the converter operate as desired in presence of matched uncertainties. The ISMC is designed so that the unmatched uncertainties are not amplified. The control law obtained from the ISMC is added with the control law obtained from the dual loop control. The control design procedure has been presented for both the qZSI and eqSBI converters.