5

Dynamic Virtual Impedance based Second Order Ripple Regulation in DC Microgrids

In previous chapters the robust SRC control techniques for SSIs has been presented. The SRCs occur on the DC end during DC-AC conversion. The SRCs occur in the DC Microgrid voltage and source currents when an AC load is connected to the microgrid. The SRCs gets distributed among the nodes depending on the impedance of the line connecting the converter to the DC bus. The node with higher line impedance gets less share of SRCs compared to the node with less line impedance. It also depends on the output impedance of the interfacing converter. In this chapter a dual loop control with an impedance loop is proposed to regulate the SRC propagation to a node. The impedance control loop regulates the output impedance of the converter virtually. The proposed control has been verified for a two node DC Microgrid. The virtual impedance obtained is compared analytically with conventional passive SRC reduction methodologies.

A DC microgrid is an integration of distributed generation units, storages, and loads to a common bus. It has various advantages over the existing power generation and distribution system such as higher efficiency, remote availability, easier control, and higher reliability. As a result, there is an increasing penetration of DC microgrids into the existing power systems. This results in the need of efficient integration of both the systems so as to maintain stability and also optimize the overall integrated system. In terms of DC microgrid, primary concerns are proportional load sharing, optimal management of energy generated, DC bus voltage regulation etc. Integration of the DC microgrid with existing grid requires DC-AC power conversion. In case of DC to single phase AC conversion, second order oscillations are reflected on DC side voltage and source currents. Since, in DC microgrid, the DC bus voltage is controlled to be within voltage regulation limits, the second order ripple are primarily in the source currents. These second order ripple currents (SRCs) propagate through the DC-DC converters to the sources and have various detrimental effects.

The SRCs affect the maximum power point tracking as they introduce second order oscillations in the voltages and currents Kan *et al.* [2019]; Liu *et al.* [2014]. They cause heating issues in photo-voltaic (PV) panels. They also increase the stress on wind turbines (WT), due to oscillations in torque Peña-Alzola *et al.* [2017]. In terms of batteries, they cause heating issues IEE [2014],IEE [2006]. The ripple current must be kept below 8% of the rated current Dong *et al.* [2013]. Hence, the SRCs cause degradation of components and lead to reduction in operating life span of sources and energy storages and, there is a need to efficiently manage the SRCs in the DC microgrid.

In literature, various active and passive methods have been proposed to mitigate the SRCs, and to improve the DC power quality. The passive methodologies consists of increasing the capacitance and inductance to absorb the SRC component. However, increasing the component size will lead to over sizing and the cost of system increases. Increased size of components degrades the dynamics of the microgrid system. This will be analyzed in later sections. Furthermore, to minimize cost bulky electrolytic capacitors may be used, but these capacitors are the weakest element in the system due to lesser life span compared to other components Almeida *et al.* [2015];

Wang and Blaabjerg [2014]. A review of different active power decoupling topologies is presented in Sun *et al.* [2016]. Adding such decoupling circuits to various nodes in the DC microgrid will increase the component count and cost of the microgrid system. The virtual impedance methods are used to regulate the input or output impedance, without using any additional component. In Zhang *et al.* [2014], authors propose a band pass filter based inductor current feedback scheme (BPF-ICFS) to incorporate virtual impedance. A notch filter based load current feedforward scheme (NF-LCFFS) is proposed in Zhu *et al.* [2015] to improve dynamics. A comparison of various such schemes is presented in Zhang *et al.* [2015]. However, such methodologies are proposed for two stage DC-AC conversions. Also, the load current feedforward schemes have been proposed to improve dynamics. However, in case of DC microgrid, communicating the load current value to individual source converters will increase the complexity of the system. In terms of ripple sharing in DC microgrid, various methods have been proposed as in Hamzeh *et al.* [2015]; Jia *et al.* [2017a], however proportional load sharing has not been addressed. In Tian and Li [2021], a notch filter and resonant regulators are incorporated in the control loop of the converters to reduce the second order ripple component. In Liu *et al.* [2020b], authors propose an SRC control method where a band-pass filter and virtual resistance is incorporated in the control loop to reduce the SRCs. Both the methods are applicable to the microgrid feeding AC loads. The SRC reduction issue is well addressed. However, the microgrid dynamics with respect to the secondary control is not addressed. The critical design parameters as communication delay between the nodes must be taken into consideration in presence of virtual impedance methodology to analyze its effect on stability. The effect of virtual impedance method to reduce SRC in comparison with converter parameter variation to reduce SRC should be analyzed.

In this paper, a dynamic virtual impedance (DVI) scheme is proposed to manage the SRCs in distributed environment like DC microgrid. The proposed control mechanism is shown in Fig. 7.1. It shows the DC bus feeding both AC and DC loads. The overall load gets distributed such that node-2 gets more loaded due to unequal line resistances R_{line} and output impedance of interfacing converters. The power P demanded from loads are shown in corresponding waveforms. The oscillations in inductor current is observed due to AC loads, as shown in Fig. 7.1a. The proposed DVI control will introduce a virtual impedance of R_d for DC load sharing and Z_v for ripple sharing as shown in Fig. 7.1b. The proposed DVI will regulate the droop constant $R_{d2} > R_{d1}$ to increase DC component load share of node-1. It also controls the impedance at $2f_{ac}$ to be $Z_{v1} > Z_{v2}$ to reduce the SRC in node-1. It can be observed that the proposed control propagates the ripple to one of the nodes. The capacitance at node-2 can be increased to absorb the ripples or some active filters can be installed. In case of a multi-node system the proposed DVI will facilitate the filter installation at a node instead of installing at multiple nodes. The proposed DVI regulates the output impedance virtually by a ripple controller, which compares the ripple reference with the magnitude of SRC. The magnitude of SRC is obtained by passing the inductor current through the second order general integrator (SOGI) tuned at $2f_{ac}$. Along with this, a communication network is used to facilitate per-unit current data exchange between the nodes. Using this, a secondary controller is incorporated to achieve proportional load sharing among all nodes with a good voltage regulation. The salient features of DVI based method are:

1. SRCs are prevented to propagate through the interfacing converter to the source or storage such that, higher the impedance at $2f_{ac}$ lower will be the SRC.
2. The DC component of load current is shared proportionally. The DC bus voltage is maintained within limits, with a good voltage regulation. For this, the per-unit load value is shared between neighboring nodes. A sparse communication network can be used for load sharing.
3. The proposed DVI SRC control is analyzed with communication delays between nodes. The system becomes more stable in case of communication delay with SRCs by implementing the proposed control.

The paper is organized as follows: Section II consists of modeling of interfacing converter. The impedance shaping with proposed inverse notch filter is explained in this section. The

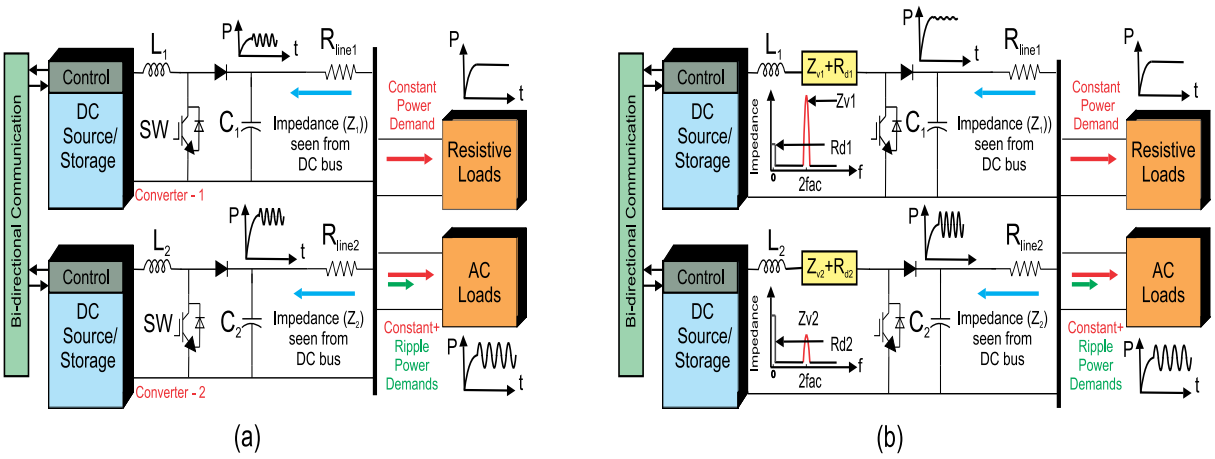

Figure 5.1 : Proposed SRC and DC component sharing (a) Without any virtual imedance control, (b) With DVI control- The virtual impedance $Z_{v1} > Z_{v2}$ hence, $SRC_1 < SRC_2$. Similarly, $R_{d1} < R_{d2}$ to share DC component equally.

methodology of controller designing is presented in sections III and IV. The stability analysis is prsented in section V. The analysis with difference scenarios like capacitance and inductance variations, communication delays, and virtual impedance variation is discussed. The section VI consists of simulation results and related explanations. Experimental validation of proposed method is presented in section VII.

5.1 OUTPUT IMPEDANCE SHAPING

A boost converter connected to a DC bus can be modeled using state space averaging as:

$$L_i \dot{i}_{Li} = -r_{L_i} i_{Li} - (1-d_i)v_o + v_{dci} \tag{5.1}$$

$$C_i \dot{v}_o = (1-d_i)i_{Li} - i_{oi} - \sum_{j \varepsilon N_i} i_{ij} \tag{5.2}$$

where, for i^{th} converter L_i is the inductor, C_i is capacitor value, d_i is duty cycle, r_{Li} is inductor series resistance, v_{dci} is the source voltage, v_o is the output voltage, i_{Li} is inductor current, i_{oi} is output current, i_{ij} is the current between nodes i and j. The current $i_{oi} + \sum_{j \varepsilon N_i} i_{ij}$ can be replaced by $\frac{v_o}{Z}$, where Z is the output impedance seen from converter. Consider a small perturbation around the desired operating point (V_o, I_{Li}):$v_o = V_o + \hat{v_o}$, $i_{Li} = I_{Li} + \hat{i_{Li}}$, $d_i = D_i + \hat{d_i}$ and derive control to output voltage and control to inductor current transfer functions as:

$$T_{vod}(s) = \frac{(1-D_i)V_o - s(LI_{Li})}{(LC)s^2 + \frac{sL}{Z} + (1-D_i)^2} \tag{5.3}$$

$$T_{iLd}(s) = \frac{s(CV_{vi}) + 2(1-D_i)I_{Li}}{(LC)s^2 + \frac{sL}{Z} + (1-D_i)^2} \tag{5.4}$$

The above voltage to control transfer function $T_{vod} = \hat{v_o}(s)/\hat{d_i}(s)$, and inductor current to control transfer function $T_{iLd} = \hat{i_{Li}}(s)/\hat{d_i}(s)$ are used to derive the PI control gain parameters. The SRC in the source current depends on the impedance of the interfacing converter, as seen from the

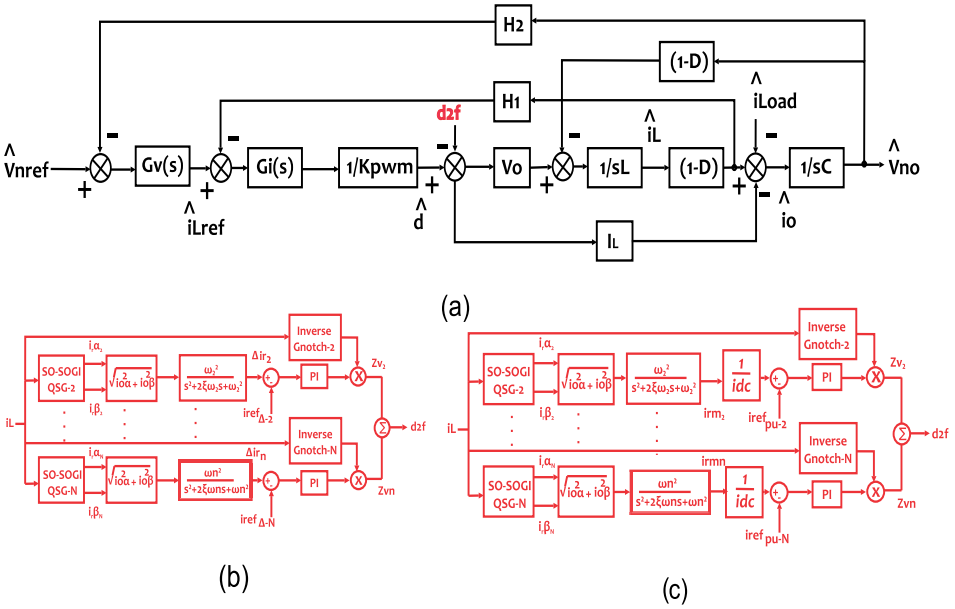

Figure 5.2 : (a) Proposed DVI control, (b) Proposed DVI with Δi_L as reference,(c) Proposed DVI with $iref_{puN}$ as reference

dc bus. To reduce the SRCs, the impedance must be greater than the impedance of the DC bus capacitor. To regulate the SRC content, a virtual impedance loop is incorporated by a feedback of inductor current. This feedback loop consist of an inverted notch filter with peak at $2f_{ac}$, to regulate the SRC. The control consists of inner current controller $G_i(s)$ and outer voltage controller $G_v(s)$. Small signal model of the interfacing converter is shown in Fig.5.2(a) where, H_1 and H_2 are the current and voltage sensor gain respectively and Kpwm is PWM gain. The transfer function of $\frac{\hat{v}_o(s)}{\hat{i}_L(s)}|_{\hat{d}=0,\hat{v}_{in}=0,\hat{i}_{Load}=0}$ with virtual impedance $Z_v(s)$ can be derived to be,

$$\frac{\hat{v_o}(s)}{\hat{i_L}(s)} = \frac{K_{pwm}(sL + \frac{Z_v}{G_N}) + \frac{1}{(1-D)}(V_o G_i - sG_i I_L)}{sLG_v G_i I_L - (1-D)^2(K_{pwm} + G_v G_i V_o)} \tag{5.5}$$

From (5.5) it can be seen that the inverted notch $G_N(s)$ will add an impedance of Z_v to the output impedance. However, the voltage controller $G_v(s)$ and current control $G_i(s)$ also affect the output impedance. The Z_v must be dynamic so that irrespective of control parameter changes or load variations, the output impedance remains at some desired value.

5.2 PROPOSED SECOND ORDER IMPEDANCE CONTROL

In this section, the proposed method for second order impedance control is explained. The control loops consists of an inner current control loop and an outer voltage control loop as shown in Fig.5.2a. The SRC control loop is designed in two ways as shown in Fig.5.2b,c. The figure shows a SRC control loop for n^{th} order ripple. The primary step is to find out the ripple content in the inductor current. For this, the inductor current i_L is passed through the second order general integrator quadratic signal generator (SO-SOGI QSG) to obtain the α and β components $i_{o\alpha}$ and $i_{o\beta}$ respectively. The SOGI can be tuned to filter out n^{th} harmonic component, to reduce ripples at various other frequencies. In Xin *et al.* [2016], authors describe SO-SOGI QSG methodology to

generate quadrature signals. Once the ripple component is extracted, it can be compared with- (a) The desired ripple content $i_{ref\triangle-n}$ or (b) The desired ripple with respect to the DC component (which should be $<$ than 8%). The resultant control signal d_{2f} is incorporated in the dual loop. The SRC reference $i_{refpu-N}$ is used when the converter rating is known to the designer. On the other hand, when the magnitude of ripple current propagation to the converter is known then the SRC reference $i_{ref\triangle-n}$ must be used.

5.2.1 Reduction of magnitude of ripple content $i_{ref\triangle-n}$

In this method, the magnitude of SRC is reduced irrespective of the direct current magnitude. The methodology is shown in Fig.5.2b. The SRC reference $i_{ref\triangle-n}$ represents the reference for n^{th} order ripple. However, here we primarily focus on the SRCs. The virtual impedance Z_v is adjusted by controller such that to reduce $i_{ref\triangle-n}$, the Z_v increases. This leads to increase in impedance and the SRC reduces considerably. The SRC sharing can be achieved by giving seperate SRC references for each node. Hence, SRC reference for node with some filter component can be increased compared to other nodes.

5.2.2 Reduction of maximum ripple current to DC ratio- i_{rm}/i_{dc}

In this methodology, the ratio of ripple current with respect to the direct current is minimized. This ratio must be less than 8% as stated earlier. The methodology is shown in Fig.5.2c. The PI controller for this must be tuned such that the i_{rm}/i_{dc} converges to per unit SRC reference $i_{refpu-N}$, where i_{dc} is dc component of load current. When the ratio is greater than $i_{refpu-N}$, the virtual impedance Z_v increases and when ratio is less, the virtual impedance decreases. This results in increase in second order impedance and the SRC is reduced as per the reference used. Further, the minimum value of Z_v is zero so that in absence of AC load, the $2f_{ac}$ virtual impedance is negligible.

5.3 CONTROLLER PARAMETER DESIGN

The source interfacing converters are designed to operate at a frequency much higher that the $2f_{ac}$. As a result, the passive components are to eliminate a higher switching frequency terms in voltages and currents. The output impedance is much lower than the DC bus capacitor, which leads to SRC propagation to these nodes. The proposed control alters the impedance at $2f_{ac}$ frequency without the need of increasing the passive component size. The proposed DVI second order impedance control consists of a PI control block apart from the inner current control loop and the outer voltage control loop. The control design consists of selection of control gains such that the inner, outer, and ripple control loop operate at different time scales so as to maintain the desired stability. Inner current control $G_i(s)$ loop is designed to have faster dynamics compared to the outer voltage loop. For this, the gain crossover frequency ω_c is chosen to be about $1/10^{th}$ of the gain crossover frequency of the $\hat{v_o}/\hat{d}$ transfer function. The phase margin at gain crossover frequency is chosen to be 60^o. The output of the inner control is the duty cycle value which is compared with the carrier to generate the switch control signals. The control designed should alter the frequency response to have high gain at low frequency and low gain at higher frequencies as shown in Fig.5.3. The proposed DVI controller regulates Z_v so as to obtain the desired impedance as shown in Fig.5.4. The virtual impedance Z_v is made to operate only at $2f_{ac}$ by the inverted notch filter. The transfer function of an inverted notch filter is:

$$G_N(s) = \frac{s^2 + \frac{2w_n s}{Q} + w_n^2}{s^2 + w_n^2} \tag{5.6}$$

where, Q is the quality factor and ω_n the frequency where the impedance is to be regulated.

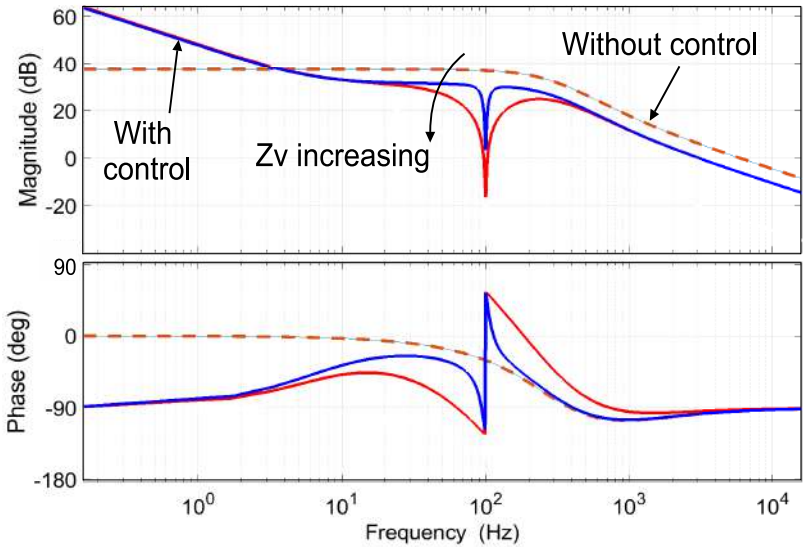

Figure 5.3 : Bode plot of $\hat{i}_L/\hat{d}$ with Z_v

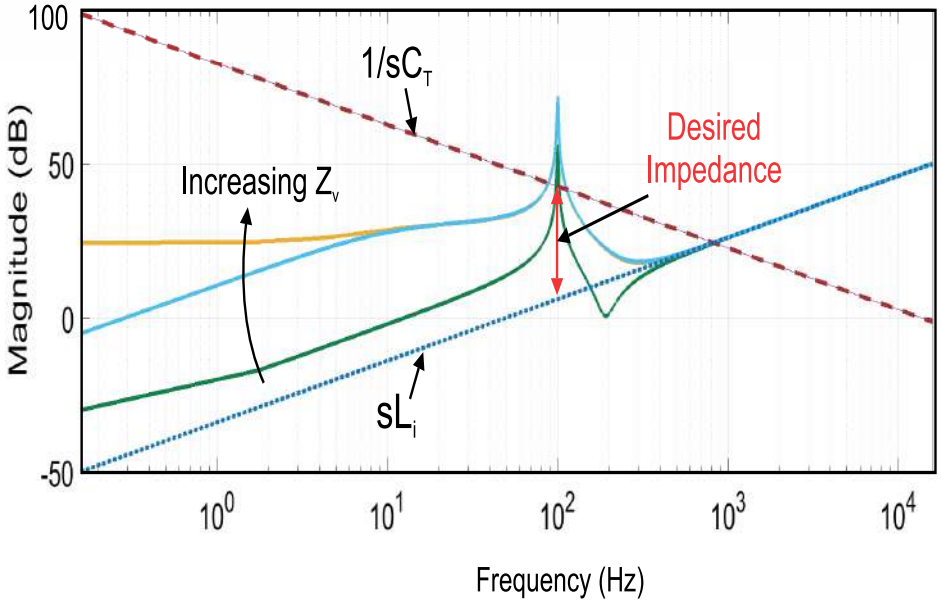

Figure 5.4 : Output impedance with different Z_v

The ripple control PI control is $G_r(s) = K_{pr} + K_{ir}/s$, then the loop gain at $2f_{ac}$ will be limited by the allowable voltage regulation allowed. If V_o is the output voltage, V_{in} is the input voltage, and duty cycle $d = 1 - \frac{V_{in}}{V_o}$ and ΔV_o is voltage regulation feasible then the duty cycle Δd can be derived as:

$$\Delta d = \frac{\Delta V_o V_{in}}{V_o(V_o + \Delta V_o)} = \frac{\Delta V_o(1-d)}{(V_o + \Delta V_o)} \tag{5.7}$$

To determine the values of control gains, the loop gain of ripple control loop and phase margin constraints are evaluated. The loop gain of the ripple controller with the inductor current to duty

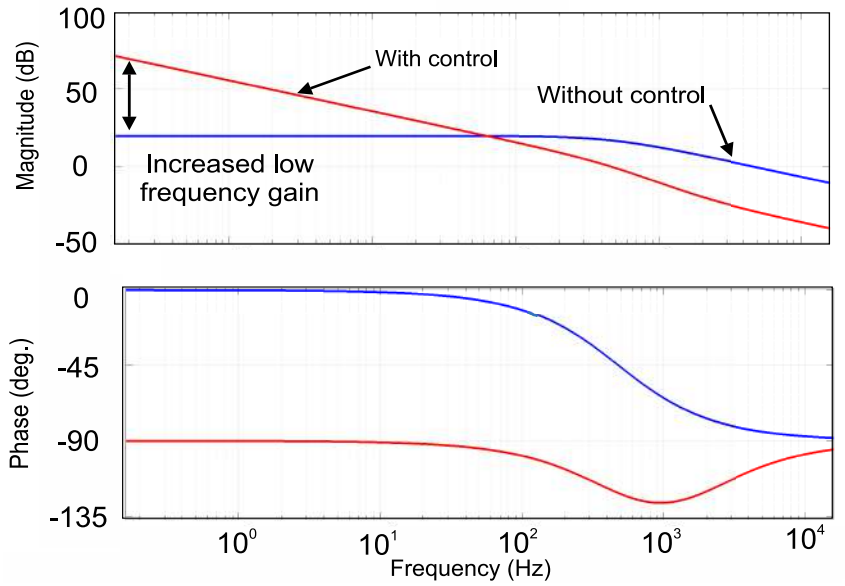

Figure 5.5 : Bode plot of $\hat{v}_o/\hat{d}$

cycle transfer function must be less than the Δd duty cycle value at $2f_{ac}$.

$$\left(K_{pr}+\frac{K_{ir}}{s}\right)\left(\frac{sCV_o+2(1-D)I_L}{s^2+sL/Z+(1-D)^2}\right)\Bigg|_{2fac} < \Delta d \tag{5.8}$$

Substitute s=jω, where ω=2πf_{ac}, and simplify and re-arrange to get limits of control gain,

$$(K_{ir}^2+w^2K_{pr}^2) < \Delta d^2\frac{[(2(1-D)I_L-w^2L/Z)^2+(w^3L/Z)^2]}{(2(1-D)I_L)^2+(wCV_o)^2} \tag{5.9}$$

Now, for phase margin (PM) constraint,

$$180^o+\angle T_{iLd}G_r = PM \tag{5.10}$$

$$\left(\frac{wK_{pr}}{K_{ir}}\right) = tan\left(PM-180^o-tan^{-1}\left(\frac{wCV_o}{2(1-D)I_L}\right)\right.$$

$$\left.-tan^{-1}\left(\frac{w^3LC}{2(1-D)I_L-w^2L/Z}\right)\right) \tag{5.11}$$

Using (5.9) and (5.11), the gain of G_r is found so as to regulate SRC through a node by regulating the output impedance. The outer voltage controller $G_v(s)$ is designed to generate the current reference corresponding to some voltage error. The voltage error is the difference between the actual and desired output voltages. This controller is designed to be slower than the current controller. The gain crossover frequency voltage control block ω_v is taken to be less than the $2f_{ac}$ frequency so as to attenuate any ripple in the voltage value as shown in Fig.5.5. Along with this,

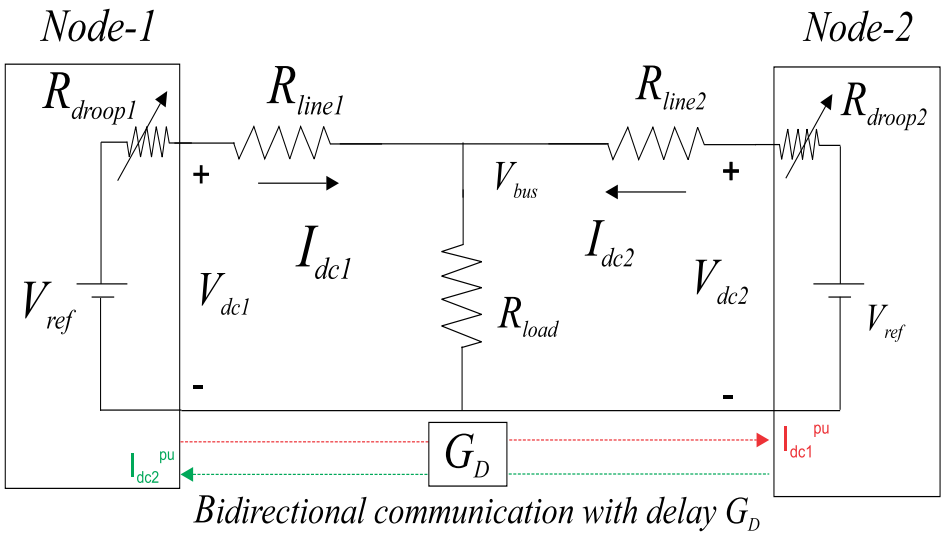

Figure 5.6 : A two node DC microgrid

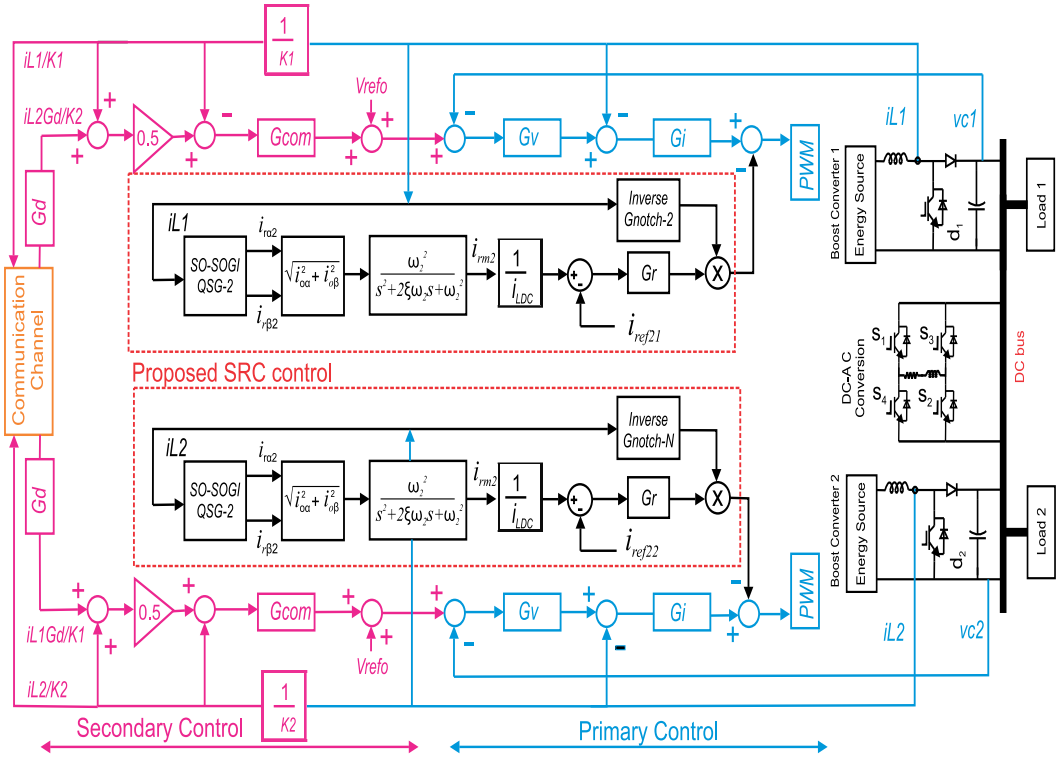

Figure 5.7 : Proposed SRC control with Primary and Secondary control

w_v must be less than w_c by almost ten times, i.e. $w_v < \frac{w_c}{10}$. The phase margin is kept at 60^o at ω_v. As an example for ΔV= 5V, and V_{in}= 40V, V_o= 120V, d= 0.666 the permissible duty cycle variation Δd is 0.0133. By using parameter values given in Table 7.1, the limits of gain values obtained will be $K_{pr} > 1.4601 \times 10^{-3}$ and $K_{ir} < 1.982$. Also the integrator time constant of ripple controller $(K_{pr}/K_{ir}$ of G_r must be between the voltage controller time constant $(K_p/K_i$ = 24.9 ms of $G_v)$ and current controller time constant $(K_p/K_i$ = 0.146 ms of $G_i)$. The values of K_{pr} and K_{ir} is taken to be 0.005 and

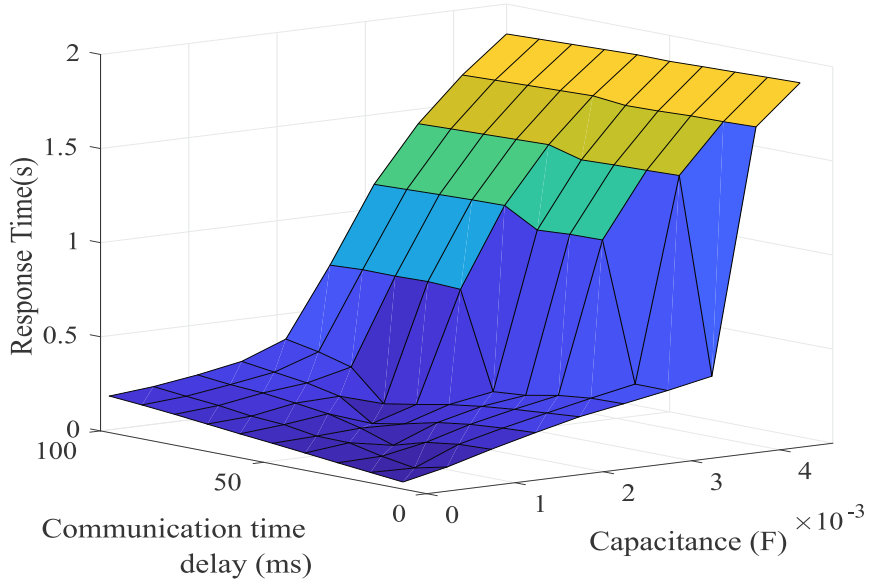

Figure 5.8 : Response time- variation in τ, C

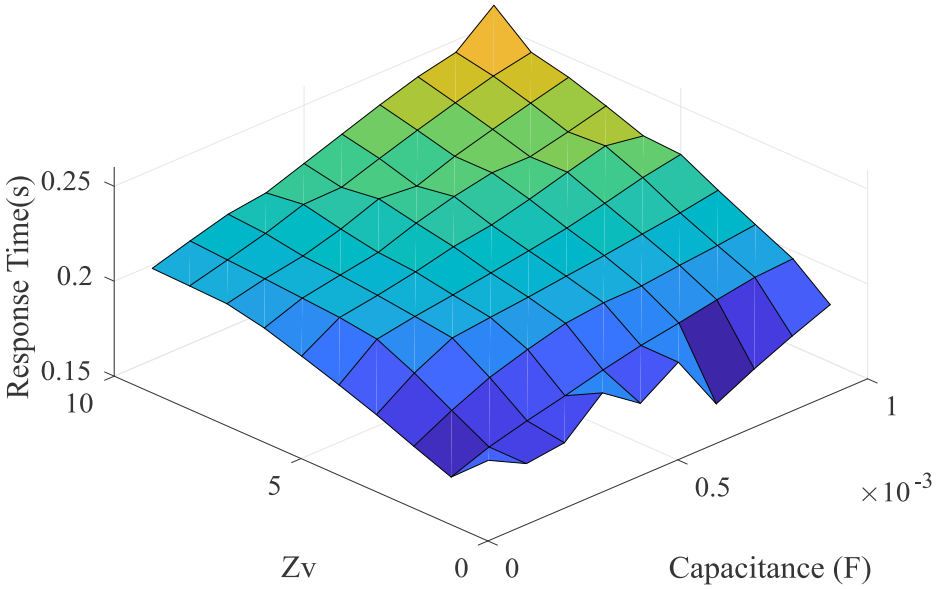

Figure 5.9 : Response time- variation in Z_v, C

0.9 respectively.

5.4 STABILITY ANALYSIS WITH PROPOSED CONTROL

An equivalent circuit of a two node DC microgrid, shown in Fig.5.6, is used to analyze the stability. The current from individual sources is derived as:

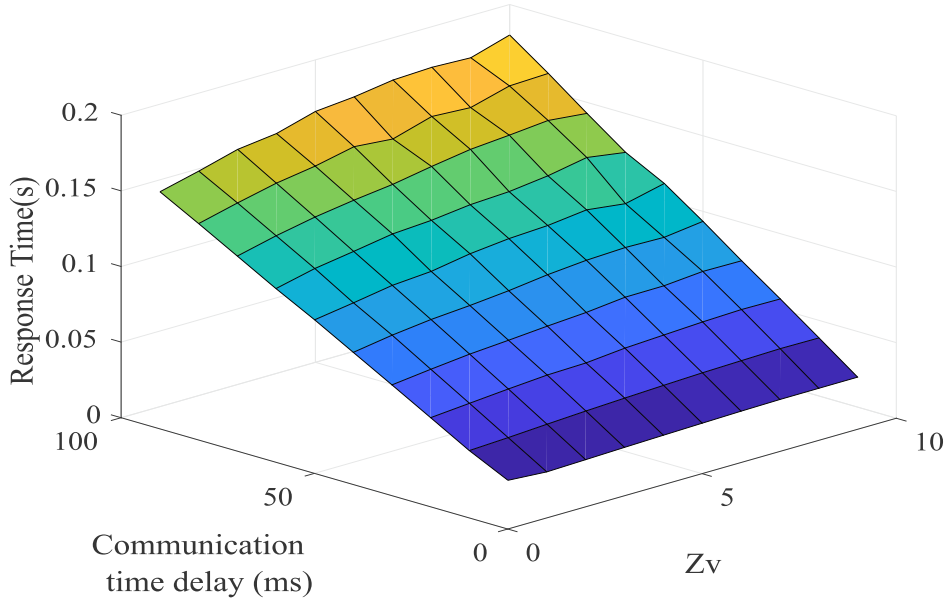

Figure 5.10 : Response time- variation in τ, Z_v

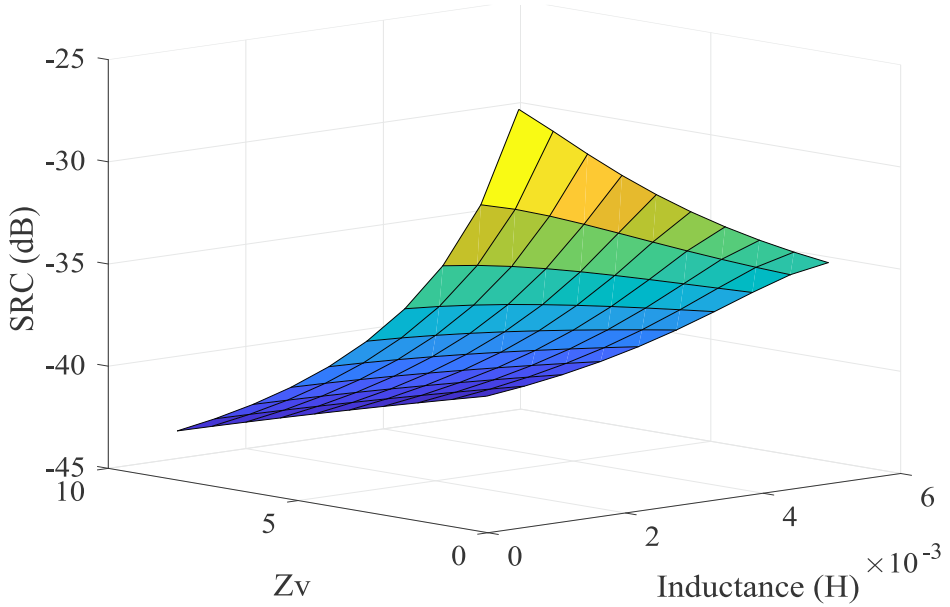

Figure 5.11 : SRC with variation in L, Z_v

$$I_{dc1} = \alpha_1 V_{dc1} + \beta V_{dc2}, I_{dc2} = \alpha_2 V_{dc2} + \beta V_{dc1} \tag{5.12}$$

$$\alpha_1 = \frac{R_{load} + R_{line2}}{R_{load}R_{line1} + R_{load}R_{line2} + R_{line1}R_{line2}}$$

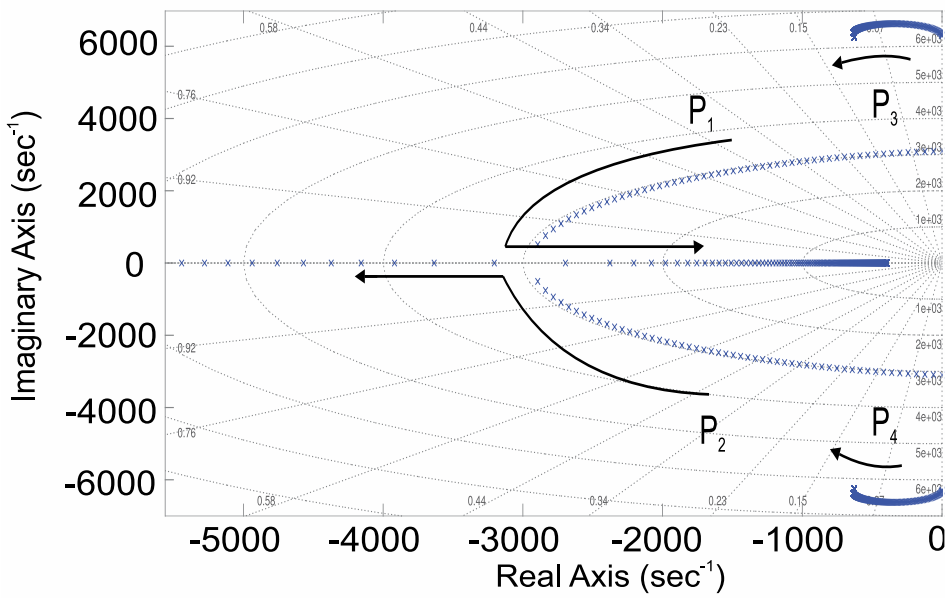

Figure 5.12 : Root locus of $\hat{v}_{io}/\hat{v}_{refo}$ with Z_v

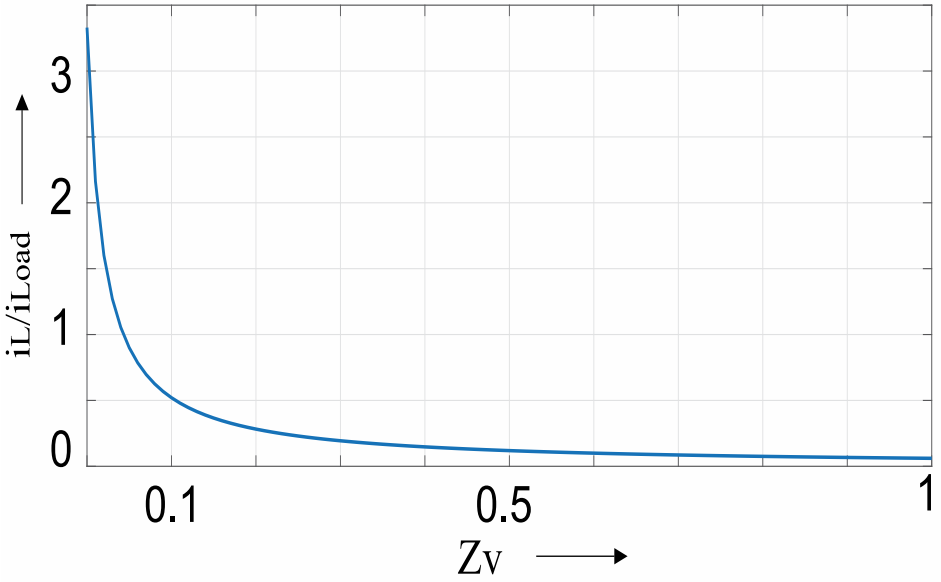

Figure 5.13 : Variation of $\hat{i}_L/\hat{i}_{Load}$ with Z_v at $2f_{ac}$

$$\alpha_2 = \frac{R_{load} + R_{line1}}{R_{load}R_{line1} + R_{load}R_{line2} + R_{line1}R_{line2}} \tag{5.13}$$

$$\beta = \frac{R_{load}}{R_{load}R_{line1} + R_{load}R_{line2} + R_{line1}R_{line2}}$$

In terms of current proportions k_1 and k_2, proportional sharing can be written as $\frac{I_{dc1}}{k1} = \frac{I_{dc2}}{k2}$ as in Lu *et al.* [2014]. The dynamic response is analyzed by deriving the transfer function of output voltage of i^{th} converter to its voltage reference, i.e., $\hat{v}_{io}/\hat{v}_{iref}$. The voltage reference v_{refo} is the DC bus voltage reference, common for all converters in the DC microgrid. The distributed secondary

control increases or decreases this voltage reference within desired voltage regulation limit to achieve proportional load sharing. The voltage reference, hence obtained for i^{th} converter, is v_{iref}. The function G_D is communication delay, $G_{com}(s)$ is PI controller for secondary control. The voltage reference of secondary control is estimated as:

$$v_{refi} = v_{refo} + (I_i^{pu} - I_j^{pu} G_D) G_{com} \tag{5.14}$$

where, v_{refo} is DC bus reference, v_{refi} is voltage reference of i^{th} converter, I_i^{pu} is per-unit loading of i^{th} converter and I_j^{pu} is per-unit loading of j^{th} converter. The transfer function $\hat{v}_{io}/\hat{v}_{refo}$ will be derived using $\hat{v}_{iref}/\hat{v}_{refo}$.

$$\frac{\hat{v}_{1ref}(s)}{\hat{v}_{refo}(s)} = \frac{1 + \frac{G_{com}}{2A_1}(\frac{\beta}{k1} + \frac{\alpha_2 G_D}{k_2})}{1 - \frac{G_{com}}{2}(\frac{\alpha_1 - \frac{G_{com}\beta B_1}{A_1}}{k_1} + \frac{G_D(\beta - \frac{\alpha_2 G_{com} B_1}{A1}}{k_2})} \tag{5.15}$$

$$\frac{\hat{v}_{2ref}(s)}{\hat{v}_{refo}(s)} = \frac{1 + \frac{G_{com}}{2A_2}(\frac{\beta}{k2} + \frac{\alpha_2 G_D}{k_1})}{1 - \frac{G_{com}}{2}(\frac{\alpha_2 - \frac{G_{com}\beta B_2}{A_2}}{k_2} + \frac{G_D(\beta - \frac{\alpha_1 G_{com} B_2}{A_2}}{k_1})} \tag{5.16}$$

where,

$$A_1 = G_{com}(\frac{\alpha_2}{2k_2} + \frac{\beta G_D}{2k_1}) - 1, B_1 = \frac{\beta}{2k_2} + \frac{\alpha_1 G_D}{2k_1}$$

$$A_2 = G_{com}(\frac{\alpha_1}{2k_1} + \frac{\beta G_D}{2k_2}) - 1, B_2 = \frac{\beta}{2k_1} + \frac{\alpha_2 G_D}{2k_2}$$

From Fig.5.7, the loop gain T_{LG} can be derived as,

$$T_{LG}(s) = \frac{\hat{v}_{1o}(s)}{\hat{v}_{1ref}(s)} = \frac{G_v G_i V_o / Kp}{\frac{sC}{(1-D)}\frac{sLG_N + Z_v}{G_N} + (1-D) + \frac{H_2 G_v G_i V_o}{K_P}} \tag{5.17}$$

Hence, the transfer function from of output voltage to reference voltage is $\frac{\hat{v}_{1o}(s)}{\hat{v}_{refo}(s)} = \frac{\hat{v}_{1ref}(s)}{\hat{v}_{refo}(s)} T_{LG}(s)$ can be simplified to obtain (5.19). When there are n nodes in the microgrid, there will be α_1,.. α_n parameters. Once all α_n are derived, the parameters A_n and B_n can be derived. These values can be substituted and rearranged to obtain $\frac{\hat{v}_{nref}(s)}{\hat{v}_{refo}(s)}$ which when multiplied by T_{LG} for n^{th} node, results in the transfer function which represents the microgrid dynamics. The relation between the DC bus voltage dynamics, DC bus capacitance, communication time delays, virtual Z_v, and interfacing converter inductance can be analyzed using (5.19.

Effect of DC bus capacitance

To reduce the SRCs, the DC bus capacitance needs to be increased as per passive methodologies. However, this results in degrading of dynamics as the bus voltage requires a longer time to settle as shown in Fig. 5.8.

Effect of Communication time delay

The communication delay between the nodes leads to an increase in the response time as shown in Fig. 5.8 and Fig. 5.10. Hence, communication delays degrades the performance of the microgrid.

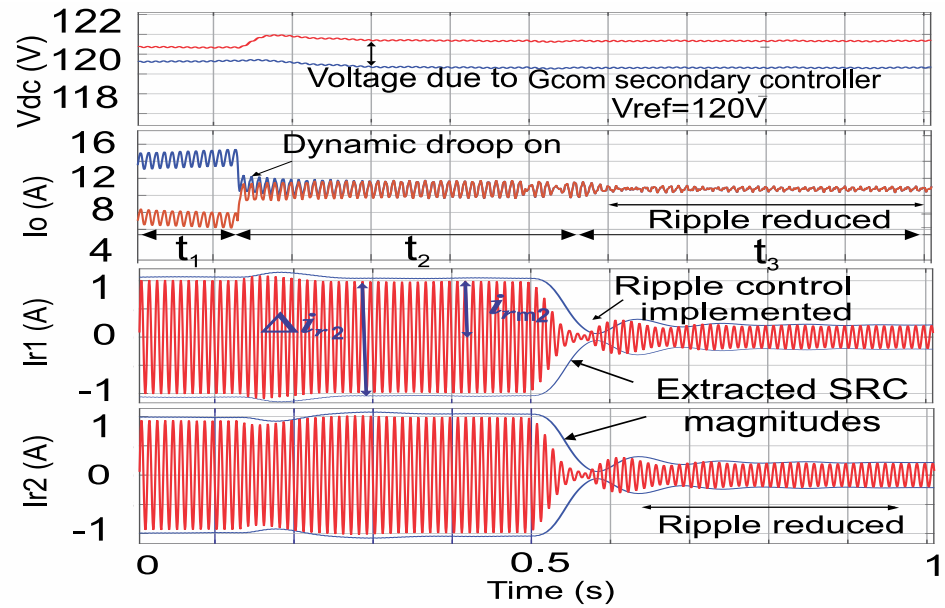

Figure 5.14 : Equal DC load sharing and SRC control

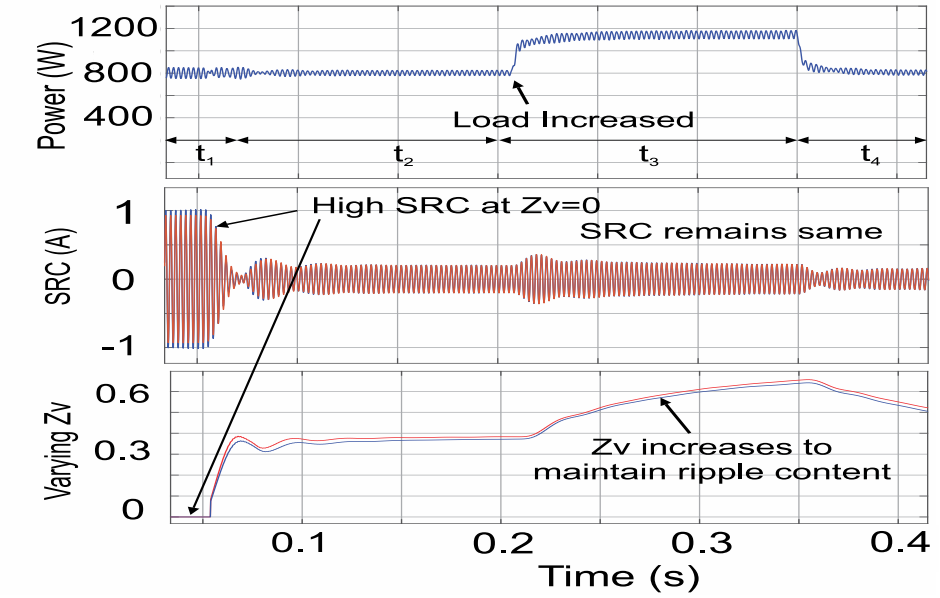

Figure 5.15 : Variation of Zv with load changes

Effect of virtual Z_v

The effect of Z_v variation with DC bus capacitance on response time is shown in Fig. 5.9. It can be observed that the response time for increase of Z_v is lesser than corresponding increase in capacitance. Similarly, Z_v does not effects the response time in presence of communication delays, as shown in Fig. 5.10. Finally, the SRC magnitude is reduced more by increasing Z_v instead of increasing the inductance of interfacing converters, as shown in Fig. 5.11.

Hence, the SRC can be mitigated using the proposed virtual SRC control by regulating

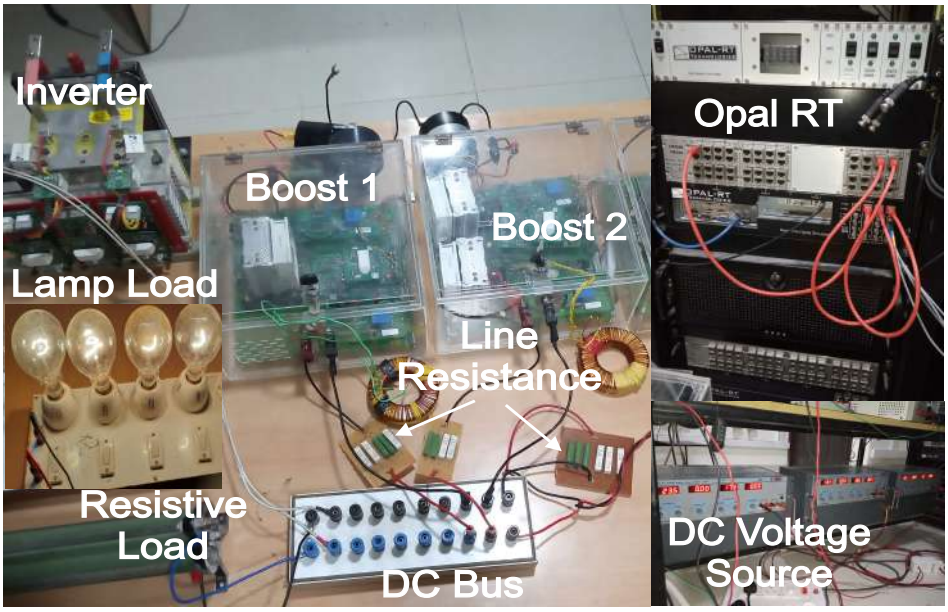

Figure 5.16 : Experimental setup

Z_v, instead of increasing DC bus capacitance, or interfacing converter inductance, in presence of communication delays. The closed loop dominant poles P1, P2, P3 and P4 for different values of Z_v is shown in Fig. 5.12. The poles of system move towards the left half plane however, P1 towards right half plane, as the value of Z_v increases. Hence, the value of Z_v must be limited within limits defined in previous section to maintain stability. Further, the transfer function of inductor current to load current is derived as:

$$\frac{\hat{i}_L(s)}{\hat{i}_{Load}(s)} = \frac{V_o G_v G_i / K_p}{s^2 LC + sCZ_v/G_N + (1-D)V_o G_v G_i / K_p} \tag{5.18}$$

The variation of inductor current to load current with varying virtual impedance Z_v is shown in Fig. 5.13. It can be observed that the magnitude of inductor current to load current at $2f_{ac}$ reduces with the increase of virtual impedance. The proposed DVI control is robust as the value of virtual impedance parameter Z_v varies depending on the SRC content and SRC reference at a node. The impedance is increased or decreased at a particular frequency irrespective of other parameters.

5.5 SIMULATION

A two node DC microgrid with AC and DC load is simulated in Matlab Simulink. The converters are connected to a common DC bus through a resistive line. The all to all per unit load

$$\frac{\hat{v}_{1o}(s)}{\hat{v}_{refo}(s)} = \frac{G_v G_i V_o / Kp}{\frac{sC}{(1-D)}\frac{sLG_N+Z_v}{G_N} + (1-D) + \frac{H_2 G_v G_i V_o}{K_P}} \cdot \frac{1 + \frac{G_{com}}{2A_1}\left(\frac{\beta}{k1} + \frac{\alpha_2 G_D}{k_2}\right)}{1 - \frac{G_{com}}{2}\left(\frac{\alpha_1 - \frac{G_{com}\beta B_1}{A_1}}{k_1} + \frac{G_D(\beta - \frac{\alpha_2 G_{com} B_1}{A1})}{k_2}\right)} \tag{5.19}$$

Table 5.1 : Simulation and Experiment Parameters

Symbol	Quantity	Values
V_{in}	Input source voltage	40 V, 40 V
V_{refo}, V_o	DC bus reference, and DC bus voltage	120 V
L_i	Inductor Values	2mH, 1.8mH
C_i	Terminal Capacitance	100 μF each
R_{Line1}, R_{Line1}, R	Connectine line resistances, load resistance	1.5 Ω, 2 Ω, 75-150Ω
$G_v(s), G_i(s)$	Local voltage and current controller	$3.74 + \frac{150}{s}$, $0.365 + \frac{2500}{s}$
$G_{com}(s)$	PI controller for secondary control	$1 + \frac{10}{s}$
G_d	Delay in communication	100 ms
H_1, H_2	Current sensor, voltage sensor gain	$1/2, 1/110$
w_n, w, ζ, K_1, K_2	SOGI QSG parameters	$2\pi 100, 77.8, 0.707, 0.175, 0.35$
AC load	Load Impedance	8x200 W bulbs

data exchange routine is implemented among the converters. The load is not shared equally during time interval t_1, as shown in Fig. 5.14. The secondary control is activated at the end of t_1. The load current is shared equally between the nodes. Due to inverter load, the SRC is 1 A at both nodes. The SRC is shown in red and its magnitude is shown in the blue waveform. The SRC magnitude $\triangle i_{r2}$ and i_{rm2} are extracted and fed in the control loop in Fig. 5.2. The impedance at both nodes is increased by making the SRC reference to 0.2 A. The SRC reduction can be seen during t_3. Hence, during t_3, the load is equally shared and ripple is reduced to a required level. The proposed control can completely eliminate SRC propagation to the source. This can be achieved by reducing the ripple reference at both the nodes. This will require an active filter to absorb the ripple content in the DC bus. The reduction in SRC must be maintained during load changes. This can be seen from Fig.5.15. The SRC control is activated at starting of t_2. During t_2, the virtual impedance Z_v remains constant, due to constant AC load. The load is increased from 800 W to 1200 W. To maintain the ripple content, Z_v increases as can be seen during t_3 in Fig. 5.15. The ripple controller reduces the value of Z_v during interval t_4 when the AC load is reduced back to 800 W. Hence, a dynamic output impedance for the converter is achieved.

5.6 EXPERIMENTAL VALIDATION

A DC microgrid prototype of two boost converters connected in parallel is implemented to verify the proposed control strategy, as shown in Fig. 5.16. The Opal-RT was used for real time control implementation. The current and voltage sensors used are ACS 709T and Lem 25-P respectively. The IGBT module FGH40N120ANTU is used as switch in boost converters, and

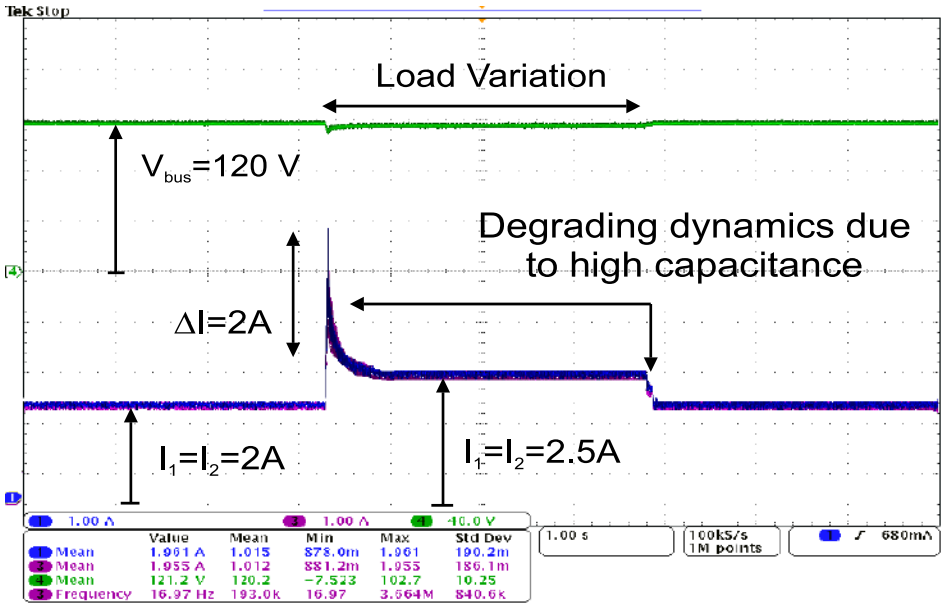

Figure 5.17 : Source currents- C_{bus} 1.36mF

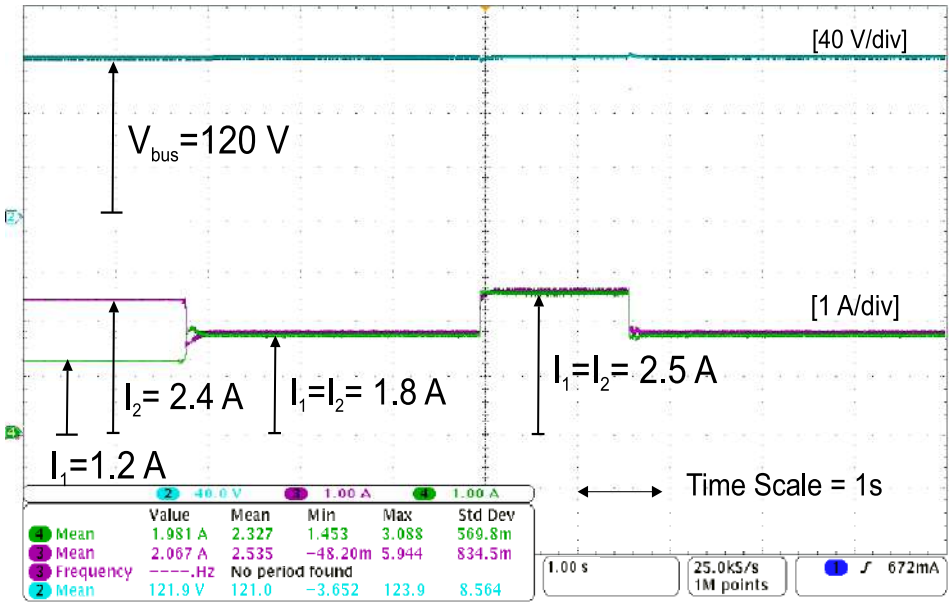

Figure 5.18 : Equal DC load sharing

SKM75GB128D are in inverter legs which feeds AC load. A controlled DC source is of 60V, 10A is used as a source. The communication routine between nodes is implemented in Matlab.

5.6.1 Equal DC load sharing

The per unit load current value is shared between the neighbors. This value is compared with current of the local converter and the error is passed to a PI controller G_{com}. To reduce SRC passively a DC bus capacitor $C_{bus} > 1/(4\pi f_{ac} L)$ must be used. The current waveforms with DC

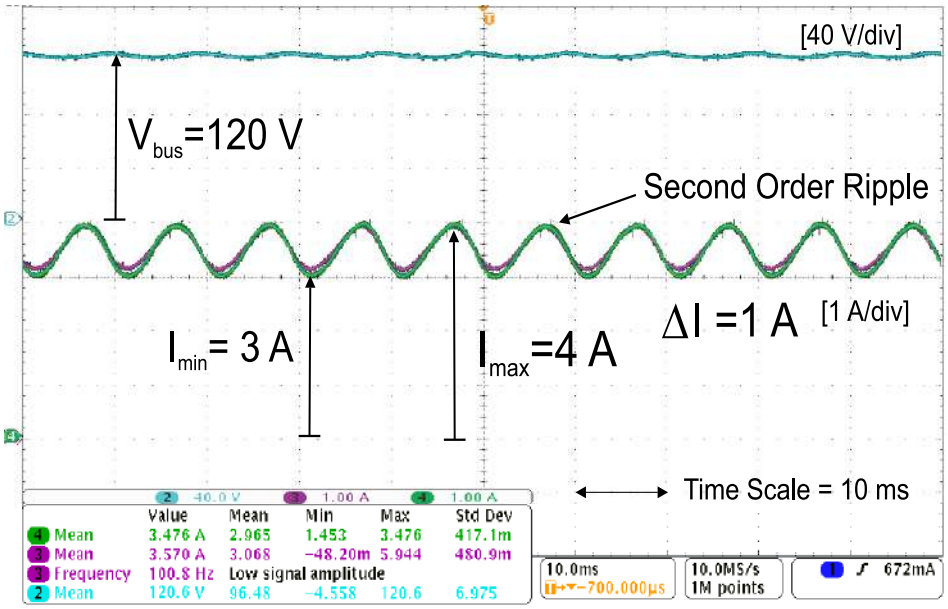

Figure 5.19 : SRC with inverter load turned on

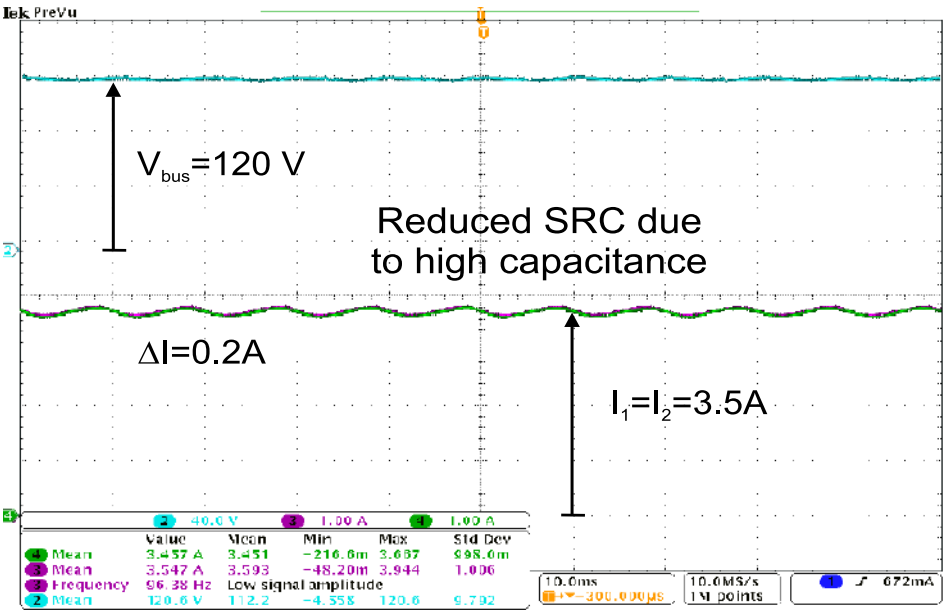

Figure 5.20 : SRC mitigation- C_{bus} 1.36mF

bus capacitance C_{bus} of 1.36mF is shown in Fig. 5.17, and with 100 μF is shown in Fig.5.18. The DC load is changed from 200 W to 300 W and back to 200 W. The load is equally shared among sources. It can be observed that the higher value capacitor degrades the dynamics as the source current may exceed the rated value. A comparison of Fig. 5.17 and Fig.5.18 shows that the current overshoots has been reduced when the proposed control is implemented and the proportional sharing is maintained.

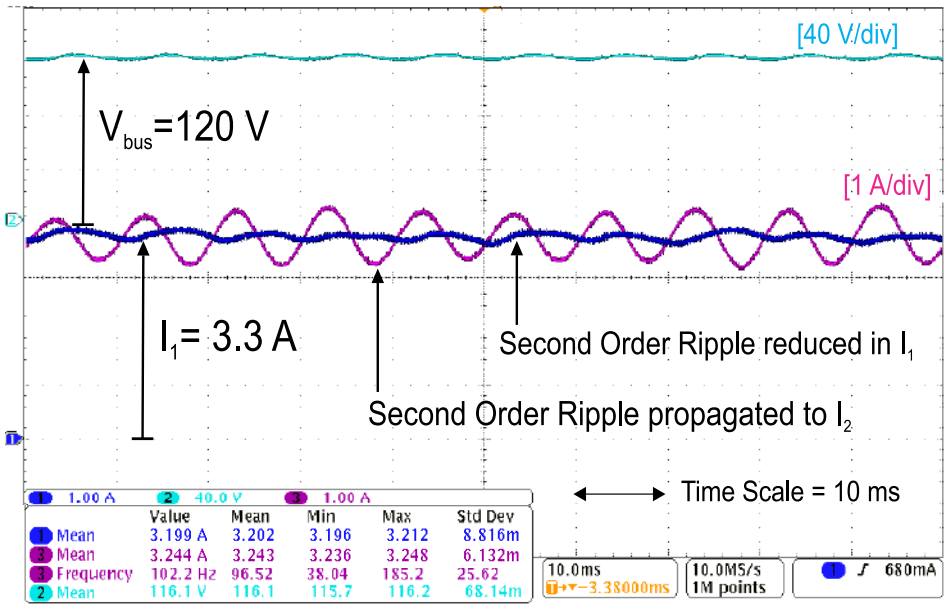

Figure 5.21 : SRC reduced at one node

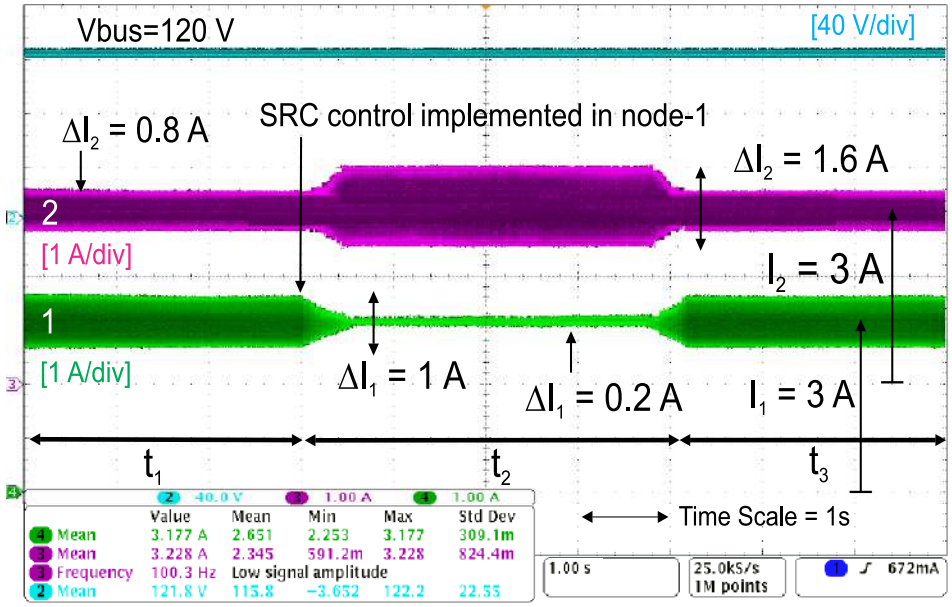

Figure 5.22 : SRC sharing between two nodes

5.6.2 SRC mitigation with AC and DC load variation

Now, that the DC load is shared equally, the AC load is also shared equally when turned on, as shown in Fig. 5.19. The DC load is 100 W and AC load is 300 W. The second order fluctuations in DC bus voltage and currents can be observed. However, the ripple in current is more (30% approx.) than in the voltage (<2%). The SRC can be reduced by using a 1.36mF DC bus capacitor, as shown in Fig. 5.20, however, it will degrade the dynamics, instead the proposed method can be used to reduce the SRCs. To obtain ripple sharing, the ripple reference in node-1 is set to 0.2 A and node-2 is set to 1.6 A. The SRC reduction at node-1 and increase in node-2 can be seen in

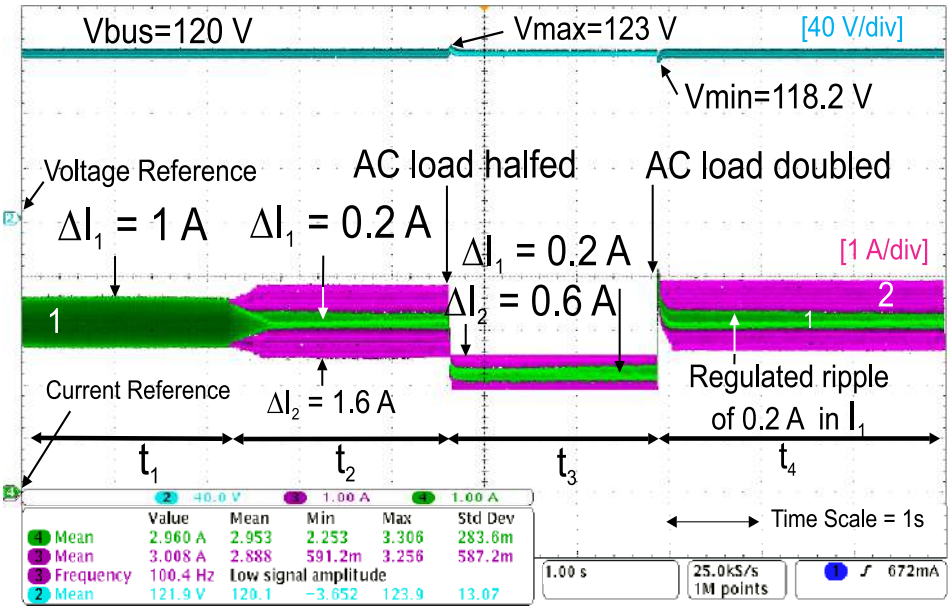

Figure 5.23 : Constant SRC with varying AC

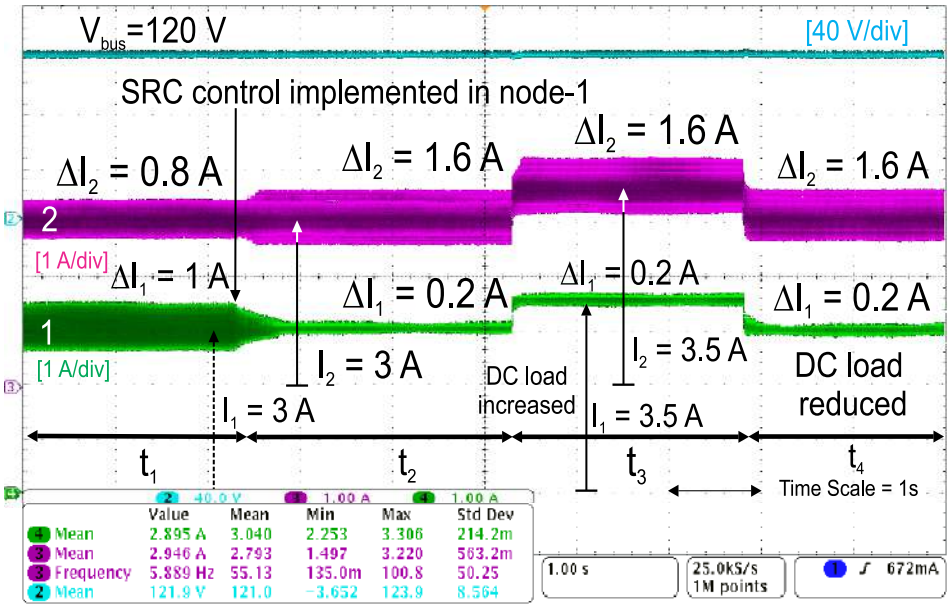

Figure 5.24 : Constant SRC with varying DC

Fig. 5.21 and Fig.5.22. The ripple control is implemented after the time interval t_1 as shown in Fig. 5.23. The ripple reference at node-1 is set to 0.2 A. The AC load is changed from 280 W to 140 W and back to 280 W while keeping DC load fixed at 100 W. It can be seen that the ripple remains constant when the AC load is varied. Further, comparison of Fig. 5.20 and Fig.5.25 shows that the SRC is reduced while sharing can also be achieved by using the proposed control instead of using a high DC bus capacitor. The ripple control is implemented during the time interval t_2, as shown in Fig.5.24. The load is varied from 150 Ω to 75 Ω and then back to 150 Ω while keeping AC load constant at 300 W. The ripple content remains 0.2 A irrespective of DC load changes as

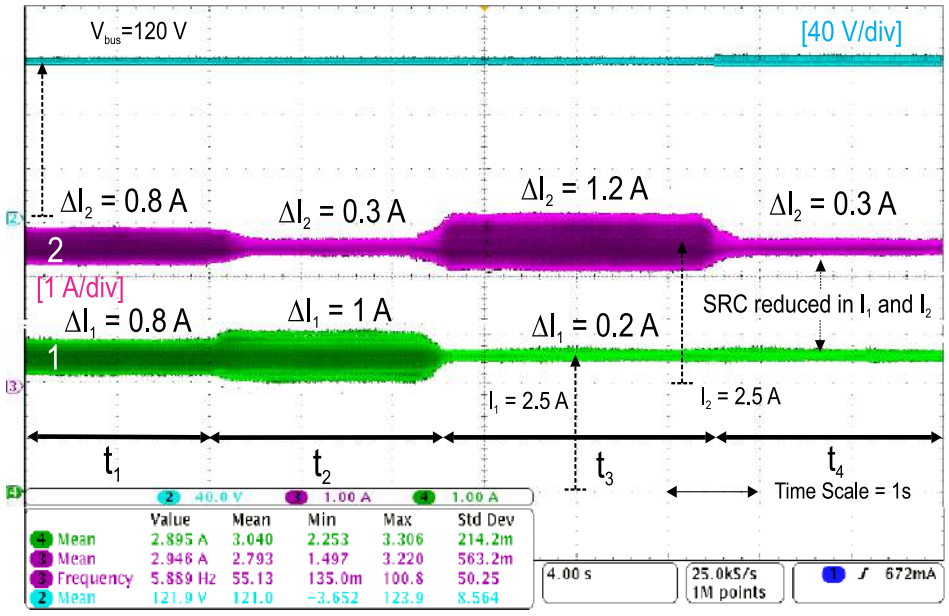

Figure 5.25 : Ripple sharing and mitigation

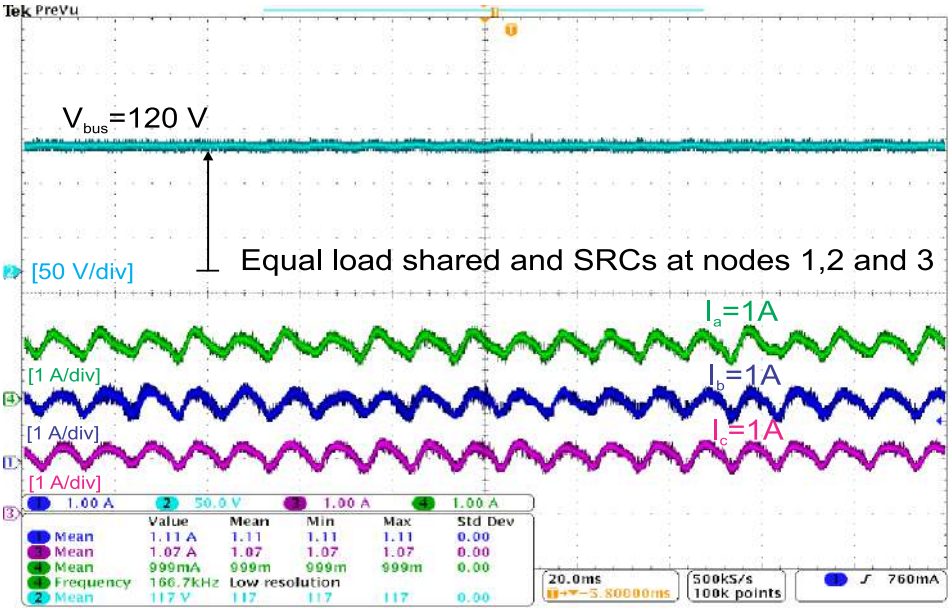

Figure 5.26 : SRC in a three node microgrid

shown in Fig.5.24. The SRC sharing is achieved by reducing the ripple current reference at both nodes. In Fig. 5.25, during t_1 both nodes share equal SRC. During time interval t_2 SRC reference of node-2 in set to 0.3 A. The SRC can be seen to propagate to node-1. Now, reference of node-1 is set to 0.2 A and reference of node-2 is increased to 1.2 A to achieve sharing. The reference is set to 0.2 A and 0.3 A respectively to reduce SRC at both nodes. The proposed control has been verified for a three node microgrid, such that the second and third converters are identical. The AC loads cause second order oscillations in source currents of all three nodes. The SRCs can be observed in Fig.5.26. To verify the proposed control, the DVI control is implemented and the SRC

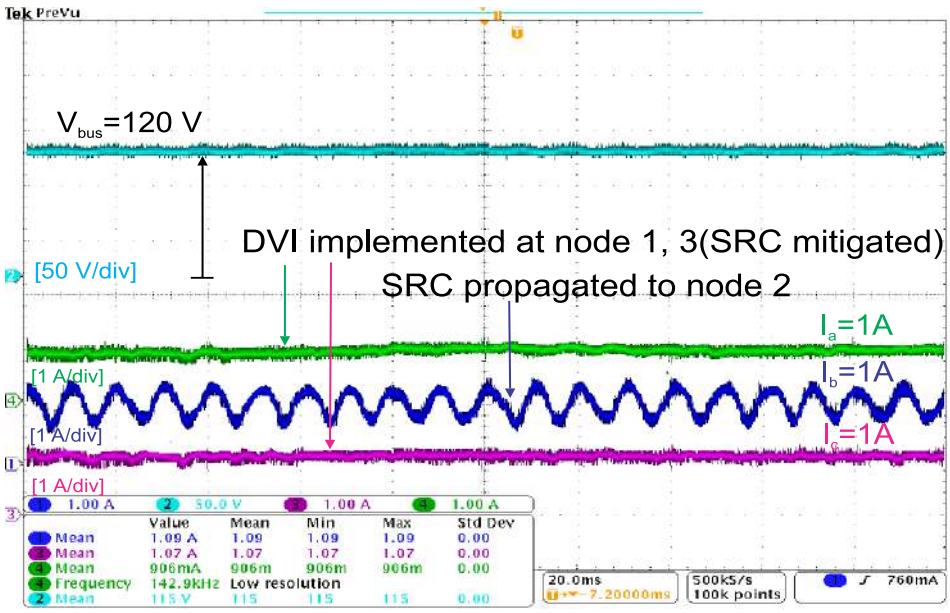

Figure 5.27 : SRC mitigation at nodes 1 and 3

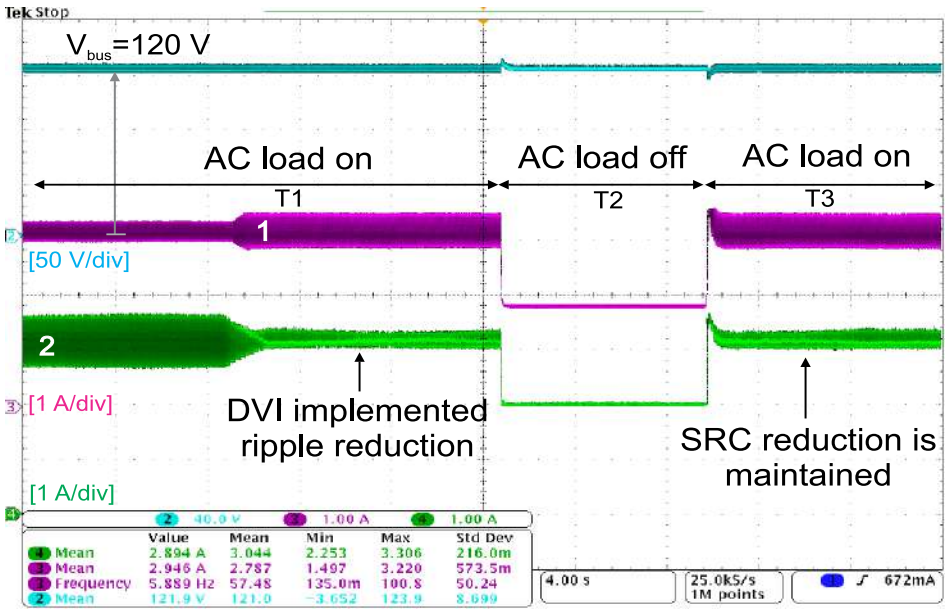

Figure 5.28 : With AC loads turned- on and off

reference is set to zero. As a result, the SRCs at node-1 and 3 gets eliminated as can be observed from Fig.5.27. Furthermore, the SRC reference for node-2 is increased so as to avoid DC bus second order oscillations. When the ripple is prevented from entering both the nodes, there is second order oscillations in the DC bus voltage. This can be mitigating by installing an active filter on the DC bus. Using an active filter eliminates the need of a higher value capacitance. It must be ensured that the SRCs must be less than 8% of the rated current. The proposed DVI should share the DC load proportionally in absence of AC load, during the impedance regulation mode. This is verified experimentally in a two node microgrid, as shown in Fig.5.28. The AC load is turned on till time

interval T_1, and the proposed SRC reduction is implemented at node 2. All AC loads are turned off at the end of T_1. It can be observed that the load gets reduced and SRCs become zero. Only DC load is fed during the time interval T_2. The AC load is again turned on at the end of T_2. The SRC regulation is maintained. Hence, the SRC mitigation is restored once the AC load is turned on. The proposed control is verified for AC load turned- on and off. A comparison of parameters is shown in Table 7.2. In Case-1, it is shown that the output impedance is increased from 2.1dB to 22dB so as to have the overall impedance greater than the capacitance branch. In Case-2, the inductor L is to be increased to 22 mH with capacitance C of 100 mF to reduce the SRCs. While on implementation of proposed DVI, the L of 2mH will be able to mitigate the SRCs. Similarly, the SRCs can be mitigated by increasing the C to 1.26mF. By using the proposed control, the SRCs can be significantly reduced by using only 100 mF capacitor. Hence, considerable reduction in passive component size is achieved by using the proposed DVI. In literature, authors in Hamzeh *et al.* [2015] and Jia *et al.* [2017a] have proposed oscillatory current sharing methodology, however, the virtual impedance does not changes with load variation and are not integrated with secondary control. The proposed DVI control, regulates the output impedance with integrated secondary control for microgrid application.

5.7 CONCLUSION

The paper has proposed a solution to regulate the SRC propagating to a node by controlling the output impedance. The proposed DVI control regulates the output impedance magnitude at $2f_{ac}$, depending on the SRC reference of the node. The proposed control improves the response of the microgrid, while enabling SRC sharing among the sources. This helps in improving the energy density in SRC filters installed at a node. The proposed control facilitates easier maintenance of active filter circuit and also reduce the capacitance requirements at all the nodes. The method is applicable to the areas where AC side ripple suppression is not considered. The simulation and experimental results show that the SRC is always regulated to be within 8% limit, irrespective of AC or DC load variations. The DC bus voltage remains within the voltage regulation limit during AC and DC load variations. Hence, the objective of mitigation or sharing SRC is achieved along with the proportional DC component sharing among sources. The proposed control methodology has been validated through simulation and experimentation.

Table 5.2 : Comparison of components for SRC mitigation

Component	Without DVI	With DVI
1. Z_L, Z_c, Z_o at $2f_{ac}$	2dB, 23dB, 2.1dB	2dB, 23dB, 22dB
2. L to mitigate SRC	22mH	2mH
3. C to mitigate SRC	1.36mF	0.1 mF

The SRCs affect the voltage references generated by the secondary control. The oscillations in voltage references leads to oscillations in the DC bus voltage. Hence, any oscillation in the data communicated between the nodes must be mitigated. This low pass filters should not be preferred as they degrade the dynamics of the system. In next chapter a robust primary and secondary controller is presented. The primary control consists of a SMC and the secondary control is ISMC. This results in an improved proportional load sharing during plug-and-play operations. The modeling uncertainties and communication uncertainties are mitigated. The ISMC cancels out any oscillations and tunes the primary control to regulate the DC bus voltage within the desired

limits.