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AMC using Constellation Analysis with Oversampling Factor Alteration

7.1 INTRODUCTION

Automatic modulation classification finds its application in many military and civil areas. It is an integral part of cognitive radio and software-defined radio technologies. In this chapter, LabVIEW-based Field Programmable Gate Array (FPGA) implementation of the modulation classification algorithm is proposed. Any modulation scheme among BPSK, QPSK, 8PSK, 8QAM, 16QAM, and 4ASK is classified by alteration of oversampling factor and further error minimization between the extracted constellation and ideal constellation of considered modulation schemes. The developed method has also been implemented on FPGA. This classifier can be used in link adaptation which provides reliable and high throughput communication system. The present algorithm is also implemented on FPGA, which can be easily replicated for industrial production and can be further updated to add more modulation schemes and resource optimization. Study results reveal that the developed method detects the above-mentioned modulation schemes reliably above 12 dB SNR in the Additive White Gaussian Noise (AWGN) channel. Comparative analysis of the proposed method with existing methods based on higher-order statistics, Mel-frequency ceptral coefficients and naive-based modulation classification shows an overall improvement in classification accuracy.

7.2 SYSTEM AND SIGNAL MODEL

Modulated signals of all schemes considered are generated by NI-PXIe-5673 (RF transmitter) and transmitted through SMA cable. The signal is received by the NI-5791 Adapter Module, which is represented as

$$r_R(t) = \Re\{e^{j(2\pi f_c t + \Delta\phi)} s(t)\} \tag{7.1}$$

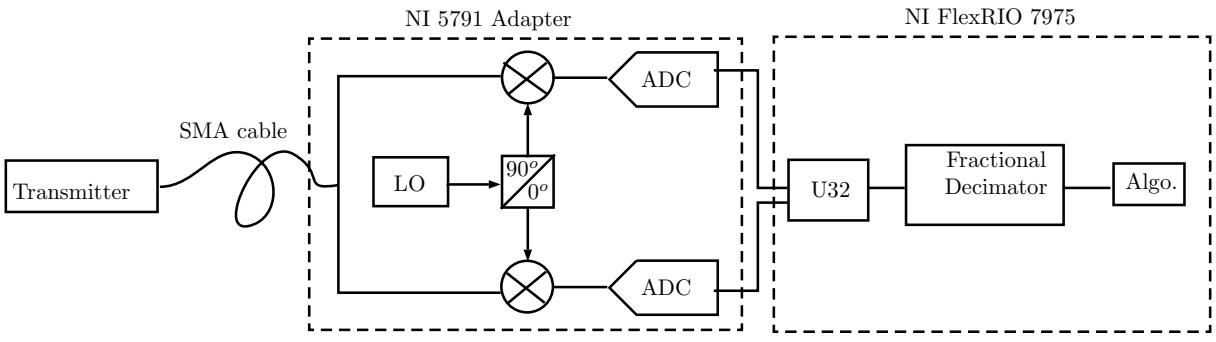

Figure 7.1 : System model

Where $s(t)$ is baseband complex envelop, f_c is carrier frequency and $\Delta\phi$ denotes phase offset. $r_R(t)$ is down-converted to baseband by mixing with the signal of frequency equal to f_c' (estimated carrier frequency). Signal with frequency f_c' is generated internally in Adapter Module or can be provided externally through the provided port. Down-converted signal is expressed as

$$r_d(t) = \Re\{e^{j(2\pi\Delta f_c t + \Delta\phi)} s(t)\} \tag{7.2}$$

Δf_c is carrier frequency offset (CFO), generated due to the difference between an actual and estimated carrier frequency $(f_c - f_c')$. Received Signal $r_d(t)$ is sampled with default sampling frequency 130M samples/second of adapter module. Sampled signal has in-phase and quadrature components, which have been given to NI-FlexRIO-7975 FPGA module for further processing. Down-converted and resampled signal $r_{ds}[nT_s]$ is given by

$$r_{ds}[nT_s] = \Re\{e^{j(2\pi n\Delta f_c T_S + \Delta\phi)} s[nT_s]\}$$

Here, T_s represents sampling time, and $r[n]$ is complex noisy baseband waveform, which can be denoted by

$$r[n] = s[n] + \eta[n] \tag{7.3}$$

Received samples of $r[n]$ are further resampled in the FPGA module using a fractional decimator as per the requirement of the algorithm. System model is shown in Figure 7.1.

$$s[n] = \sum_{k=0}^{K} a_k[n] p[n - kT - \Delta T] \tag{7.4}$$

Where $s[n]$ is pulse shaped complex baseband waveform, $p[n]$ is pulse shaping filter coefficients, T is symbol time and ΔT is symbol time offset. $s[n]$ contains $(K+1)$ equiprobable symbols from any candidate modulation scheme. {BPSK, QPSK, 8PSK, 8QAM, 16QAM and 4ASK} is the set of candidate modulation schemes. $\eta[n]$ is complex Additive White Gaussian Noise (AWGN) whose Probability Density Function (PDF) can be given as

$$\eta(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(x-\mu)^2}{2\sigma^2}} \tag{7.5}$$

μ, σ are the mean and standard deviation of the AWGN noise, respectively.

7.3 MODULATION CLASSIFICATION ALGORITHM

7.3.1 Preprocessing for constellation extraction

Proposed algorithm requires constellation for modulation scheme detection. In preprocessing step carrier frequency (f_c), carrier frequency offset (Δf_c) and symbol time offset (ΔT)

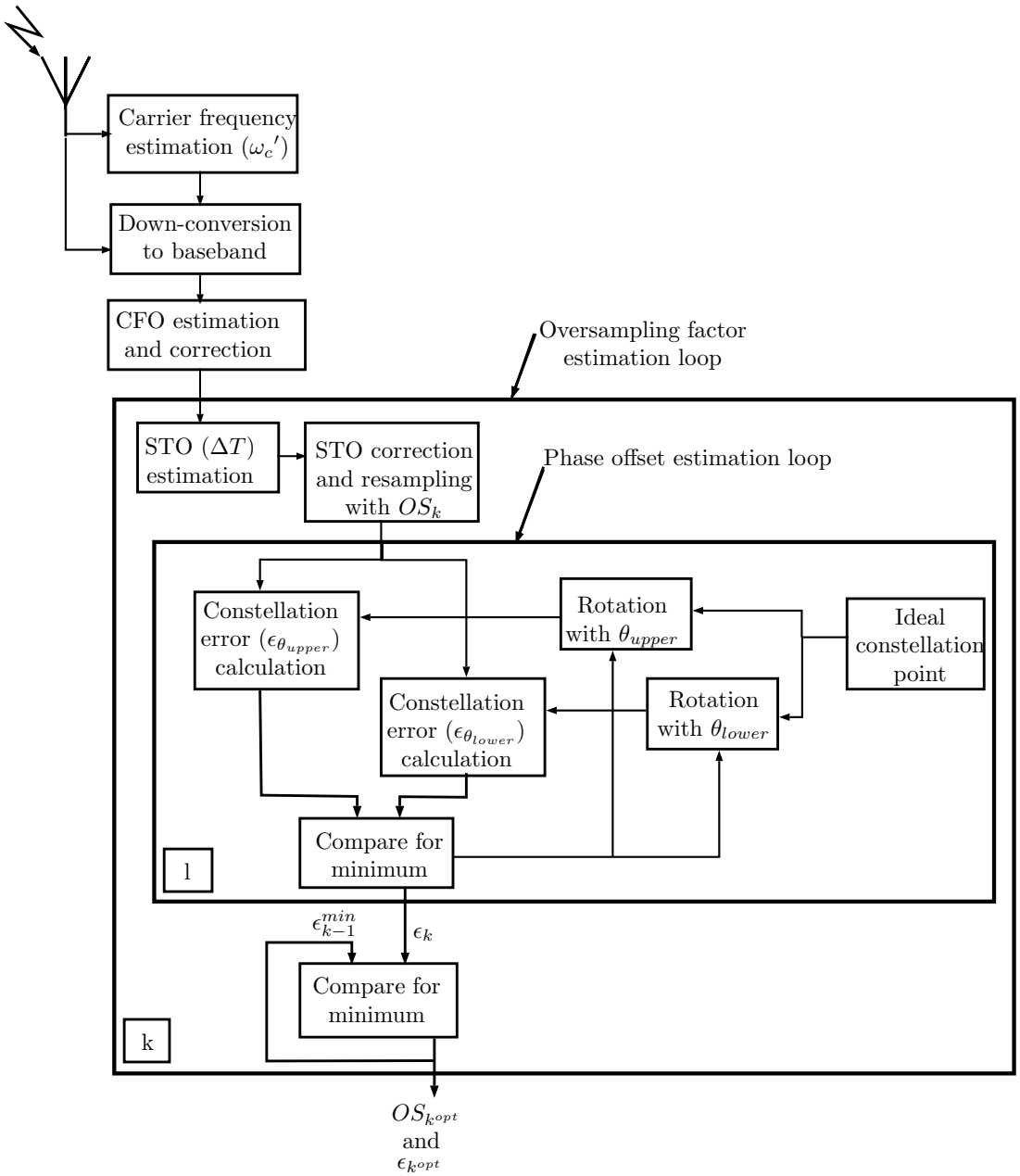

Figure 7.2 : Modulation classification approach.

are estimated, and Δf_c, ΔT are corrected for extraction of constellation points. Center frequency of 90% power spectrum band is calculated as estimated carrier frequency f_c' and RF received signal is down-converted with it. Downconverted signal with Δf_c CFO is denoted by

$$r_{ds}[n] = r_{dsI}[n] + jr_{dsQ}[n] \tag{7.6}$$

where $r_{dsI}[n]$ and $r_{dsQ}[n]$ are in-phase and quadrature component of down-converted and resampled received signal respectively, which is further used for Δf_c estimation by using [Sethi and Ray, 2013] as shown in Equation (7.7).

$$C[f] = |FFT(r_{ds}^{8}[n])| \tag{7.7}$$

N-point FFT has been taken of eighth power of $r_{ds}[n]$, where N is length of FFT. Peak is identified at index k, which corresponds to $8\Delta f_c$ and can be calculated using Equation (7.8).

$$8\Delta f_c = \frac{k f_s}{N} \tag{7.8}$$

Where f_s is sampling frequency.

Signal with frequency offset Δf_c gives a phase shift of $\Delta f_c T_s$ to each sample w.r.t. previous sample and forms circle. As algorithm is based on constellation, Δf_c needs to corrected for correct constellation formation. Frequency offset correction can be done by applying $-n\Delta f_c T_s$ phase shift to n^{th} sample of $r_{ds}[n]$, which can be mathematically expressed as given in Equation (7.9)

$$r'_{ds}[n] = r_{ds}[n] e^{-jn\Delta f_c T_s} \tag{7.9}$$

Where $r_{ds}[n]$ and $r'_{ds}[n]$ are the signals before and after carrier frequency offset correction respectively.

7.3.2 Modulation scheme detection

Oversampling Factor (OS): oversampling factor can be defined as samples per symbol or ratio of sampling frequency and symbol rate [Jajoo *et al.*, 2017].

Method is proposed for modulation identification based on the error minimization between constellation received for particular oversampling factor and ideal constellation among a considered set of modulation schemes. Block diagram of algorithm is shown in Figure 7.2. The algorithm is divided into three parts: resampling and constellation extraction, phase offset estimation, and modulation scheme detection.

Resampling and constellation extraction

Signal corrected for CFO is fed to the oversampling factor estimation loop for symbol time offset estimation and correction for particular oversampling factor. Signal is then down-sampled with oversampling factor OS_k as shown in Figure 7.2. For each OS_k, constellation is generated which is used further for phase offset and symbol rate estimation. If the signal is having f_s sampling frequency and range of oversampling factor considered is $(OS_{initial} - OS_{final})$, then symbol rate range will be $(\frac{f_s}{OS_{final}} - \frac{f_s}{OS_{initial}})$. For k^{th} iteration oversampling factor will be

$$OS_k = OS_{initial} + k\Delta p$$

Where Δp is the resolution of oversampling factor. Symbol rate estimation error (ζ_{SR}) depends on Δp. So, Δp is chosen such that the symbol rate is estimated accurately with lower computational complexity.

$$\zeta_{SR} \propto \frac{1}{\Delta p}$$

Phase offset estimation

Phase offset is estimated by rotating the ideal constellations of all the modulation schemes as explained in Algorithm 2. Step size and direction of rotation are made dependent on the error calculated in the previous iteration. Θ_{upper} and Θ_{lower} are initialized for all modulation schemes. $\varepsilon_{\Theta_{upper}}$ and $\varepsilon_{\Theta_{lower}}$ is error calculated between the received constellation and ideal constellation rotated with angle Θ_{upper} and Θ_{lower} respectively. Expression for error calculation is given in Equation (7.10). Either Θ_{upper} or Θ_{lower} is selected by comparing $\varepsilon_{\Theta_{upper}}$ and $\varepsilon_{\Theta_{lower}}$ for minimum. Selected angle ($\Theta_{selected}$) is updated by $(\Theta_{upper} - \Theta_{lower})/4$ to find Θ_{upper} and Θ_{lower} for next iteration. This process is repeated for 10 iterations and Θ_{upper} will be the optimum phase offset Θ^{opt}.

$\varepsilon_{\Theta^{opt}}$ is calculated for all modulation schemes using the expression given below

$$\varepsilon_{\theta} = \sum_{l=1}^{N_2} \min_{1 \le i \le M} \left(I_i e^{j\theta} - P_l\right)^2 \tag{7.10}$$

Where M is order of modulation, P_l is l^{th} received constellation point, I_i is i^{th} points of ideal constellation of order M and N_2 is number of symbol points received. This formula is used to find the summation of the square of Euclidean distance of all received points from the nearest ideal point rotated with θ angle. The final modulation scheme is identified by comparing $\varepsilon_{k^{opt}}$ for all modulation schemes.

Algorithm 2: Phase Offset Estimation

Calculate optimum phase offset (Θ^{opt}) using constellation error minimization.
Initialize Θ_{upper} and Θ_{lower}
while $l \le 10$ **do**
  if $\varepsilon_{\Theta_{upper}} \le \varepsilon_{\Theta_{lower}}$ **then**
    $\Theta_{selected} = \Theta_{upper}$
  else
    $\Theta_{selected} = \Theta_{lower}$
  end if
  $\Theta_{update} = (\Theta_{upper} - \Theta_{lower})/4$
  $\Theta_{upper} = \Theta_{selected} + \Theta_{update}$
  $\Theta_{lower} = \Theta_{selected} - \Theta_{update}$
end while
$\Theta^{opt} = \Theta_{upper}$

Symbol rate estimation

Symbol rate is defined by

$$R_s = \frac{f_s}{OS_{k^{opt}}}$$

$$OS_{k^{opt}} = OS_{initial} + k^{opt}\Delta p$$

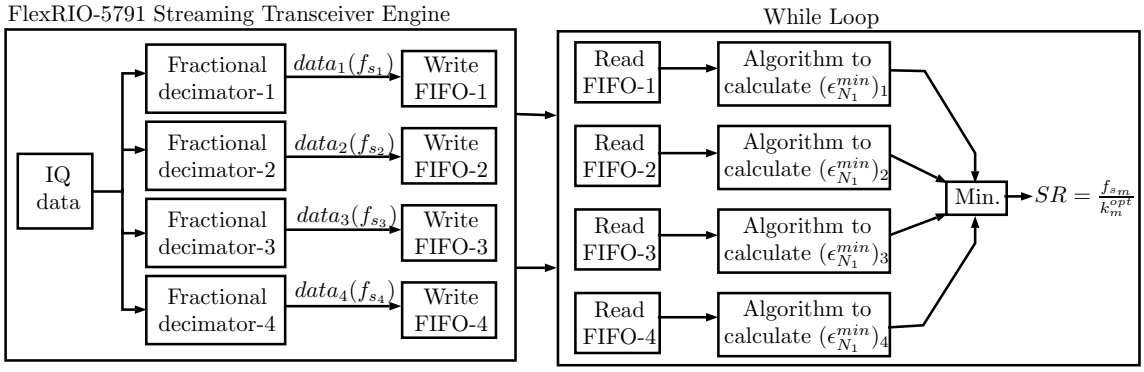

Figure 7.3 : Parallel processing of algorithm for four ranges of symbol rate.

Where k^{opt} is iteration number for which ε_k is minimum ($\varepsilon_{k^{opt}}$) and Δp is resolution of oversampling factor.

Δp is trade off between constellation error and computational complexity. Constellation error increases with Δp. Range of symbol rate, which can be estimation is defined by $(\frac{f_s}{OS_{final}} - \frac{f_s}{OS_{initial}})$.

7.4 FPGA IMPLEMENTATION OF ALGORITHM

7.4.1 LabVIEW FlexRIO communication architecture

The algorithm is implemented on LabVIEW FPGA and programs generated are called Virtual Instruments (*VIs*). Two *VIs* are used, i.e. *host VI* and *target VI* or *FPGA VI* to implement the method on LabVIEW FPGA. *Host VI* runs on windows and FPGA is programmed through a bit file generated according to *target VI*. Users can change the parameter through *host VI*. Both *VIs* interact with each other through front panel communication and First-In-First-Out (*FIFO*). To provide instruction or small data transfer between these two *VIs*, front panel communication is used and for large data transfer, *FIFO* is used. Direct Memory Access (DMA) *FIFO* is used for data communication between *FPGA VI* and *host VI*. *Target scoped FIFO* is another communication unit, which transfers data to and from *FPGA VIs* under the same target using the same *FIFO*. *Block Memory* is another FPGA element to store and access data within a target and memory is assigned to it at the time of code compilation. The advantage of *Block Memory* is that data of any address can be accessed from one or all *FPGA VIs* under the same target.

Compilation of LabVIEW *VIs* convert graphical code into VHDL code and hardware circuit realization is generated using Xilinx compiler. Bitfile is generated as a final result after compilation which contains information about how the gates should be connected.

7.4.2 Data Acquisition

Received RF signal at adapter NI 5791 is downconverted and sampled at 130M samples/seconds (default), from where inphase (*Rx_I*) and quadrature (*Rx_Q*) component of baseband waveform is received in *I*16 (16-bit integer) format. *Rx_I* and *Rx_Q* are converted in *U*32 (32-bit signed integer) format, which contains 16 bit of inphase data and another 16 bit of quadrature data. *U*32 data is now downsampled by four fractional decimators of sampling frequency f_{s_i}, where $1 \leq i \leq 4$ and four signals are generated $data_i$, where $1 \leq i \leq 4$ for four different range of symbol rate as shown in Figure 7.3. Downsampled data is transferred to while loop using

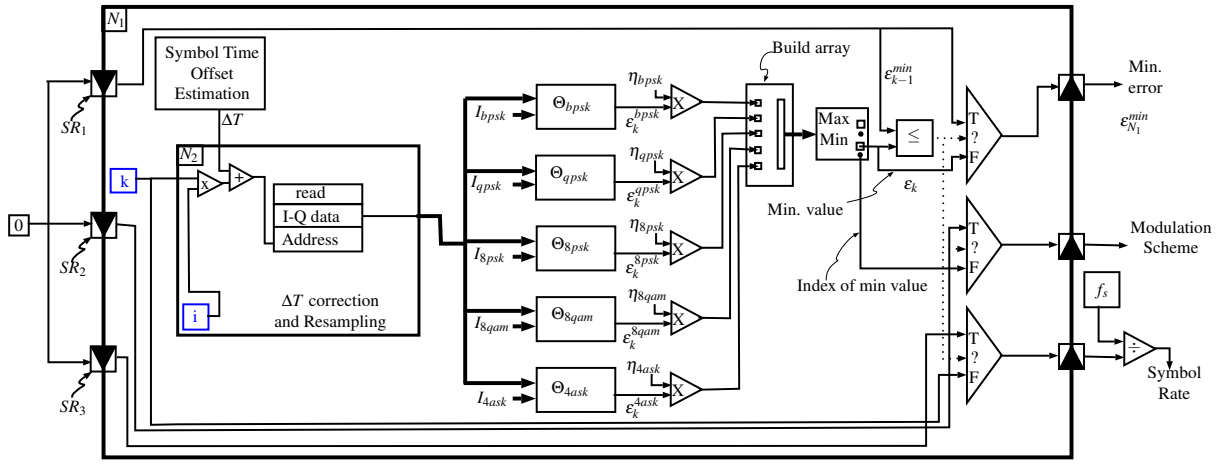

Figure 7.4 : FPGA implementation of modulation classification approach.

target scoped FIFOs (FIFO-*i*, where $1 \leq i \leq 4$), which is further written in block memories named $I-Q\ data_i$, where $1 \leq i \leq 4$ for processing of these four signals parallel to find $\varepsilon_{N_1}^{min}$. Calculation of $\varepsilon_{N_1}^{min}$ is described in Figure 7.4.

7.4.3 Modulation scheme detection and symbol rate estimation

Sampled data read from four block memories ($I-Q\ data_i$, where $1 \leq i \leq 4$) and fed to four parallel algorithm blocks to take the optimum decision by comparing errors. Each of the blocks contains an algorithm depicted in Figure 7.4. Parallel processing of the algorithm reduces the time required for classification. The objective of the algorithm is to find out oversampling factor for which the constellation extracted has a minimum error with anyone ideal constellation of modulation schemes considered. For four different ranges of symbol rate (5k-10k), (10k-15k), (15k-20k), and (20k-25k), range of oversampling (1000-2000), (1000-1500), (1500-2000), and (1600-2000) is considered respectively. 90000 ($N_2 * OS$ i.e 60*1500) sample points in block memory $I-Q\ data_2$ and 120000 (60*2000) sample points in $I-Q\ data_1$, $I-Q\ data_3$ and $I-Q\ data_4$ has been written for extraction of 60 symbol points in all four parallel algorithms.

CFO estimation and correction

CFO estimation is common to all four signals as each signal contains the same information with a different sampling frequency. Once CFO is estimated, CFO correction is done for all four parallel blocks before further processing. CFO is estimated with the method explained in section 7.3.1, considered length of FFT is 8192. In FPGA, the FFT block has $2m$ points latency for the signal length of m. 8192 is the maximum FFT length available in the FPGA being used. To get 8192 valid output points, 24576 points need to be given to the eighth order non-linearity, which is generated by using high throughput complex multiplication VI. Passing that output signal through the FFT block and the last 8192 points are considered to get the CFO. CFO is estimated by calculating frequency corresponding to the peak index of FFT output using Equation (7.8). N is 8192 and f_s depends on the selection of the signal from any four. Sampling frequencies considered

are 10M, 15M, 30M and 40M for f_{s_i}, where $1 \leq i \leq 4$ respectively. CFO correction has been done by using Equation (7.9) to all four signals r_{ds_i}, where $1 \leq i \leq 4$ with their respective sampling frequency. Then, CFO corrected signals are given to the algorithm to find out the optimum oversampling factor in their symbol rate range.

Symbol time offset estimation and correction

For each oversampling factor (say m), it is known that each symbol of the sampled signal contains m samples. i^{th} sample of each symbol is added to the corresponding sample of contiguous symbols till the last sample. It will give an array of m values. The index corresponding to maximum value gives an estimate of symbol time offset, as average energy is maximum at that symbol sampling instants. This offset is removed from the signal and all samples corresponding to constellation signature are acquired as shown in Figure 7.4. Outer *For Loop* in Figure 7.4 is running for number of oversampling factors (N_1) and inner *For Loop* is running for N_2=60, i.e., number of symbols.

Phase offset, symbol rate, and modulation scheme detection

Phase offset is estimated by using Algorithm 1. Initial Θ_{upper} and Θ_{lower} considered for BPSK are $(135°, 45°)$, for QPSK $(22.5°, -22.5°)$, for 8PSK $(11.25°, -11.25°)$, for 8QAM $(22.5°, -22.5°)$ and for 16QAM $(22.5°, -22.5°)$. The array of length 10 is taken with these values, which are updated as the algorithm iterates. As shown in Figure 7.4, $\Theta_{modulation}$ is used for phase offset estimation and $I_{modulation}$ is ideal constellation points. Θ_{upper} and Θ_{lower} are updated by comparing the error between the received constellation and the ideal constellation rotated with these two angles. This process is done for all modulation schemes considered and minimum error and angle are selected. Minimum error ($\varepsilon_k^{modulation}$) calculated for all these phase offset blocks is multiplied by a constant factor $\eta_{modulation}$, which is used to remove biasing of classification towards higher-order modulation. Value of $\eta_{modulation}$ is optimized in section 7.5.1. These six values of error are given to the *build array* FPGA element to form an array. The minimum value of this array (ε_k) is stored for comparison with the next iteration value. The further oversampling factor is increased by minimum resolution ($\Delta p = 1$ is considered) and ε_k is calculated for all modulation schemes in the same way of the previous step and compared to find the minimum for all oversampling iterations. Optimum oversampling factor ($OS_{k^{opt}}$) is used for symbol rate calculation using $SR = \frac{f_s}{OS_{k^{opt}}}$. *Min. value* ($\varepsilon_{N_1}^{min}$) for all four parallel algorithm blocks are compared for minimum and optimum modulation scheme and symbol rate is identified.

7.5 PERFORMANCE EVALUATION

In this section, the performance of the developed algorithm is evaluated. Test signal of considered six modulation schemes is generated using NI PXIe-5673, mixed with AWGN, and transmitted through SMA cable. AWGN is added in simulation as it is not possible to control noise in the physical environment for algorithm performance evaluation. Results are given to show the modulation classification accuracy with Signal to Noise Ration (SNR). SNR is defined as

$$SNR(dB) = 10log_{10}\frac{P_{signal}}{P_{noise}}$$

Where P_{signal} and P_{noise} denotes signal power and noise power.

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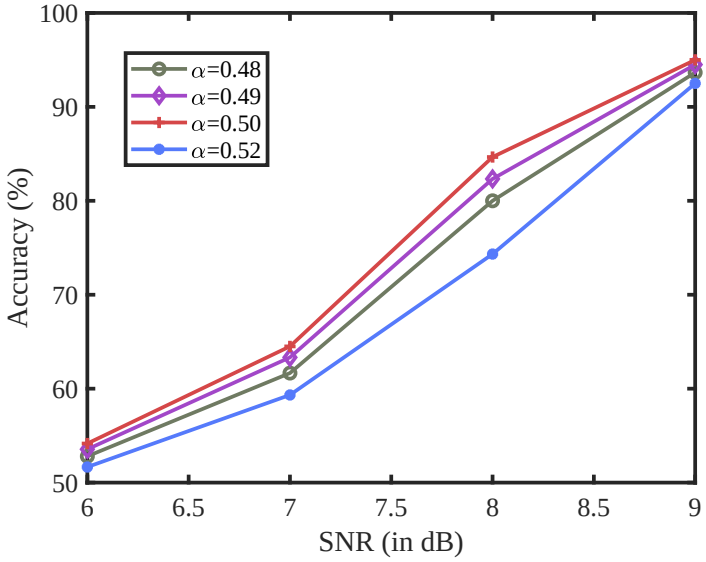

Figure 7.5 : Optimization of α (Graph shows maximum accuracy at α=0.5).

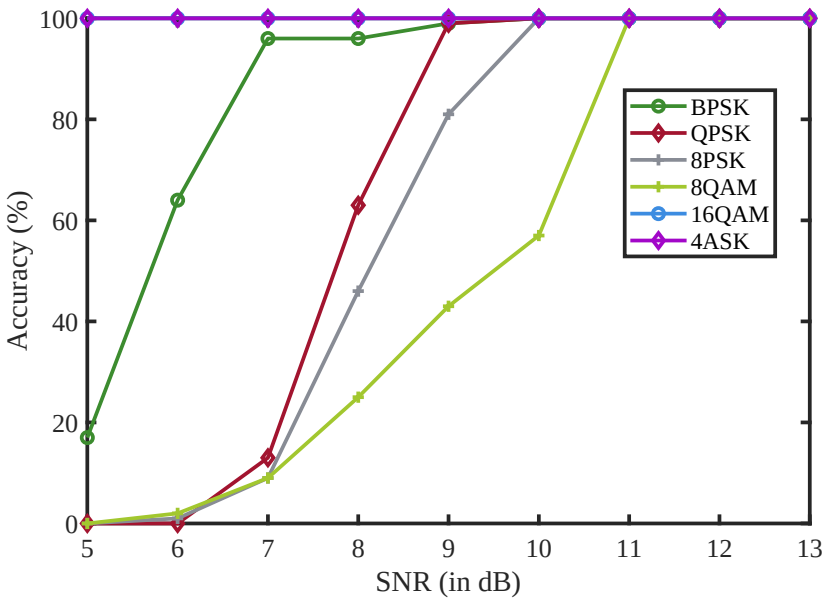

Figure 7.6 : Accuracy versus SNR for 5k-10k symbol rate range and f_s=10M.

7.5.1 Optimization of results for α

The average error of constellation of any unknown modulation scheme with ideal constellation is less for higher-order, as it has more number of symbols. This biasing is removed by multiplying error with constant factor $\eta_{modulation} = M^{\alpha}$ as shown in Figure Biasing of the modulation scheme is directly proportional to M^{α}, where M is an order of modulation. With a large number of Monte-Carlo simulations, it has been observed that, for α=0.5, average classification accuracy is maximum, as shown in Figure 7.5.

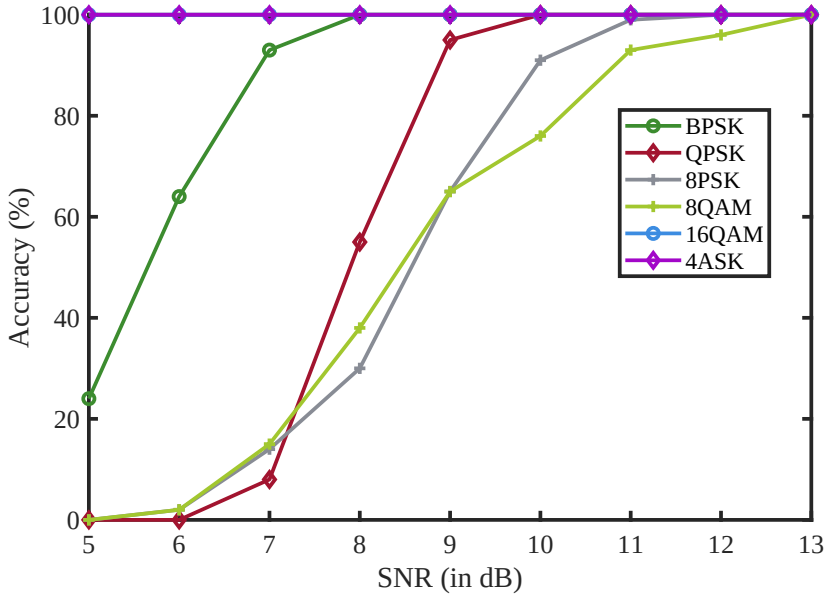

Figure 7.7 : Accuracy versus SNR for 10k-15k symbol rate range and f_s=15M.

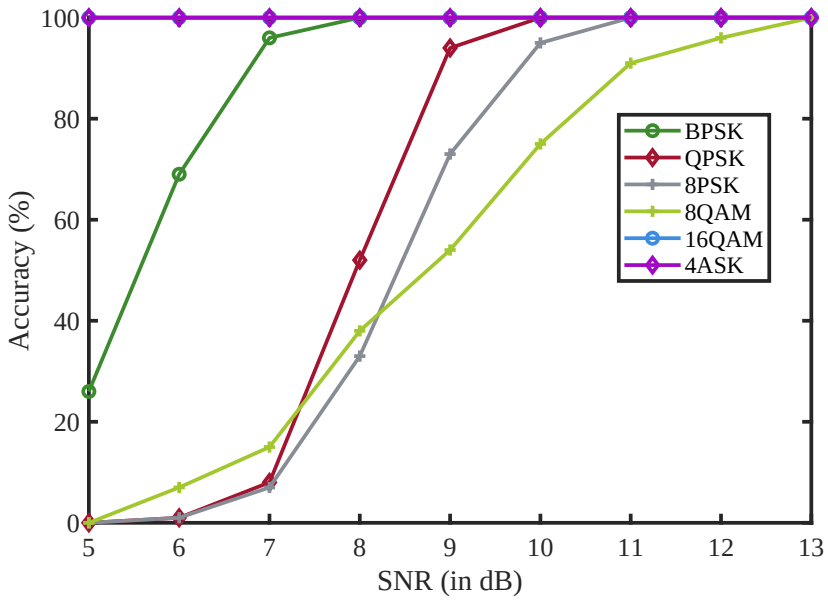

Figure 7.8 : Accuracy versus SNR for 15k-20k symbol rate range and f_s=30M.

7.5.2 Experimental Outcomes

Received RF signal is given to four parallel blocks for four ranges of symbol rate. Figure 7.6, 7.7, 7.8 and 7.9 are showing graphs for classification accuracy versus SNR for (5k-10k), (10k-15k), (15k-20k) and (20k-25k) range of symbol rates. As shown in Figure 7.6, for (5k-10k) range of symbol rate, algorithm gives 100% accuracy above 12 dB SNR. Similarly, for remaining three ranges of symbol rate, algorithm gives reliable results above 13 dB SNR as shown in Figure 7.7, 7.8 and 7.9. 200 signals of 60 symbols of each modulation scheme are considered for performance

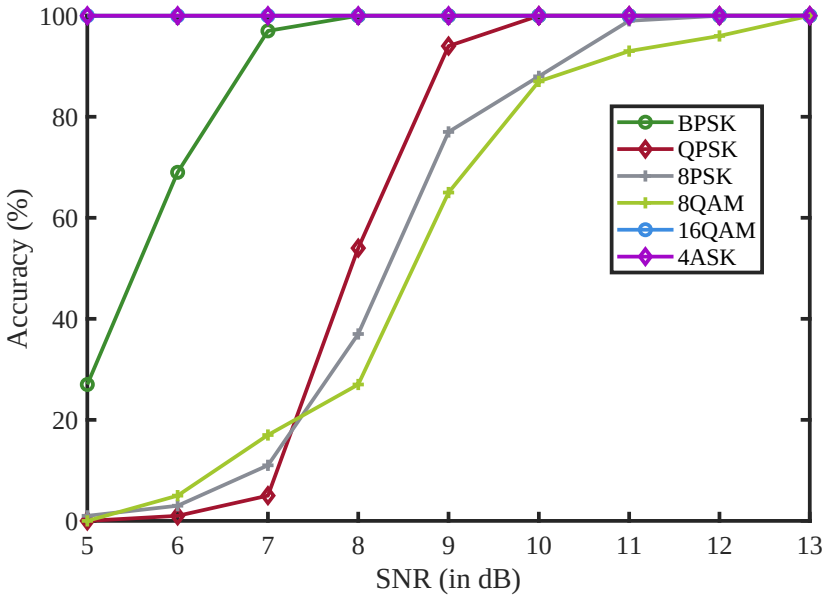

Figure 7.9 : Accuracy versus SNR for 20k-25k symbol rate range and f_s=40M.

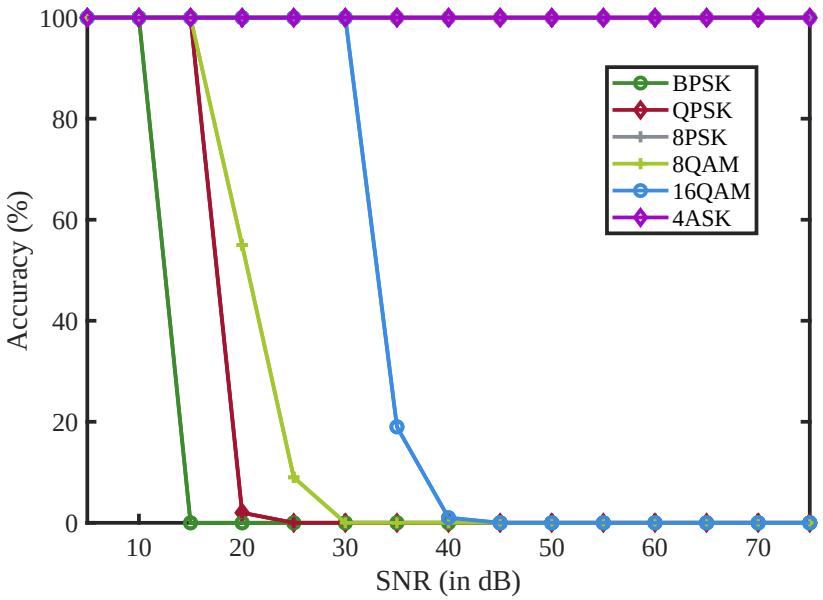

Figure 7.10 : Accuracy versus CFO for 5k-10k symbol rate range and f_s=10M.

evaluation.

7.5.3 Classification against CFO

CFO is a practical channel effect on signals transmitted, which causes abrupt degradation of classification accuracy for a small change. Effect of CFO on classification is shown in Figure 7.10, 7.11, 7.12 and 7.13 for all four symbol rate ranges. CFO is estimated and corrected

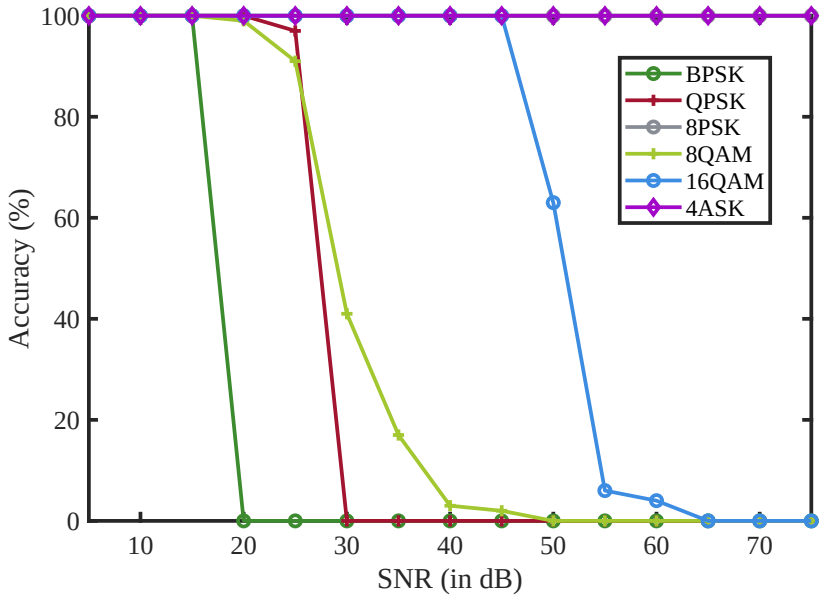

Figure 7.11 : Accuracy versus CFO for 10k-15k symbol rate range and f_s=15M.

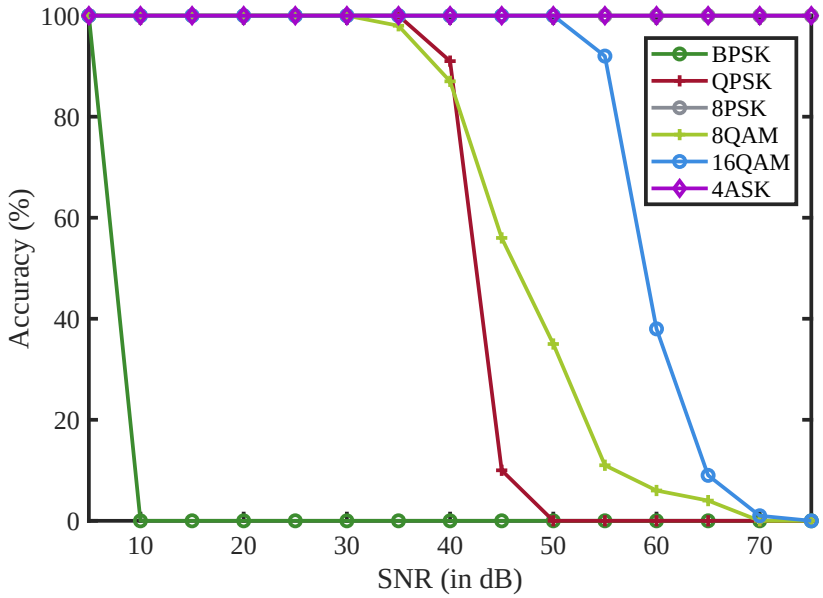

Figure 7.12 : Accuracy versus CFO for 15k-20k symbol rate range and f_s=30M.

in one of the previous steps, but results are shown with CFO to show the robustness of the algorithm from residual CFO. Relative frequency i.e. ratio of frequency offset in Hz and sampling frequency ($\Delta f_c / f_s$) can be calculated for valid comparison with other works. Random CFO is added in the transmitting channel, which can not be used for performance evaluation against CFO. So, signals with 20 dB SNR are generated and transmitted through an SMA cable. After the step of CFO correction, a known CFO is added and accuracy is evaluated for that CFO. Higher-order modulations 8PSK, 8QAM, and 16QAM have better classification accuracy compared to lower

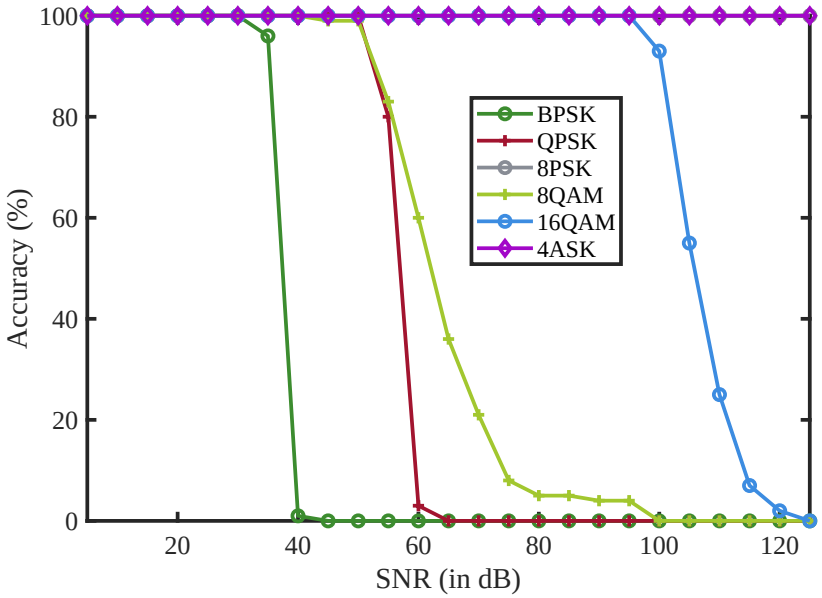

Figure 7.13 : Accuracy versus CFO for 20k-25k symbol rate range and f_s=40M.

orders. For higher-order modulation, symbol points are more, and individual symbol gets less effect of CFO as shown in Figure 7.10, 7.11, 7.12 and 7.13.

7.5.4 Comparison with related works

The classification accuracy of the proposed scheme is calculated for signals containing 60 symbols. In [Mirarab and Sobhani, 2007], Higher-Order Statistics (HOS) is used for classification, which gives 70% and 77% accuracy for 500 symbols at 10 dB and 15 dB SNR but the proposed method gives 94% and 100% accuracy respectively for 60 symbols. Mel-Frequency Cepstral Coefficients (MFCC) of signal, DCT of signal, DWT of signal, and DST of the signal have been used for feature generation and SVM/ANN is used for classification in [Keshk *et al.*, 2015]. Modulation classification accuracy of [Keshk *et al.*, 2015] for 8PSK using MFCC features of signal and SVM/ANN (RPROP/VLR) classifier is always less than 100% below 25 dB SNR, whereas in our case it is 100% above 12 dB SNR. Also, the classifier of [Keshk *et al.*, 2015] requires training of the ANN model with large sample features set, and every time one or more features are changed, it needs to be re-trained before classification. In [Wong *et al.*, 2008], a naive Bayes modulation classifier has been used to calculate the posterior probability of modulation schemes for fourth and sixth-order cumulants. Classification accuracy for naive based classifier is 96.66% in [Wong *et al.*, 2008] for 512 symbols, but proposed method has 100% accuracy for 14 dB SNR. 95.75% accuracy has been attained by [Wong *et al.*, 2008] at 14 dB SNR when SVM with the poly kernel is used, but in the proposed method 100% accuracy is achieved for the same SNR.

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