1
Introduction

The reign of power electronics dates back to more than a century now. The journey started with what is known as the "Classical era" in the early 20th century, when Peter Cooper Hewitt invented the glass-bulb pool-cathode mercury-arc rectifier. The first vacuum diode was invented by J. A. Fleming in 1904, silicon valve by G. W. Pickard and vacuum tube by L. Forest in the year 1906. These inventions led to the development of first Electronic amplifier, and a vacuum triode was developed by L.forest in 1907, whose principle formed the basis for many electronic devices. The vacuum diodes ruled the market until the late 1920s. They were replaced by mercury equipment in the 1930s due to the problems associated with vacuum diodes. The disadvantages of the vacuum tubes included limited life of a few thousand hours, bulkiness, requiring an internal power heater, substantial of power dissipation and rise in temperature during operation and high cost. In the year 1948, Bardeen, Brattain and Shockley of Bell Labs revolutionized the electronics market with the invention of the transistor. The period between mid 50s to early 60s, the electronic market migrated from vacuum tubes to transistors, paving a path for many research opportunities to be conducted in the coming future.

Another major invention, which marked the era of first-generation power devices and led to their commercialisation, was that of silicon-based thyristors by General Electric in 1956. Before this, operations of semiconductors were confined to low currents and low voltages. This era of first-generation devices lasted till 1975. From 1975 to 1990, second-generation devices became prevalent with the development of bipolar junction transistors (BJTs), gate turn-off thyristors and metal oxide semiconductor field effect transistors (MOSFETs). The development of insulated gate bipolar transistor (IGBT), marked the era of third-generation devices, bringing intelligent power devices.

Widespread use in different applications has made power electronics ubiquitous. It has established itself as an important disciple at the core of power and energy control. The electronics processing of power is needed at domestic as well as industrial domains to power the apparatus and equipment. Majority of these supplies substitute switching power converters in place of linear power supply due to the benefits like low losses, prolonged equipment life, low maintenance, small size, the capability to operate at various voltage and current levels with improved controllability. Therefore, the power converters form an integral part of the power electronics to transform one type of electric energy to another. Essentially the basic elements that make a converter are- (a) Linear Elements: These include intermediate energy storage as well as filtering reactive elements like inductors, capacitors and mutual inductances (transformers). (b) Non-linear Elements: These include semiconductor devices like electronic switches and diodes.

Depending on the type of energy conversion, power converters can be divided into four major categories.

- AC input to AC output.
- AC input to DC output.

- DC input to AC output.
- DC input to DC output.

The underlying common attribute amongst all these static converters is that they all are electrical networks which transfer energy from one form to another using semiconductor switches. The conversion is carried out by proper sequential operation (modulation) of these switches. These power converters operating in the switching mode, have two discrete switch states (conducting and non-conducting). The switching should be carried out to ensure the transition, from one state to another, is done at a low loss while meeting the desired requirements. Ideally, a converter should regulate the power flow, between the source and the load, with 100% efficiency. Therefore, another important requirement that runs common is that in any power conversion process higher efficiency is vital. It is so because of two reasons: the high worth of the energy wasted and the complication in eliminating the heat generated due to dissipated energy. Hence, the converter efficiency could be increased by minimizing the losses occurring in the switches.

Achieving the ideal case of 100 % efficiency corresponds to the ideal switches exhibiting the following characteristics: No limit on current it can carry during ON state, No limit on voltage it can withstand during OFF state, Zero ON-state resistance- no voltage drop, Infinite OFF-state resistance- no leakage current and, No switching delays- ability to switch at any speed.
The ideal switch and its respective waveforms are shown in Fig. 1.1 where, i_{sw} and v_{sw} represent current through and voltage across the switch, respectively, and DT_s is the ON-time. As shown,

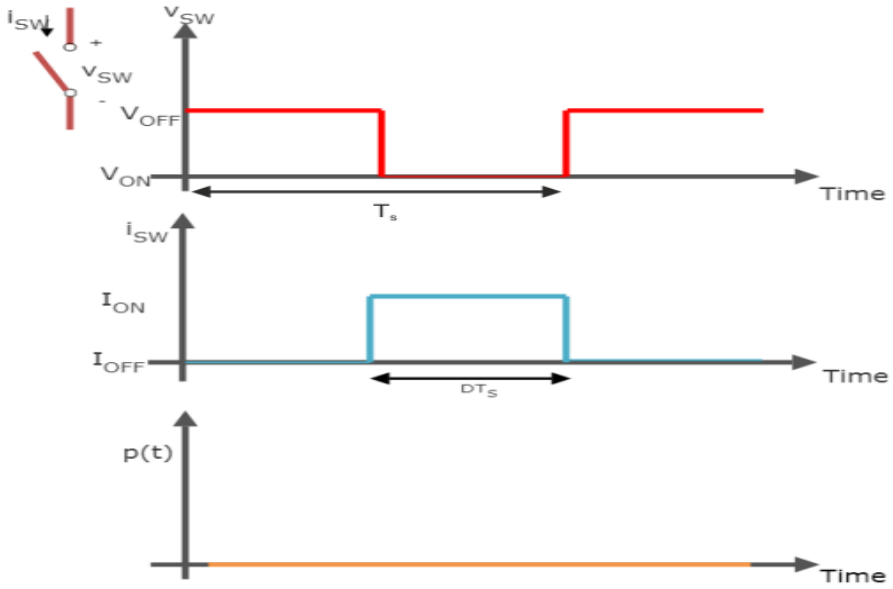


Figure 1.1 : An ideal switch and it's switching waveform (voltage, current, and power)

during the conduction as well as switching period, the power loss is zero. Therefore, an ideal switch is said to have no losses, unlimited power handling capacity and unlimited switching speed.

However, a practical switch has limitations in terms of limited power handling capacities, finite ON-state and OFF-state resistances and limited switching speed. As a result, it experiences losses due to switching transition (switching losses) and while in ON/OFF state (conduction losses), and becomes a source of loss in a practical converter.

A typical waveform for a practical switch is shown in Fig. 1.2. Although the exact switching

waveform is dependent on the device under use, the presented waveform is reasonably good to evaluate the associated losses. Here, again, i_{sw} and v_{sw} represent current through and voltage across the switch, respectively, but, for simplicity, DT_s is the ON-time plus the switching delays. t_{on} and t_{off} are the delay during ON and OFF switch. The average power dissipation over a switching

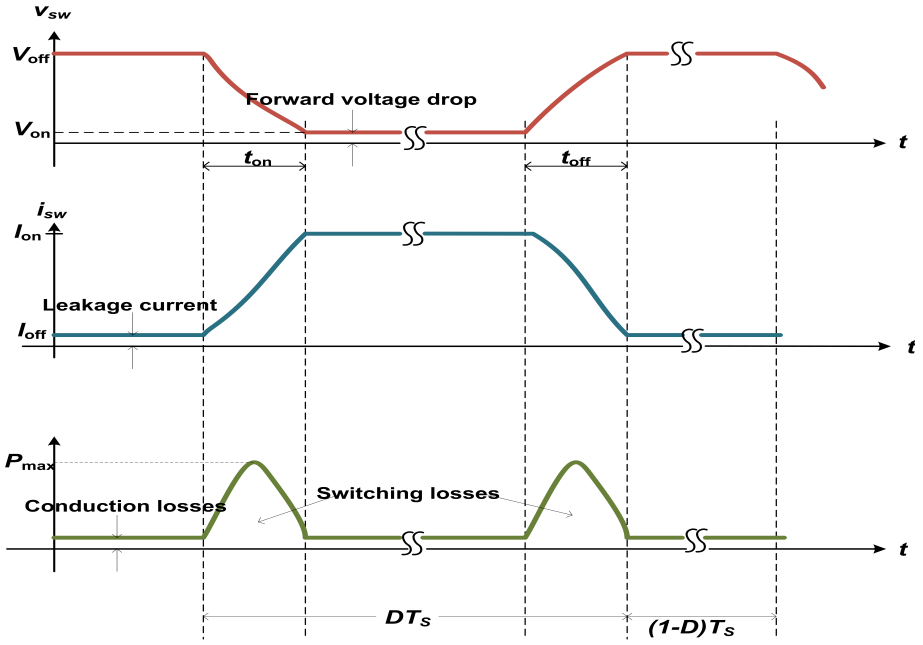


Figure 1.2 : Switching waveform for a practical switch (voltage, current, and power)

cycle (T_s) is

$$\begin{aligned} P_{avg,loss} &= \frac{1}{T_s}\int_0^{T_s} v_{sw} i_{sw}\, \mathrm{d}t \\ &= P_{avg,swit} + P_{avg,cond} \end{aligned}$$

Where, $P_{avg,swit}$ and $P_{avg,cond}$ are switching and conduction losses, respectively. They are evaluated as

$$P_{avg,swit} = \frac{1}{T_s}[\underbrace{\int_0^{t_{on}} v_{sw} i_{sw}\, \mathrm{d}t}_{on\ switching\ loss} + \underbrace{\int_{DT_s - t_{off}}^{DT_s} v_{sw} i_{sw}\, \mathrm{d}t}_{off\ switching\ loss}] \tag{1.1}$$

$$P_{avg,cond} = \frac{1}{T_s}[\int_{t_{on}}^{DT_s - t_{off}} V_{off} I_{on}\, \mathrm{d}t + \int_{DT_s}^{T_s} V_{on} I_{off}\, \mathrm{d}t] \tag{1.2}$$

$$= V_{off} I_{on}(D - \frac{(t_{on} + t_{off})}{T_s}) + V_{on} I_{off}(1 - D) \tag{1.3}$$

Here, $P_{avg,cond}$ represents the conduction loss in the switch and is a function of the load current. $P_{avg,swit}$ is the power loss linked with turning ON and OFF of switch. This is a function of the switching frequency and is independent of load current.

The different kinds of losses in a power converter with practical switches could be summarized as

1. **Conduction losses**: Such losses are due to the presence of the resistive parasitics in power converter constituents like the switch , the Equivalent Series Resistance (ESR) of capacitors, the DC Resistance (DCR) of Inductor, and the resistors for traces and sense. Moreover, they are also a function of the RMS currents. As the shape of the current waveform differs for each component, the value of RMS current also differs. Furthermore, for each component the resistive parasitic value is also different.

2. **Switching losses**: These losses are as a result of the voltage-current overlap period during switching. These are a function of the switch's operating frequency, voltage across the junction capacitances of the switch, the value of these junction capacitances and the current flowing through the switch.

3. **Gate-drive losses**: These losses are due to the power taken to drive the field effect transistor (FET) gate. It is a function of the switching frequency, FET gate charge value and the gate drive voltage used.

Another set of losses taking place in a converter consists of inductor core losses, reverse recovery losses, losses due to leakage currents and standby losses. For a converter, these losses could be accounted using common power losses equation which are covered elaborately in the existing literature [Trescases and Wen, 2011], [Qahouq *et al.*, 2007], [Klein, 2006], [Zhou *et al.*, 1997]. Some common power loss equations for buck converter is pictorially represented in Fig. 1.3.

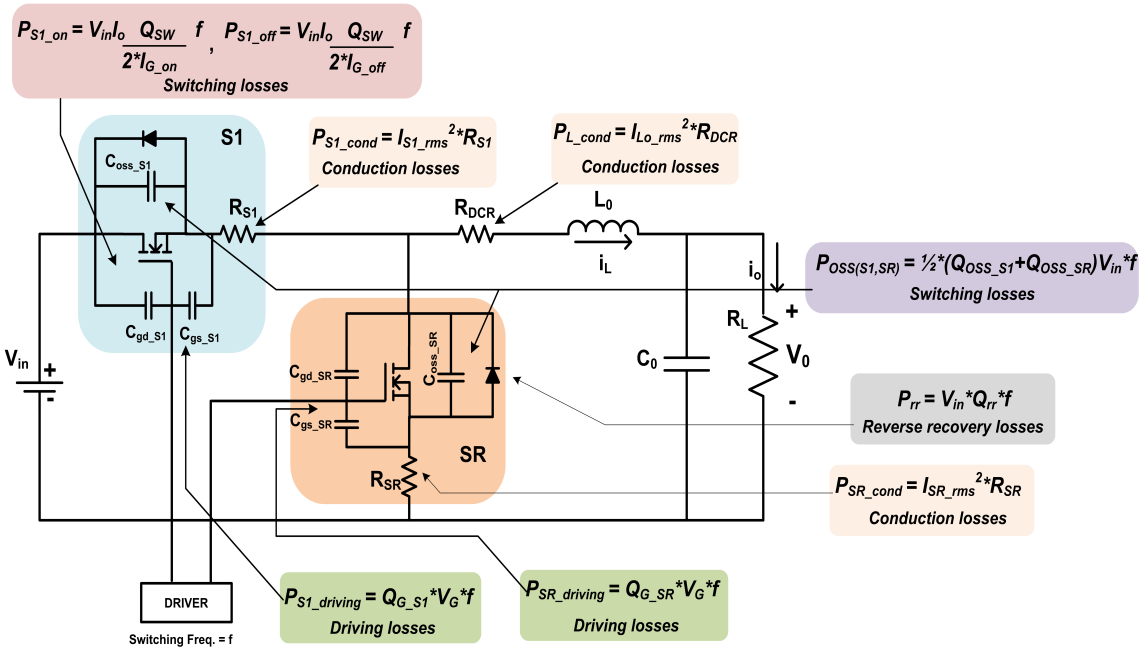
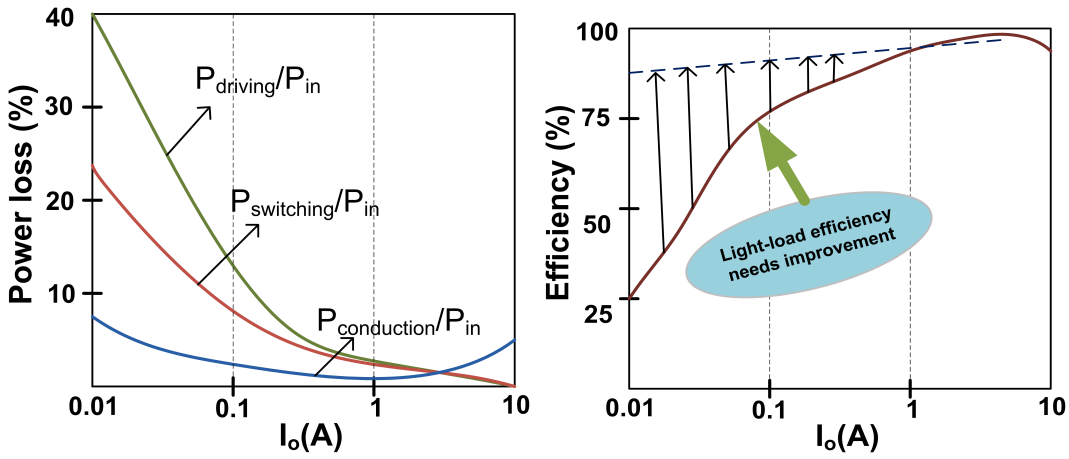


Figure 1.3 : Sources of power loss in a synchronous buck converter [Qahouq *et al.*, 2007].

In order to minimize the conduction losses, the ON resistance of the switches must be as low as possible to minimize the voltage drop in the ON-state, and during OFF-state, the leakage current must be negligible. The conduction losses depend on the voltage across and the current passing through the switch, in contrast, the switching losses are independent of the load current and happen as a result of energy loss every time a switch changes state. Therefore, the way these

switches are operated or otherwise called the switching pattern is not only crucial in meeting the application requirements but also with its efficient operation. Depending on the switching pattern, the converters are again broadly categorized as those with Fixed switching frequency and Variable switching frequency operations. In a fixed frequency operation of converters, since the switch is switched ON/OFF at a fixed interval, the associated switching losses contribute a fixed loss independent of the load current [Erickson and Maksimovic, 1995]. Hence, at low loads these fixed switching loss become very significant Fig.1.5(a).

Majority of the works, use fixed frequency control signal for their operation. This time driven periodic switching strategy has received attention due to its simplicity in analysis and design. The power converters are composed of reactive components, whose choice is strongly dependent on the system switching frequency and thereby fixed frequency is preferred for the ease of design process. However, this design process chooses system parameters for improving single operating point efficiency only. In view of the power converter under consideration being inherently non-linear, with their behaviour highly dependent on the operating point, fixed frequency switching operation will not result in maintaining maximum efficiency at various line and load settings. This is due to various types of losses being dominant at different load levels in a converter. The power losses normalized to input power for a buck converter and its typical efficiency curve is shown in Fig. 1.4.



(a) Power losses normalized to input power. (b) Efficiency curve

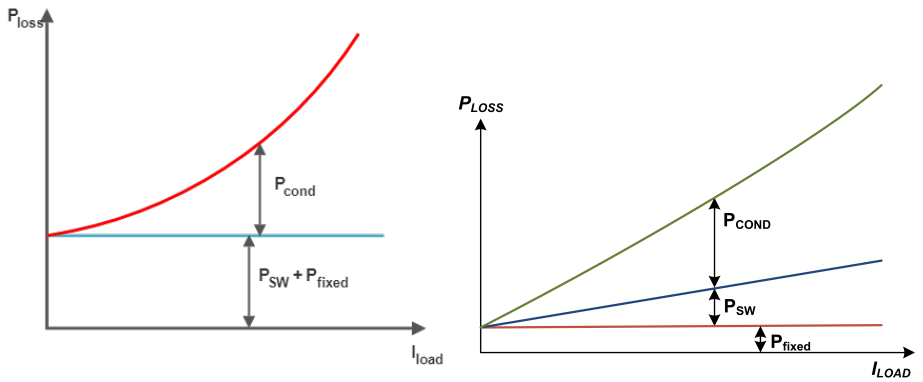
Figure 1.4 : Plots for typical buck converter [Qahouq *et al.*, 2007].

Fixed frequency operation at low loads exhibit fixed switching and driving losses and thereby, efficiency of the system tails off. A study made by International Telecommunication Union, presented at 2012 CoC EPS meeting, revealed a substantial drop in efficiency, at loads lower than 10%, in power supplies [R. Bolla *et al.*, 2012]. Power supplies are widely adopted in all types of communication equipments, computers, and home appliances. In the late 1990s, the exponential rise in consumer electronics and data-processing equipment has led to the proposal of different prerequisites in order to minimize the power consumed at light-load. Amongst which some are voluntary organizations like the U.S. Environmental Protection Agency ENERGY STAR and European Commission (EC) Code of Conduct (CoC). There are also compulsory programs, specified as standards. They include the U.S. Department of Energy (DOE) Energy Independence and Security Act (EISA), the California Energy Commission (CEC) Title 20 Appliance Efficiency Regulations and, the EC Ecodesign Directive for Energy-Related Products. These program were formulated with the agenda to bring tighter no-load power consumption and higher active-mode

efficiency requirements [Fassler, 2017].

Currently, the power supply market is at the brisk of a major focus shift which requires efficiency improvements at all load range to be in the forefront of performance needs. Economic and environmental concerns have been a reason for this shift. For example, the 80 Plus incentive program [80p, 2004] and Climate Saver Computing Initiative (CSCI) [CSC, 2007], already implemented, need the power supplies for computer applications to have more than 80% efficiency for the complete (100% to 20%) load range. This efficiency aims have made it to the U.S. Environmental Protection Agency's (EPA) Energy Star specifications [EPA, 2009] in 2009. However, there is a need to make the light load efficiencies exceed the latest Energy Star specifications for many of the largest computer, telecom, and network equipment manufacturers. Moreover, the requirements have been extended down to 10% and even 5% loads. It is expected that energy efficiency requirements in the future program will be even more demanding in terms of efficiency, harmonic distortion specifications and, power factor for power supplies. This thesis focuses on control schemes to improve efficiency in power converters, both AC-DC and DC-DC, which are used at the front-end stages in power supplies.

In order to achieve consistent efficiency for the complete load spectrum, novel models change switching frequency as per the load, thus, the frequency dependent losses can be reduced to achieve lower losses and hence higher efficiency. This is illustrated in the Fig.1.5(b). By altering switching frequency, based on the current status of the system, the efficiency and performance of the converter could be retained for the complete range of operating conditions. The next section gives a comprehensive view of the existing strategies to reduce switching losses at low-loads to obtain a flat efficiency curve, for a wide range of line and load variation.



(a) Fixed frequency operation (b) Variable frequency operation

Figure 1.5 : Variation of losses in a converter with load [Erickson and Maksimovic, 1995].

1.1 LITERATURE REVIEW

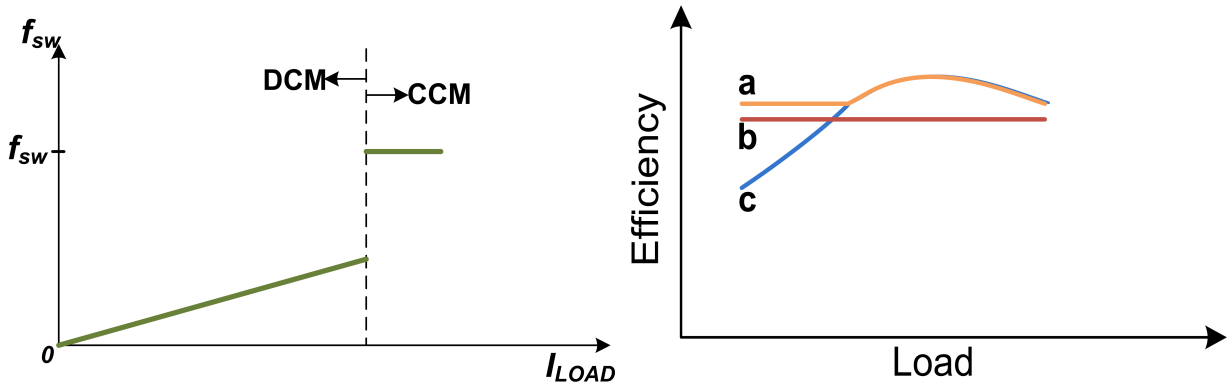
The literature review has been carried out with an aim to cover the existing variable frequency schemes to minimize switching losses. The Section has been divided into three sub sections wherein, strategies pertaining to the DC-DC stage (for voltage regulation), AC-DC stage (for power factor correction), and for a single-stage PFC converter, used at the front-end of power supplies are discussed.

1.1.1 Control schemes for DC-DC stage of AC-DC-DC Converter

A variable-frequency control technique finds widespread applications in point-of-load converters because of its fast transient response, and improved light-load efficiency. They have been developed, over the time, to adapt power delivery to different load demands. The adaptive quality is achieved by dynamically adjusting the control or/and by adjusting the hardware structure of the converter. [Huffman and Flatness, 1993], [Zhou *et al.*, 2000].

Variable switching frequency strategies for light loads efficiency improvement in conjunction with discontinuous conduction mode (DCM) have been used. For example, [Arbetter *et al.*, 1995] proposes a variable switching frequency dependent on the load current for a synchronous buck converter, operating in DCM. In DCM, as the inductor current does not become negative the conduction losses are reduced. Moreover, it reduces switching losses due to lower switching frequency and also because the rectifier is turned off at zero current. However, due to DCM operation of the converter and reduced switching frequency, a large ripple current is generated which requires a larger capacitor at the output for filtering.

A tailored approach, called hybrid control, was proposed in [Wang *et al.*, 1996], to tackle this issue. In this work, a DC-DC converter operates in the continuous conduction mode (CCM) with fixed switching frequency at heavy loads, and in DCM with variable switching frequency, that is also a function of the load current, at light loads [Zhou *et al.*, 1997], [Wang *et al.*, 1997]. The switching frequency transition and corresponding efficiency curve is shown in Fig. 1.6.



(a) Use of the CCM near full load, and variable frequency DCM at light load.

(b) Efficiency v/s Load for a) Hybrid control b) Variable frequency control c) Fixed-frequency control

Figure 1.6 : Mode hopping with load [Erickson and Maksimovic, 1995], [Zhou *et al.*, 1997].

In pulse frequency modulation (PFM), the switching frequency is made to reduce as the load reduces, thus at light loads switching losses are reduced. Two PFM schemes working in DCM have been proposed [Erickson and Maksimovic, 1995]: (i) constant peak inductor current and (ii) constant ON-time, which can also be dynamically adapted [Sahu and Rincon-Mora, 2007]. For both the cases, there is an optimal value of peak current and ON-time that gives maximum efficiency [Erickson and Maksimovic, 1995].

Depending on the load current, Mode-hopping between CCM and DCM modes is suggested. To mode-hop, a digital pulse width modulation (DPWM) controller is used in [Prodic and Maksimovic, 2000] to control the working mode of the converter, depending on the output current. However, detecting this conversion point is complex and may cause false signals. A smooth PFM/PWM transition is difficult to achieve [Chen *et al.*, 2008] because of their structural difference. Furthermore, hybrid controllers can provoke relatively large output voltage transients when

switching between pulse width modulation (PWM) and pulse frequency modulation (PFM) control modes.

This dual-mode converter (PWM/PFM) [Chen *et al.*, 2008] is a widely accepted scheme for efficiency improvement. However, as shown in Fig. 1.7, there is a dip in region C. This implies a reduction in efficiency where PFM curve and PWM curve cross each other. Hence, the dual-mode modulation is not effective for efficiency improvement in region C. This led to the proposal of a novel load sensor in this tri-mode buck converter in [Huang *et al.*, 2006] for dynamic switching between the three modes, namely, PFM mode, pulse-skipping modulation (PSM) and, PWM mode. To decrease the switching conduction loss, PSM mode masks the part of the switching signal of power transistor and then get better efficiency. Including PSM mode improves the dip in efficiency at the crossover of PWM curve and PFM curve. Thus, the tri-mode buck converter provides high efficiency over a wide range of load.

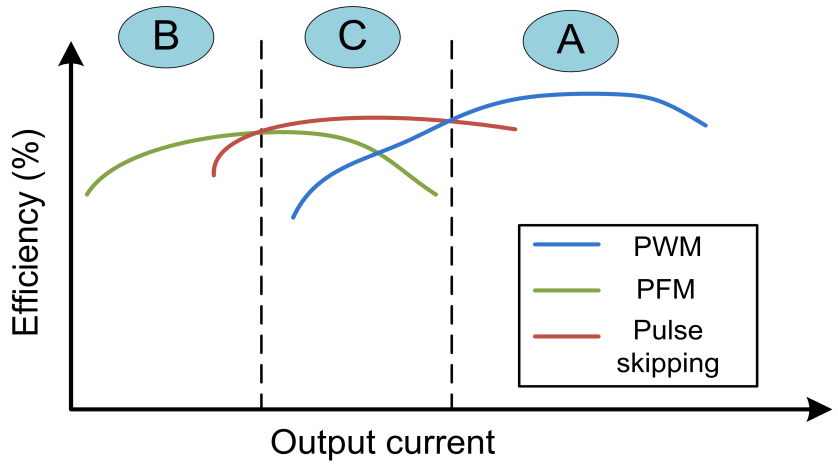


Figure 1.7 : Three control modes converter and their efficiency as functions of output current. [Huang *et al.*, 2006].

This Pulse skipping modulation, discussed above, is another technique to reduce switching loss while maintaining good output voltage regulation. The pulse skipping mode can reduce switching loss by keeping the switch in the OFF-state for several switch cycles. As a result, the switching losses in gate driver circuit and switch are reduced [Angkititrakul and Hu, 2008]. In Burst Mode (also called pulse-skip mode), during active mode a burst of energy to the output is released, by cyclically switching the transistors ON/OFF at a fixed frequency (the same as in PWM), while during an inactive period, switches stay permanently OFF [Kok *et al.*, 2017]. The duration of the inactive period depends on the load current, hence at low loads an equivalent switching frequency is obtained. In [Feng *et al.*, 2013], this principle has also been extended for light-load efficiency improvement of resonant DC-DC converters .

To control the burst in active period, two schemes have been proposed [Trescases and Wen, 2011] : (i) Constant duty cycle [Kok *et al.*, 2017]; and (ii) Constant inductor current [Angkititrakul and Hu, 2008], which found application in various commercial DC-DC converters like LT1303, STBB1-AXX, TPS6120x,and L6920. The traditional burst mode control measures the voltage feedback of a converter and then using a hysteresis comparator, it compares measured voltage with the two reference voltages [Huh *et al.*, 2004]. This scheme adapts to the load as shown in Fig. 1.8. At heavy load, the feedback loop stays unaffected by the burst mode control circuit, thus the converter operates in normal PWM mode. However, during light load feedback voltage becomes lower than the lower reference voltage and hence, the feedback loop is ceased by the burst mode

control, making the converter go into burst mode.

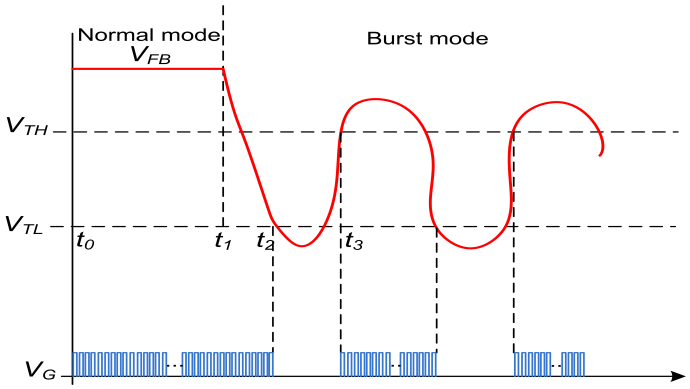


Figure 1.8 : The operation principle of the conventional burst mode [Lee *et al.*, 2013].

In [Telefus *et al.*, 2004] another novel control algorithm called Pulse Train (PT) control algorithm was proposed. The output voltage is regulated depending on the presence and absence of power pulses, instead of using PWM. When the output voltage becomes higher than the reference level, low-power sense pulses are generated sequentially till the voltage level reaches to the desired level. On the other hand, for the output voltage less than the reference level, high-power power pulses are generated. Even though the duration for the sense and power pulses are the same; more power will be delivered to the load during a power pulse due to the longer ON time of the switch. The ratio between the ON-time duration of the switch in a power pulse and of that in a sense pulse is decided by trading off between power regulation from full load to low load and the output voltage ripple. A method having some similarity with Pulse Train control was proposed in [Luo *et al.*, 2002] with inferior characteristics. Pulse train control scheme presents low and high pulses with different frequencies [Telefus *et al.*, 2004]. ON time durations for low and high pulses are fixed using either generated using peak current mode control [Wang and Xu, 2012], predefined values [Ferdowsi *et al.*, 2005] or digital control [Kapat, 2014]. However, present pulse train control techniques cause unpredictable high periodic behavior [Kapat, 2014].

Several other techniques have been introduced for light load efficiency improvement in DC-DC converters. One of these technique is resonant switching, which reduces switching loss by making either the current through or the voltage across the switches nearly zero, whenever the switch changes states [Smith *et al.*, 2000], [Song *et al.*, 2005]. A low-power [Zhou and Rincon-Mora, 2006] and medium-power [Choe *et al.*, 2014] DC-DC converter application of the soft switching techniques exist in the literature. However, this scheme employs extra components, like switches, capacitors, or inductors, causing an increase in cost and size. Furthermore, these additional components lead to reduced efficiency as they are placed on the power delivery path. Hence, the resonant switching technique does not make an ideal scheme for low voltage applications.

Another technique of variable frequency operation is the Hysteresis control. The hysteretic DC-DC converters do not need any additional circuitry such as error amplifiers for stability compensation, thus they form a low cost architecture having fast transient response. Hence, these converters are very popular for managing power in portable devices. In a hysteretic buck converter [Seo *et al.*, 2017], a feedback ripple signal is generated from the inductor current or the output voltage. The switching pulses for the converter are obtained by comparing the feedback signal with the references of the hysteretic comparator. The hysteretic buck converter is categorized as current or voltage mode hysteretic control depending on the generation method of the feedback ripple. For a voltage mode hysteretic controlled buck converter , authors in [Bao *et al.*, 2013] derive condi-

tions of ESR in the output capacitor for normal operation and mode shifting. This control has just a hysteresis band with a low reference and a high reference. The aim is to ensure that the tracking references is kept inside the hysteretic band. The choice of high and low reference values decide the ON/OFF instants of the switch to regulate the output voltage. However, the voltage-mode hysteretic control faces challenges like offsets in comparator, high noise sensitivity, and driver delays during steady-state regulation. In [Duan and Huang, 2006] a current-mode control architecture with variable switching frequency is presented. This technique is advantageous on account of simple controller design, better transient response with no increment in switching frequency at steady state, and easier practical implementation. Authors in [Miao *et al.*, 2019] propose a novel concept of hybrid modulation using hysteresis current mode and burst mode (HCM-BM)in order to improve light load efficiency in a boost converter.

In general, a DC-DC converter has a wide spectrum of input voltage and load current range. So far the control schemes like Pulse frequency modulation, hybrid control, and pulse skipping modulation varied the switching frequencies to improve efficiency at low load; however, the heavy-load efficiencies, which are also important, are not optimized. In [Sun *et al.*, 2009] the authors pointed that by decreasing switching frequency with the loads during DCM operations, even though there was an improvement in efficiency at very light load, but for load between 20% and 100% there was no improvement in efficiency. Especially, when the load decreases from the peak efficiency point, the efficiency drops very quickly, indicating a room for efficiency improvement during CCM. As shown in Fig. 1.6(a), the switching frequency remains unchanged during CCM operation, hence to improve the efficiency in CCM, switching frequency can be slightly varied using adaptive ON-time control. An adaptive frequency control in [Al-Hoor *et al.*, 2007], although can further improve heavy-load efficiencies, the additional control circuits, including analog-to-digital converters and minimum input power tracking circuits, are required and thus result in increased power loss. An efficiency-optimized switching-frequency (EOF) control method is proposed in [Liu *et al.*, 2011]. Adaptive Frequency-optimization (AFO) controller, which tracks maximum efficiency point corresponding to minimum input current and causes step changes in frequency. However, it does not accommodate fast load transients [Al-Hoor *et al.*, 2009], [Abu-Qahouq *et al.*, 2009]. Variable frequency modulation with both ON and OFF time as control inputs, provides an improved transient performance. But the method requires an accurate model of the converter dynamics, and designing and implementing a multi-loop controller [Priewasser *et al.*, 2014]. Adaptive FET modulation scheme uses multiple Field Effect Transistors (FET), with different characteristics, applied in parallel such that driven FETs and their gate driving voltage are adaptive to load current. Howbeit, the cost involved with additional circuitry makes the overall system to be a costly pursuit [Abdel-Rahman *et al.*, 2008].

Apart from these adaptive schemes, since DC-DC converters are intrinsically variable structure systems (VSS), Sliding mode control (SMC)[Mattavelli *et al.*, 1993], which is inherently variable frequency control, serves as a natural choice. The main advantage of this control scheme is its robustness to system parameter and load variation. The control law involves use of a signum function, and the generated discontinuous control signal requires, ideally, infinite switching frequency [Utkin, 1993]. Several methods to deal with reduction of the switching frequency associated with SMC have been discussed [Cardoso *et al.*, 1992]. Hysteresis Method (HM) has been most commonly adopted of them [Tan *et al.*, 2005]. This involves replacing the signum function in SMC by a hysteresis comparator, thus carrying out the variable frequency control action at finite frequency. The SMC would be discussed in detail in the later part of the chapter.

DC-DC converters are also used for active power factor correction (PFC) in a two-stage AC-DC-DC conversion. Majority of the electronic equipment use a full-bridge rectifier for AC-DC conversion. The rectification unit is a non-linear load and thus the current drawn by it, from the grid, gets distorted. Currently the number of such non-linear loads, getting connected to the

grid, is increasing exponentially. This raises concern not just regarding power quality but also of energy efficiency. Therefore, [Fiorentino *et al.*, 2013] the energy efficiency and power quality of such converters have become increasingly important and the following subsection discusses the control schemes covered in the literature for efficiency improvement of PFC converters.

1.1.2 Control schemes for PFC stage of AC-DC-DC Converter

Products that wish to qualify for the Energy Star program must meet or exceed certain efficiency requirements. Also, the total harmonic distortion (THD) must meet the IEC 61000-3-2 standard which sets harmonic current limits for different categories of appliances. These standards and regulations are increasingly strict about light load conditions because more and more devices tend to stay in light load for longer periods of time (e.g. computers, TV boxes, etc.); and the poor performance in light load condition counts for a significant percentage of the total power loss. In line with the above aim, to improve light load efficiency while keeping the %THD within limits, several similar efforts have been made by the community.

The concept of multi-mode operation of converters in CCM and DCM depending on load conditions is also practised for PFC application, to improve efficiency at light load conditions. In paper [Wang and Tzou, 2011], a digital multi-control method was incorporated with variable frequency control to improve the characters of both efficiency and total harmonic distortion (THD). The front-end boost PFC converter used in server power applications is designed to be operated in CCM, however, when the converter is operating in light load condition, it will operate in DCM condition and the voltage conversion ratio becomes nonlinear as a function of inductor current and input voltages, this leads to increased line current distortion [De Gusseme *et al.*, 2007]. An important challenge of multimode control is to ensure smooth transition between the control strategies as load changes. Existing multimode control solutions for PFC can be classified into two main categories, namely CCM-DCM control scheme with reduced switching frequency as load reduces and addition of ON-OFF control scheme to existing active mode control. For the first category, there are adaptive frequency CCM/DCM current control [Chen and Maksimović, 2010] that provide input current shaping in both CCM and DCM with reduced switching frequency as load reduces and adaptive ON-time control [Li *et al.*, 2009] where, the switching frequency is reduced to about 25% when operating in light load condition and the switching frequency becomes higher as the line current is increased. [Wang *et al.*, 2010] combines continuous and critical conduction modes and has the merits of simple control, high efficiency in a light-load condition, and being fit for personal computer (PC) power applications.

The previous research on PFC structure can increase the efficiency of the PFC converter with auxiliary switches that are triggered by zero-current switching (ZCS) and zero-voltage switching [Wang *et al.*, 2013b], [Jang *et al.*, 2006], [Wang, 2003]. Nevertheless, the drawbacks are the cost and complicated control method. The burst-mode operation [Hwang and Chee, 1998], [Lo *et al.*, 2008] can make the PFC circuit operate in active mode and sleep mode alternatively, leading to reduced switching frequency at light load. Nevertheless, the burst-mode operation is only limited to extremely light load condition because of its large RMS current. Some research has only addressed the efficiency at the no-load or stand-by condition for PFC converters, and does not address the entire light load range [Lee and Lai, 2009], [Lee *et al.*, 2011]. One research paper [Jang and Jovanovic, 2009] devises a method to improve the light load efficiency for all PFC converters using conduction angle control, which is an ON-OFF control scheme that is added to existing active mode control and reduces constant losses at light load by turning the PFC ON and OFF to regulate the output voltage within a hysteresis band. A major problem with these ON-OFF control schemes [Jang and Jovanovic, 2009] [Lo *et al.*, 2008], is that the peak current increases and the PFC turn-OFF time period reduces as load increases, making it difficult to exit these control modes without a current limit and a large load jump in a standalone PFC control solution [Lim and Khambadkone, 2012].

Adaptive switching and adaptive frequency control techniques are introduced to reduce switching losses and improve efficiency at light loads in [Chen and Maksimović, 2010]. In [Yu *et al.*, 2011], the output load range is divided into several sections and efficiency optimization is achieved through operating the converter at different switching frequencies. For two-stage PFC design, turning OFF the PFC stage has been proven as an effective method to reduce power loss [Lo *et al.*, 2008].

Irrespective of the methodology adopted and topology used, the fundamental concept behind power factor application is to make the input current follow the input voltage, thus the system should present itself as pure resistive load to the supply. Therefore, the notion of Loss free resistor (LFR) becomes an inherent choice for PFC application. Initially, the concept was confined to the acknowledgement that certain switching converters like buck-boost, *Ć*uk, SEPIC etc., working in DCM, display inherent property of being resistive at the input. Later, the notion evolved from relying on the DCM operation to using feedback controllers to attain switching converter with resistive input impedance. Several works, employing LFR for PFC, could be found in the literature [Singer *et al.*, 2004], [Bist and Singh, 2015], [Nasirian *et al.*, 2013], [Cid-Pastor *et al.*, 2013], [Marcos-Pastor *et al.*, 2015], [Haroun *et al.*, 2014], [Flores-Bahamonde *et al.*, 2014]. Sliding mode control, being another important variable frequency control scheme, has been adopted to realize LFR by the authors of [Cid-Pastor *et al.*, 2013]. The term Sliding mode based LFR (SLFR) was coined for the emulated LFR. The SLFR, discussed in above works, had been proposed for a PFC pre-regulator in a two-stage AC-DC-DC converters. Since the emulated resistance is a constant at all conditions, it can not cater to the varying load power demands and thus is not suitable for a single-stage AC-DC application.

The strategies discussed in the above section were for the PFC stage in a two-stage AC-DC-DC converters. In general it is difficult to apply the methods, used for PFC in two-stage AC-DC converter, to single-stage PFC converters as the PFC stage and DC-DC stage share the same power switch, unless the converter has multiple switches and is constructed differently such that it can control currents from the AC line and intermediate storage capacitor to flow into the converter in separate time slots within a switching period (e.g. [Lu *et al.*, 2008]). [Lu and Ki, 2012].

1.1.3 Control schemes for single-stage AC-DC Converter

The single-stage PFC configuration were introduced to reduce the cost and complexity of the two-stage AC-DC-DC converters. They are preferred for low/medium power devices, as all the power does not need to be processed twice, thus giving better efficiency. Additionally, reduced components and control circuitry favour their usage [Chen *et al.*, 2016]. The DC-DC and PFC units have the common control circuit and can also share the switches in this configuration. Amalgamating the PFC stage and DC-DC stage, causes a trade-off between the power-factor correction and dynamic performance. The common practice in single-stage converters is to allow the converter to operate in DCM mode to utilize its inherent current shaping. This scheme can easily be used in the single switching device-based converters (boost, buck-boost, *Ć*uk, SEPIC etc) when they are operated in DCM, which inherently provides an input current shaping and power-factor correction in single-stage conversion. Then a closed-loop control of output DC voltage to desired value is achieved using proportional-integral (PI) or proportional, integral and derivative (PID) or proportional-derivative (PD) or sliding mode controllers. However, DCM operation causes increased current stress, which not only accompanies increased switching losses and lower efficiency, but also EMI issues. Moreover, since the inductor current will operate in DCM, it cannot store any energy. This is because all the stored energy should be released by the end of the switching cycle, and a bulk capacitor should be used.

Generally, for the CCM operation, the control schemes consist of two loops, an inner fast

current loop and an outer slow voltage loop. In the literature considering single-stage active PFC, typically, a linear, two-loop PI controller is used to achieve the dual aim of PFC and voltage regulation. The inner control loop forces the input current to follow the sinusoidal supply voltage and the outer loop maintains the output voltage to its required value. The drawback of such conventional controller is the slow dynamic response [Nasirian *et al.*, 2013], [Fernandez *et al.*, 2005].

Soft-switching techniques were introduced to the single-stage PFC converters in an attempt to enhance the power density and efficiency. An auxiliary branch was added in parallel to the power switch to achieve Zero Voltage Transition (ZVT) at the turn ON [Rustom and Batarseh, 2001]. An adaptive switching frequency control technique is developed in [Wang and Tzou, 2012] to reduce switching losses and improve efficiency at light loads. In this a repetitive controller is designed to minimize periodic errors within the current loop bandwidth. A critical conduction mode (CRM) soft-switched buck PFC converter with constant on-time control is presented in [Wu *et al.*, 2011].

Whatever be the application of power converters, the idea has been to operate them in a way such that the resources (Grid AC or DC supply or Battery) are used efficiently. A similar efficient notion prevailed known as, the Event Triggered Control, for control implementation guaranteeing minimum resource usage and is discussed in the following section.

1.2 EVENT TRIGGERED CONTROL

Traditionally, for practical applications, the feedback controls developed are implemented on digital platform and are updated periodically every T (sampling time) unit of time. However, this periodic update of the control signal may not be required. Control tasks execution should be carried out whenever it is demanded [Anta and Tabuada, 2010]. Furthermore, the value of time period is chosen keeping in mind the worst-case scenario (to ensure performance at all possible operating conditions), and therefore the control action is carried out at the same rate irrespective of the system state. Thus, at nominal conditions, the periodic implementation of control tasks causes inefficient performance in terms of processor usage, energy, network bandwidth etc. For example, with regard to embedded systems, various tasks share the CPU time. Therefore, performing the control action even when the system states do not change much leads to a waste of computational resources. For the networked control systems, there is resource constraints not only in terms of the processor time but also in terms of the available communication bandwidth. Therefore, communication should occur only if there is a significant change in state compared to the previous state. This information is then required to be passed from the sensor to the controller and/or from the controller to the actuator. Periodic execution of control laws have been covered extensively in the existing literature, however, they might not always be the best solution, especially for nonlinear systems. Since, generally closed form nonlinear systems cannot be discretized exactly.

To get over the limitation of the periodic implementation, various researches ([Su *et al.*, 2017], [Zhang *et al.*, 2018], [Heemels *et al.*, 2008], [Tabuada, 2007]) advise the notion of event-triggered control. This notion suggests execution of control depending on the system state. This event-triggered scheme reduces resource usage and makes the system robust (as system states are continuously measured).

In the literature, event-based control is used with different terminologies. Although the triggering mechanisms are called event-based sampling [Arzén, 1999] or event-driven sampling [Heemels *et al.*, 2008], Lebesgue sampling [Åström and Bernhardsson, 2003], deadband sampling [Otanez *et al.*, 2002], asynchronous control [Heemels *et al.*, 1999], or level-crossing sampling [Kofman and Braslavsky, 2006], with slightly different meaning, all refer to the situation where the control action is not invoked by some clock but ''on demand'' by the control error or some other

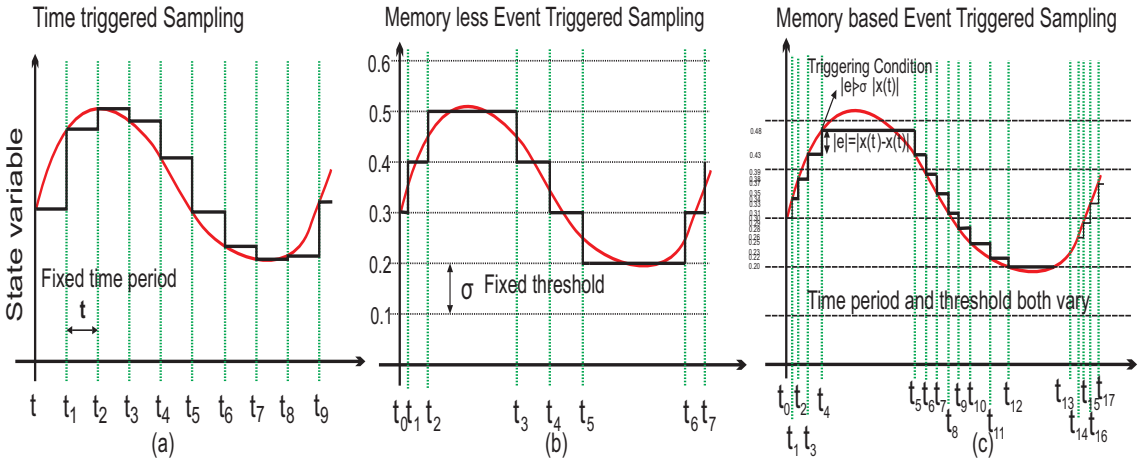


Figure 1.9 : Types of sampling. (a) Fixed time period and variable threshold, (b) Variable time period and fixed threshold, (c) Variable time period and variable threshold.

signal exceeding a certain threshold.

Lebesgue sampling occurs naturally in many context. A common case is in motion control where angles and positions are sensed by encoders that give a pulse whenever a position or an angle has changed by a specific amount. Lebesgue sampling is also a natural approach when actuators with on-off (switched) characteristic are used [Su *et al.*, 2018]. Recently event-triggered control has been implemented for various practical application systems, including current control of BLDC motors [Horvat *et al.*, 2013], PEM fuel cell air-feed system [Liu *et al.*, 2016], air-breathing hypersonic vehicles [An *et al.*, 2016], in nuclear plant [Fang and Xiong, 2014], in ocean wave energy plant [Mishra *et al.*, 2018] to name a few. Moreover, in modern distributed control systems it is difficult to stick to the time-triggered paradigm. This is specially the case with networked control system i.e. feedback systems that introduce varying communication delays [Wen *et al.*, 2015], [Cucuzzella *et al.*, 2019].

Traditional time-driven controllers are designed with a main focus on the performance of the controlled process. The aim of event-driven control is to create a better balance between this control performance and other system aspects (such as processor load, communication load, and system cost price). Co-designing the control law and event-triggering condition, with a view to establish a balance between performance and efficiency of the system, poses a crucial challenge. Various event triggering mechanisms have been proposed for ETC. Memory-less event-triggering [Heemels *et al.*, 2008] implies that, an event will be marked when the input variable exceeds a predetermined threshold. In memory based event-triggering [Lunze and Lehmann, 2010], when the difference between the current state and the stored state during the previously triggered event exceeds the threshold, then an event is triggered. Prediction method/Self-triggering suggests that the next sampling time is predicted by the measured state and system dynamics [Anta and Tabuada, 2010], [Behera and Bandyopadhyay, 2015]. The effect of the condition will be that controller will execute at the nominal sampling time during transients, i.e., set point changes and load disturbances, and that the controller will execute at the maximal sampling interval during steady state conditions. A pictorial representation of the relation between a state variable and its time triggered sampling, uniform memory less event triggered sampling and memory based event triggered sampling is presented in Fig. 1.9.

1.2.1 Concept of Event-triggered Control

Event-triggered strategy is essentially a need-based control technique where, instead of continuous/periodic update, the control is executed depending on the current state of the system [Tabuada, 2007]. The control signal is maintained to the previous value while the performance is satisfactory. It is modulated when a certain pre-defined constraint is breached i.e. an "event" occurs. An existing control, that makes the given system asymptotically stable, can be made event-triggered, provided it satisfies the pre-designed condition with appropriately chosen parameter.

To understand the concept, let us consider a system $\dot{\mathbf{x}} = f(\mathbf{x}, \mathbf{u})$ where $\mathbf{u}$ is the feedback control input $\mathbf{u} = \mathbf{K}(\mathbf{x})$ such that the closed loop system $\dot{\mathbf{x}} = f(\mathbf{x}, \mathbf{K}(\mathbf{x}))$ is asymptotically stable. Now, rather than updating this feedback control continuously or periodically, it is held to its previous value, i.e. for $t \in [t_i, t_{i+1})$ the control $\mathbf{K}(\mathbf{x}(t)) = \mathbf{K}(\mathbf{x}(t_i))$. This asynchronous control implementation induces error in the system, defined as $\mathbf{e}(t) = \mathbf{x}(t_i) - \mathbf{x}(t)$.

There exists an Input-to-State Stability (ISS) Lyapunov function $V(x)$ [Sontag, 2008] such that

$$\alpha_1||\mathbf{x}|| \leq V(\mathbf{x}) \leq \alpha_2||\mathbf{x}|| \tag{1.4}$$

and

$$\frac{\partial V}{\partial x} f(\mathbf{x}, \mathbf{K}(\mathbf{x}+\mathbf{e})) \leq -\alpha_3||\mathbf{x}|| + \gamma||\mathbf{e}|| \tag{1.5}$$

Where, α_1, α_2 and α_3 are class $-\kappa_\infty$, and γ is a class $-\kappa$ functions. In order to ensure the stability of the system with this input, which is being held until the next triggering instant, the following condition must be satisfied

$$\gamma||\mathbf{e}|| \leq \sigma\alpha_3||\mathbf{x}|| \tag{1.6}$$

Where, $\sigma \in (0, 1)$.
Then, using (1.5) and (1.6), the following equation is obtained.

$$\dot{V} \leq -(1-\sigma)\alpha_3||\mathbf{x}|| < 0. \tag{1.7}$$

Thus, the system is stable as long as (1.6) holds true. Since α_3^{-1} and γ are Lipschitz, (1.6) can be given as

$$||\mathbf{e}|| \leq \sigma L||\mathbf{x}|| \tag{1.8}$$

Where, L is an appropriate Lipschitz constant. The above equation is known as the Event-triggered condition, which generates the triggering instances guaranteeing to make the closed loop system asymptotically stable. That is, to say, the control input could be held as long as the above condition is satisfied.

Let (t_i), where $i \in [0, \infty)$, be the sequence of triggering instants at which the control is updated. This update time period is called inter-execution time, denoted as $T_i := t_{i+1} - t_i$, and is not constant. Higher value of σ ensures a longer time between updating of the control task at the expense of sluggish performance and precision. Therefore, σ is a design parameter capturing the trade-off between performance and execution frequency of control.

This strategy is a generic technique, applicable to any controlled systems, which are rendered stable through state-feedback. Various studies have been carried out on robust stability of linear and non-linear systems, controlled using various event-triggered state feedback controls viz. full state feedback, PID, H_∞, SMC etc. [Ferrara *et al.*, 2014], [Henningsson *et al.*, 2008], [Tabuada,

2007], [Su *et al.*, 2017], [Behera and Bandyopadhyay, 2016a], [Cucuzzella *et al.*, 2019]. The benefits of event based control have been well established using simulation and experiments.

The scheme was used with the Sliding mode control and was proposed and established as Event triggered SMC (ETSMC) by Behera and Bandyopadhyay in [Behera and Bandyopadhyay, 2016a], [Behera and Bandyopadhyay, 2016b]. As mentioned earlier, this event based control is a natural approach when actuators with ON-OFF characteristic are used. This motivated the work carried out in the presented thesis to implement Event-triggered control for the efficiency improvement of power converters, while maintaining the required performance. This is the the first work to implement event-triggered control for power converter applications. The Sliding mode control and Event-triggered sliding mode control are briefly discussed in the following sections.

1.3 SLIDING MODE CONTROL

The concept of sliding mode control is widely adopted as it makes the system invariant to parametric variations and disturbances [Utkin and Shi, 1996]. Owing to these attributes, the SMC control has received due attention within the control community since late 70s.

The design of SMC requires two important steps, namely, (a) Switching function (s) design: A stable sliding surface for $s = 0$ and the corresponding system motion, when $s = 0$, is known as sliding mode (b) Control law design: Control causes system to reach the sliding mode in finite time. In the SMC approach, The system trajectories are forced to move, from the initial point, towards the designed sliding surface. This phase is known as the reaching-phase. Once the trajectories reach the surface, the system is said to be under sliding mode. During this phase, the system states move along the switching surface and converge to operating point. The attraction and movement of system states from the initial condition towards the sliding surface ensure that the sliding mode exists, for this to happen the existence condition must hold, which is given as

$$s\dot{s} \leq \eta |s| \tag{1.9}$$

Here, $\eta$is a positive number.

Once the states reach the surface, in order to make them converge to the operating point, the stability of the sliding mode must be ensured. Lyapunov stability is one of the approaches to investigate the stability. The readers are encouraged to read the details found in excellent text on the subject [Edwards and Spurgeon, 1998], [Utkin, 1978]. It is observed that during reaching phase, the system dynamics are sensitive to the parameter variations and disturbance. However, during the sliding mode system becomes invariant to the matched disturbances entering in the system. The concept of SMC is shown in Fig. 1.10.

1.4 EVENT-TRIGGERED SLIDING MODE CONTROL

The work proposes to implement the classical SMC as event-triggered SMC, for power converter application. This section discusses the methodology briefly.

Ideally, in order to maintain the state trajectory on the sliding surface, SMC requires infinite switching. However, real-time discrete implementation of this control makes the above demand not achievable, owing to the limitation on control update by the sampling frequency. Consequently, the trajectories deviate from the sliding manifold until the updated control steers them back. Nevertheless, the trajectories remain bounded within a band, called quasi sliding mode band, dependent on sampling frequency and disturbance bound. This phenomenon is also called practical sliding mode. Owing to the similar argumentation, the trajectories move away from the

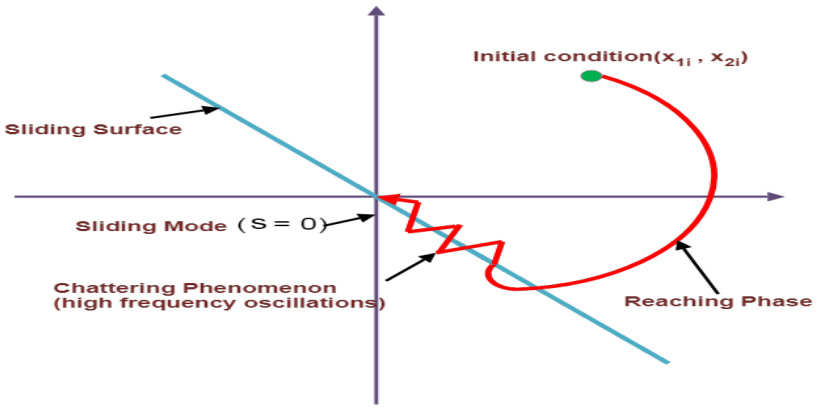


Figure 1.10 : Concept of Sliding mode control

sliding manifold in event-triggered implementation also. However, the trajectories remain within a bound.

Employing event-triggered control law requires constant monitoring of the state, although the control is not invoked until the evolution of system trajectories violates a predefined constraint. The basic idea of event triggering scheme is to hold the input control constant for a time interval between two consecutive events, i.e. for $t \in [t_i, t_{i+1})$

$$\begin{aligned} u(t) &= u(t_i) \\ &= \frac{1}{2}[1 - \text{sign}(s(t_i)] \end{aligned} \tag{1.10}$$

Event-triggered control mimics the behavior of the original periodically implemented control. Thereby, similar to classical SMC, practical application of the event-triggered SMC also needs to fulfil the following conditions.

- The event-triggered SMC drives the system trajectories to the sliding manifold and keeps them within a band from there on.
- Once the system trajectories enter the band, the stability of the closed loop system is ensured.
- No Zeno execution: Consecutive triggering instants generated, as a result of the rule, do not accumulate i.e. they are separated by a finite time.

1.5 INTERGAL SLIDING MODE CONTROL (ISMC)

As discussed in above sections, Sliding mode control (SMC) forms an inherent choice as non-linear control, for converters. SMC offers a robust performance with respect to matched perturbations, under sliding mode. However, in the reaching phase the system is sensitive to the disturbances. ISMC eliminates this reaching phase of conventional SMC and thus makes the system robust throughout. Moreover, ISMC combines the non-linear SMC with the existing linear control strategies like PI controller, LQR etc. which have been developed owing to their ease of design and analysis. These classical linear controls are designed and optimized to make the system perform well around its nominal operating point, however, when subjected to large transients, they compromise on system performance. Thus, non-linear control approaches are better choice

in these systems. Hence, the ISM based control approach is used which leverage benefits of both classical linear controller and sliding mode control. ISM control eliminates the reaching phase in SMC and thus compensates for matched disturbances entering into the system from the very beginning [Rubagotti *et al.*, 2011]. However, the system dynamics are governed by nominal controller. Therefore, the overall performance of the system improves using the overall control input which combines the control inputs of nominal controller and ISM controller.

To understand the principle of ISMC, consider a dynamic model of a system with uncertainty as,

$$\dot{x} = Ax + Bu + \phi \tag{1.11}$$

Here x is the state-vector, $A \in \mathbb{R}^{nxn}$ is the system matrix, $B \in \mathbb{R}^{nxm}$ is the input matrix. It is assumed that the matrix B has full rank, i.e. $rank(B) = m$ and the pair (A,B) is controllable. The function ϕ represents a matched uncertainty which is unknown but has a known upper bound for all x and t, say λ. Since it is a matched uncertainty therefore $\phi = B\phi_m$ Therefore, (1.11) can be written as,

$$\dot{x} = Ax + Bu + B\phi_m \tag{1.12}$$

Let $u = u_o$ be a nominal control designed for (1.11) assuming $\phi_m = 0$, wherein u is designed to achieve a desired task, whether it be stabilization, tracking, or an optimal control problem. Thus, the trajectories of the ideal system ($\phi_m = 0$) will be given by the solutions of the following ODE equations:

$$\dot{x}_o = Ax_o + Bu_o \tag{1.13}$$

Thus, for $x(0) = x_o(0)$ and ϕ_m being not equal to zero, the trajectories of (1.11) and (1.13) are different. The trajectories of (1.13) satisfy some specified requirements, whereas the trajectories of (1.11) might have a quite different performance (depending on ϕ_m) to the one expected by the control designer. Now the control design problem is to design a control law that, provided that $x(0) = x_o(0)$, guarantees the identity $x(t) = x_o(t)$ for all $t \geq 0$. Thus, the control objective can be reformulated in the following terms: design the control $u = u(t)$ in the following form:
$u(t) = u_0(t) + u_n(t)$

where, $u_o(t)$ is the nominal control part designed for (1.13) and $u_n(t)$ is the integral sliding mode (ISM) control part guaranteeing the compensation of the unmeasured matched uncertainty ϕ_m, starting from the beginning ($t = 0$). Now, the first step, in design of ISM, is to design a sliding surface. Suppose s is the switching function given by,

$$s(x,t) = G[x(t) - x(0) - \int_0^\tau \{Ax(\tau)) + Bu_o(x(\tau))\}d\tau] \tag{1.14}$$

Here, $G \in \mathbb{R}^{mxn}$ is a full rank matrix to be designed such that $det(GB) \neq 0$.

Now, in order to ensure stable sliding mode and its robustness towards the uncertainty ϕ_m, consider derivative of s as,

$$\dot{s} = GB(u_n + \phi_m) \tag{1.15}$$

where, the square matrix GB is non-singular by design. It is to be assumed that the system states have reached the sliding surface and will stay there from then on i.e. $s = \dot{s} = 0$. The control signal ensuring the existence of sliding mode can be obtained by solving $\dot{s} = 0$, for u.

$$u_{eq} = -\phi_m \tag{1.16}$$

The term u_{eq} is the equivalent control, for the actual discontinuous control law, used as an average value for analysis purposes. This implies the matched uncertainty is eliminated and the sliding motion is governed by the nominal control given by

$$\dot{x}(t) = Ax + Bu_o(t) \tag{1.17}$$

1.6 MOTIVATION AND RESEARCH OBJECTIVES

Previous sections, in the Chapter, have discussed several compensation techniques to reduce the switching losses in a power converters at low load. By altering switching frequency, based on the current status of the system, the efficiency and performance of the converter could be retained for the entire range of operating conditions. In line with the above aim, various load adaptive schemes have been developed, over the time, to amend power delivery to different load demands. The adaptive quality is achieved by dynamically adjusting the control or/and by adjusting the hardware structure of the converter.

The electronic market is amongst the largest and fastest growing manufacturing industry across the globe, with computer systems and consumer electronics making about 40% of the total production. These devices demand power and their large scale proliferation in commercial and household environments raises concerns regarding Energy efficiency and Grid power quality. Multiple non-governmental and governmental bodies around the world have put in place standards and regulations to deal with these issues. Energy Star is an Environmental Protection Agency (EPA) voluntary program in which companies comply with the standards set by the EPA. This guarantees that the product meets certain requirements for energy efficiency and power quality.
The frond end circuitry for these electronic equipment consists of an AC-DC stage and a DC-DC stage as shown in Fig. 1.11.

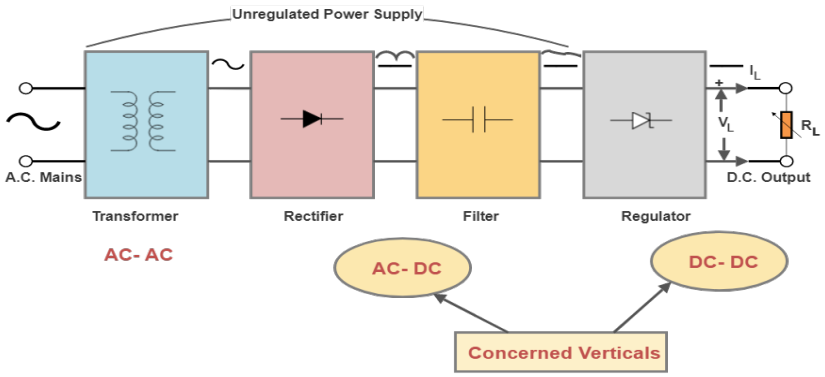


Figure 1.11 : Front end circuitry of a typical electronic equipment.

The power converter used for power factor correction in the AC-DC stage ensures power grid quality (by limiting the harmonic currents) and the DC-DC stage is used to regulate the DC bus voltage. With an aim to maximize the use of resources and to abide by the regulation imposed, various control algorithms have been developed in the past. Some of these techniques, developed lately, involve Adaptive Frequency-optimization (AFO) controller, which tracks maximum efficiency point corresponding to minimum input current and causes step changes in frequency. However, it does not accommodate fast load transients. Constant On/Off PWM technique increases switching frequency dynamically under heavy/light load conditions as the control shifts

between constant on and off-time control, depending on the load current. Variable frequency modulation with both on and off time as control inputs, provides an improved transient performance. But the method requires an accurate model of the converter dynamics, and designing and implementing a multi-loop controller. Adaptive FET modulation scheme uses multiple Field Effect Transistors (FET), with different characteristics, applied in parallel such that driven FETs and their gate driving voltage are adaptive to load current. Howbeit, the cost involved with additional circuitry makes the overall system to be a costly pursuit. Sliding mode control is an inherent choice for power converters, however it suffers with the phenomenon of chattering. Hysteresis mode based SMC is used to suppress this high frequency oscillations by providing a band around the switching surface, however, this band is designed for the worst case scenario and is kept fixed at all operating conditions. Moreover, these control algorithms are usually implemented over digital platform using time-triggered scheme. The periodic sampling of the control law may cause a critical piece of information be lost if it falls between the two triggering instants. Therefore, an event-triggered implementation of control law is needed.

The main objective of this research work is to leverage system dynamics in order to improve efficiency of the power converters using non-linear control techniques. Event-triggered implementation provides better balance between this control performance and system efficiency. The fundamental concept of this scheme is that the control tasks must be executed when something "significant" happens in the process to be controlled i.e. only when it is required to update control law. This generic strategy makes an existing well-established control algorithm, load adaptive by changing the way it gets implemented. Thus the event-triggered phenomenon is a natural choice for applications where such aperiodic execution is natural and the control signal is in form of a positive or negative pulse of given size. This became the motivation for proposing Event-triggered Sliding mode control for power converters. Executing control only "on-demand", limits the control execution thus avoiding unnecessary switching actions, while maintaining the performance. The work causes a paradigm shift from development to implementation of control strategy vis-a-vis conventional techniques. Sliding mode control provides robustness against large line-load transients, when operating under sliding mode. However, it remains susceptible to disturbance in reaching phase. The Integral sliding mode control eliminates this reaching phase and ensures sliding mode from the initial point, thus making system invariant to disturbances/uncertainties entering through the input channel.

The Event-triggered Sliding mode controller is proposed for efficiency improvement in the DC-DC voltage regulation stage and also in the AC-DC harmonics-free rectification stage. A novel concept of adaptive sliding mode based loss free resistor (ASLFR) is also proposed to maintain the output voltage as well as maintain grid quality, at all operating conditions and is later implemented using event-triggered scheme. Another non-linear controller Integral Sliding mode control (ISMC) is also proposed for power factor correction with a dual-loop PI controller (nominal control). It improves the performance of the nominal controller by eliminating the matched uncertainty from the beginning of the system response. Moreover, it is also able to compensate for the parametric perturbations. This aspect of ISM, of being able to maintain the system performance even under system parameter variation, has also been explored with Z source converters. The controllers are verified through a detailed experimentation and simulation studies. Here is the brief of the contributory work in the Thesis.

In the First work, a novel event-based control implementation technique for power converters has been proposed and analysed to serve twin objectives of providing load-adaptive feature to the system and reducing the excess switching losses. The proposed scheme exploits the state dynamics to update the control action, thereby reducing switching actions in exchange for a user acceptable performance, and hence, maintaining the efficiency as well as the required performance over the wide load range. The expediency of the strategy has been analysed in general. Moreover,

HM-SMC is established as a special case of ETSMC mathematically. HM-SMC could be emulated using memory less event-triggered scheme, in which the triggering condition is independent of the system dynamics, thus providing a fixed boundary around the switching surface. Using ETSMC, load adaptive frequency modulation occurs very naturally unlike the existing variable frequency schemes, which involve sudden mode hopping between different control/algorithm, moreover detecting the exact moment of hopping is complicated. Furthermore, ETSMC does not require any change in the hardware of the system for implementation. The proposed theory is demonstrated and validated through simulation and experimentation over a half-bridge isolated converter. Experimental results clearly exhibit and confirm the accuracy and effectiveness of the proposal. The improvement in efficiency using the proposed scheme is reported graphically.

Generally electronic equipment employ a full-bridge rectifier at the front-end of power supplies to convert utility AC into specific DC level. Being non-linear loads, the rectifiers distort the current drawn from the grid raising concerns over grid pollution. Regulatory measures like IEC 61000-3-2 Harmonics Standards by European Union, for these devices, have been imposed to maintain the grid quality. These regulations categorized appliances up to 600W as Class D. The current limits for them are expressed in terms of mA /Watt. Various control schemes have been developed to make the current waveform meet the regulatory standards. One of the most significant control scheme is Hysteresis control; however this control keeps the current to stay within a fixed band which stays the same at all loads, even though the regulatory rules provides flexibility of increased allowable harmonic content with the load, thus causing unnecessary switching and thus associated switching losses. The Second work of the thesis extended the proposed Event-triggered Sliding mode control strategy for the power factor correction application. This control adapts the band with load in order to maintain the current within the varying limit at the same time reducing the switching losses.

The SLFR addressed in the previous work was pre-defined constant and thus could be applied only for input current shaping application. Therefore, there was a need to introduce an adaptive emulated resistance such that it dynamically changes with the operating conditions, in order to serve the dual purpose of current shaping as well as voltage regulation. In the Third work, a novel notion of Adaptive Sliding mode based loss free resistor (ASLFR) is proposed. The scheme serves itself as an efficient single-stage PFC solution wherein the two stages of voltage regulation and PFC, dealt separately in first and second work, are combined. This is achieved by allowing the emulated loss free resistor to adapt itself to accommodate the load demands. ASLFR is used to achieve the dual purpose of harmonics-free rectification along with excellent system response under load and line transients. The work is implemented for a single phase boost PFC commonly used for low/medium power electronic equipment under consideration. A collection of simulation results are provided to validate the effectiveness of the adopted novel scheme over the existing SLFR based controller and the most commonly adopted dual-loop PI control for single-stage PFC solution.

All high power equipment derive power from three-phase mains. In the fourth work, the proposed sliding mode based strategy to emulate loss free resistor for modular three-phase AC-DC rectification using three isolated single-phase Ćuk converters, operating in CCM, is presented. The AC input sides of three modules are Y-connected, and their DC output sides are connected in parallel. The proposed converters were independently controlled to achieve the dual aim of power factor correction (for all phases) and output voltage regulation. In the experimentation, the expediency of the proposed control is verified for various operating conditions.

The classical control methodologies such as PID, optimal control are largely researched for power factor correction in the two-stage AC-DC-DC converters. However, such control methodologies ensure stability close to the operating point only. Moreover, in practical applications, the

disturbances and uncertainty are involved which perturb the desired operation of the linear controllers. The non-linear controls e.g. SMC are generally preferred to ensure the robustness against the disturbances/uncertainty and the stability at the large line-load transients. However, SMC has finite reaching phase during which system is not invariant to noise. To avail the advantages of classical and modern control methods, there is a need of control methodologies which ensures harmonics reduction problem along with desired dynamic performance and ensure stability and robustness. The integral sliding mode control is one of the desired control approaches. The integral sliding mode control (ISMC) ensures the robustness against the disturbances/ uncertainty from the beginning of the system response and allows the classical control methodologies to combine with the sliding mode control.

In the fifth work, an ISM based controller has been proposed for power factor correction. In this work, a dual loop PI-controller (nominal controller) amalgamates with ISM controller. ISMC improves the performance of the nominal controller by ensuring invariance against the matched uncertainty from the beginning of the system response. Moreover, it is also able to compensate for the variation in system parameters from their nominal values. This aspect of ISM, of being able to maintain the system performance even under system parameter variation, motivated the next work on Z-source converters. Nominal linear control, designed using the reduced order Z-source converter model, are able to perform well, provided the assumed symmetry in the system is maintained. This is done for the ease of analysis and reduced complexities in controller design. Nonetheless, this symmetry in the Z-source network is an ideal case because duplicating two elements is infeasible. The proposed non-linear ISM controller mitigates this uncertainty in parameters if they lie in the matched space of the input and is able to maintain the system performance despite the non-ideality.

The major contributions of the Thesis can be listed as:

- This work is the first one to use Event-triggered Sliding mode Control (ETSMC) in order to improve low load efficiency in power converters.
- The proposed scheme is generic in nature and HM-SMC is presented as a special case of ETSMC with memory less event-triggered mechanism.
- The effectiveness of the ETSMC has been verified for PFC and DC-DC stages of a two-stage AC-DC-DC converter.
- A novel concept of Adaptive Sliding mode based Loss free resistor has been proposed for single-stage AC-DC converter, and has been explored for single-phase as well as three-phase application.
- This work also proposes the concept of Integral Sliding mode Control (ISMC) for PFC application. It makes the system robust from the starting point by eliminating the reaching phase associated with Classical SMC.
- The concept of ISMC has further been proposed, for the first time, for Z-source converters. ISMC mitigates the effect of parametric asymmetry on system performance during practical applications of ZSC. Hence a reduced order model can suffice for control design.
- A comprehensive analytical as well as experimental validation of the proposed schemes is given.

The organization of the thesis is presented in the next section.

1.7 ORGANIZATION OF THESIS

The Thesis is organized in the seven Chapters and the content of the each Chapter is briefly discussed here,

Chapter First: This Chapter presents an introduction of the stooping efficiency due to switching losses, especially at low loads, in the power converter. The Chapter covers a comprehensive literature review based on the existing methods and techniques to achieve a flatter efficiency curve at all operating conditions. It also presents the main objective, motivation and organization of the Thesis.

Chapter Second: This Chapter presents the Event-triggered Sliding mode control for low-load efficiency improvement in DC-DC voltage regulation stage. In this Chapter, complete mathematical proof of the proposed control is established. Furthermore, Hysteresis modulation based SMC (HM-SMC) is established as a special case of ETSMC, thus highlighting the proposed scheme's generic nature. The scheme is demonstrated on an isolated half-bridge converter.

Chapter Third: This Chapter presents the proposed ETSMC for power factor application. The control is implemented over a Boost PFC working as a pre-regulator stage in AC-DC-DC converter. The input current wave shaping is done within an adaptive boundary layer, to avoid unnecessary switching. The performance analysis of the presented control is presented over the HM-SMC.

Chapter Fourth: This Chapter presents a novel concept of adaptive sliding mode based loss free resistor for a single-phase single-stage Boost PFC operating in CCM. Furthermore, the presented control is implemented in an event-triggered fashion. A comparative study is made with the existing methodologies and the expediency of the presented control is established.

Chapter Fifth: This Chapter carries forward the concept of ASLFR for a three-phase application. It is implemented for a modular three-phase power factor correction circuit (PFC) using three isolated single-phase Ćuk converters, operating in CCM. Complete analysis is done and the relevant simulation as well as experimental results are presented.

Chapter Sixth:ISM based controller for the boost PFC is presented to provide harmonics-free rectification. A dual-loop PI controllers scheme is used as the nominal controller of the ISMC. The performance analysis of the PI controllers based dual-loop control method over the proposed ISMC is presented. Moreover, the robustness of the proposed ISM based controller against the disturbances and uncertainty in the system is investigated. This Chapter further explores the robustness against system parameter variation due to ISMC for Z-source converters. Firstly, a study on a reduced model of Z-source converter and effect of parameter variation is made. Secondly, ISMC was extended to mitigate the effect of asymmetry in Z-source caused by parametric variations. The control is verified through simulation using MATLAB-Simulink.

Chapter Seventh: This Chapter concludes and discusses the major contributions of the Thesis. The chapter also presents recommendations for the future research.

1.8 PUBLICATIONS

1. N. Rathore, D. M. Fulwani, A. K. Rathore and A. R. Gautam "Adaptive Sliding mode based Loss Free resistor for Power Factor Correction Application," in IEEE Transactions on Industry Applications (2019). doi: 10.1109/TIA.2019.2912799

2. N. Rathore, D. M. Fulwani, and A. K. Rathore "Event-triggered Sliding Mode Control for light load efficiency improvement in Power Converters," in Control Engineering Practice (Under Review)

3. A. R. Gautam, Rammohan R. Makineni, D. M. Fulwani, and N. Rathore "ISMC for Boost-derived DC-DC-AC Converter: Mitigation of 2ω−Ripple and Uncertainty, and Improvement in Dynamic Performance", IEEE Transactions on Power Electronics (Conditionally Accepted-mandatory major changes requested)

4. N. Rathore, S. Gangavarapu, A. K. Rathore, and D. M. Fulwani, "Loss free resistor emulation for Single-stage Three-Phase PFC converter using Single-phase Ćuk modules" (Under preparation)

5. N. Rathore, and D. M. Fulwani "Event triggered control scheme for power converters" IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1342-1347. doi: 10.1109/IECON.2016.7794129

6. N. Rathore, A. R. Gautam and D. Fulwani, "Adaptive Sliding mode based Loss Free resistor for Power Factor Correction Application," 2018 IEEE Industry Applications Society Annual Meeting (IAS), Portland, OR, USA, 2018, pp. 1-6. doi: 10.1109/IAS.2018.8544659

7. N. Rathore, S. Gangavarapu, A. K. Rathore, and D. M. Fulwani, "Loss free resistor emulation for Single stage Three-Phase PFC converter using Single-phase Ćuk modules," IFEEC 2019 - 4th IEEE International Future Energy Electronics Conference, Singapore. (Accepted)