5

Adaptive Sliding mode based Loss-free Resistor for a single stage three-phase modular PFC application

In the previous Chapter, a novel notion of Adaptive Sliding mode based Loss-free Resistor (ASLFR) was proposed for single-stage, single-phase power factor correction application. Then on, event-triggered implementation of the adopted ASLFR was proposed. The aforementioned work was been analysed for single-phase low/medium power electronic equipment falling into the Class D category as per IEC 61000-3-2:2014 guidelines [IECLimits, 2014]. However, almost all high powered loads require three-phase supply. They, being non-linear loads, while drawing current from the mains, pollute the grid. Therefore, three-phase PFC converters are needed at the front-end of such equipments.

In order to prevent harmonics from negatively affecting the utility supply, in Europe and United Kingdom, harmonic distortion levels from chargers are subjected to IEC regulations [IECLimits, 2014]. This standard categorizes the home appliances into four different classes and provides guidance for limitations of harmonic currents from various electric equipment. The details had been discussed in Chapter 3. Class A covers balanced three-phase equipment, household appliances, ballast dimmers, audio equipment and other equipment not covered under Class B-D.

To be a feasible solution, the equipment must satisfy the grid code in terms of total harmonic distortion (THD) from the utility side. The regulations do not ask for a perfect sinusoidal input current waveform but just for a limited harmonic content. This flexibility allows many new different options to meet the regulations, broadly categorized as Passive and Active. Active solutions can, then, be classified into two main groups: 1) single-stage solutions and 2) two-stage solutions. The industry-standard approach to power-factor-corrected AC-DC rectification is to use a two-stage power converter. They consist of two converters connected in cascade. The first converter operates as a resistor emulator, and the current it drives from the mains is almost a perfect sinusoid. The second converter is a conventional DC-DC converter with fast output voltage regulation. For example, EV battery chargers have utilized a two-stage converter featuring a boost pre-regulator and a full-bridge resonant converter [Hayes *et al.*, 1999], [Musavi *et al.*, 2011]. However, due to the two processing stages, conversion efficiency is reduced and an extra PFC stage adds components and complexity.

While two-stage approaches to PFC and regulation have proliferated, the power supply industry has shown interest in developing single-stage solutions with the desire to reduce the parts count and cost of the conversion stages [Li *et al.*, 2016], [Lee *et al.*, 2008], [Azazi *et al.*, 2018]. Generally, the input current is not perfectly sinusoidal. Nevertheless, only a small part of the input power is processed twice, and hence, efficiency is typically very high, and the size is small in comparison with the two-stage converter. Similar trends exist in the automotive industry, where performance and cost must be continually optimized and, if necessary, traded off. Hence, the interest is in high-power-factor topologies, which maximize power delivery while addressing component count and cost [Egan *et al.*, 2007].

The three-phase PFC converters can then further be classified as: Direct three-phase sys-

tems and Phase-modular systems. The conventional three-phase, CCM, six-switch PWM boost or buck-type converters, are used for high power application and while capable of giving improved current quality, they have more component counts and a complicated controller design that causes poor reliability [Ayyanar *et al.*, 2000], [Umamaheswari *et al.*, 2013]. Under three-phase topologies, the approach of paralleling single-phase converter units to form high-power, single stage three-phase converter has become quite popular [Savage *et al.*, 2014], [Kisacikoglu, 2018], [Yoo *et al.*, 2012], [Kamnarn and Chunkag, 2006], [Huang *et al.*, 2012]. The output stages of three single-phase PFC modules are made in parallel. It owes the popularity to advantages which involve great flexibility in developing power converter for different power levels, easier maintenance, and also standard single-phase converter units do not require high-voltage devices that are normally needed in specially designed three-phase converters.

Usage of modular single-phase non-isolated PFC circuits for three-phase rectification is discussed in reference [Spiazzi and Lee, 1997]. The main problem faced in using non-isolated modules is the interaction among the three phases. Resolving this issue requires the use of additional circuit techniques such as split inductors and split free-wheeling diodes. This issue can also be addressed using isolated single-phase PFC modules. These isolated modules, in addition to solving the interaction problem, also eliminates use of an additional DC-DC converter stage, otherwise required in non-isolated topologies. Buck-boost derived converters like Ćuk, flyback and SEPIC are attractive for PFC application because they provide ease in implementing isolation, achieving desirable voltages and limiting in rush current during start-up and overload conditions. Three-phase AC/DC converter using three single-phase isolated Ćuk rectifier was proposed in [Kamnarn and Chunkag, 2009], [Bhuvaneswari *et al.*, 2012], [Umamaheswari *et al.*, 2013].

The modular three phase isolated Ćuk converter, operating in CCM, was proposed in [Kamnarn and Chunkag, 2009] for telecommunication application. It well establishes the expediency of Ćuk converters for PFC applications. The referred work uses PI controller with power balance control technique, for improved power factor at heavy load conditions. In order to improve dynamic response in the DC voltage control, load current is also sensed and added to the inductor current amplitude reference as load feed-forward. Moreover, the referred work operates even under module loss and provides good voltage regulation dynamics, however, the current quality degrades at lower loads (a comparison between the referred work and the proposed work is presented in later section).

In this Chapter, the concept of Adaptive sliding mode based loss free resistor (ASLFR), which was proposed for single phase, Class D converters in Chapter 4, is proposed for the modular three-phase PFC application using Ćuk converters. This work is carried out to provide an alternative for three-phase, single-stage PFC for high power Class A equipment The adopted topology and control employ six sensors for a balanced three-phase CCM operation, enabling harmonics-free rectification and regulated output voltage, in a single-stage. This eliminates the need of an additional converter stage while fulfilling the IEC 61000-3-2 (Class A) requirements. Use of the proposed controller will emulate the entire equivalent circuit for each of the module as a loss-less resistor, thus allowing each of the phase current to follow the phase voltage. The adaptive nature of the controller will ensure the power factor correction for a wide range of line and load conditions.

The rest of the Chapter is organized as follows. Section 5.1 provides the system description and design of a single Ćuk module. The concept of the proposed ASLFR is discussed in Section 5.2 while the in-depth stability analysis for the controller is covered in Section 5.3. Section 5.4 and 5.5 present the simulation and experimental results respectively. Summary of the Chapter is provided in Section 5.6.

5.1 SYSTEM DESCRIPTION

A three-phase converter using three single-phase, single-switch modular rectifier topology has the merits of simple control, few components and ease of maintenance. The proposed system comprises of three Ćuk rectifier modules as shown in Fig. 5.1. Ćuk converter is a cascade combination of boost converter at its input side, and buck converter at the output side. These three single-phase modules are connected in Y- connection with the neutral at the input and in parallel at the output side [Kamnarn and Chunkag, 2009]. The configured converters work in CCM, to deliver a fixed voltage at the output. Running the circuit in DCM results in small inductor size and simpler control, however, the penalty is higher current stress, higher conduction loss and reduced efficiency. Thereby, CCM operation is required for high power application.

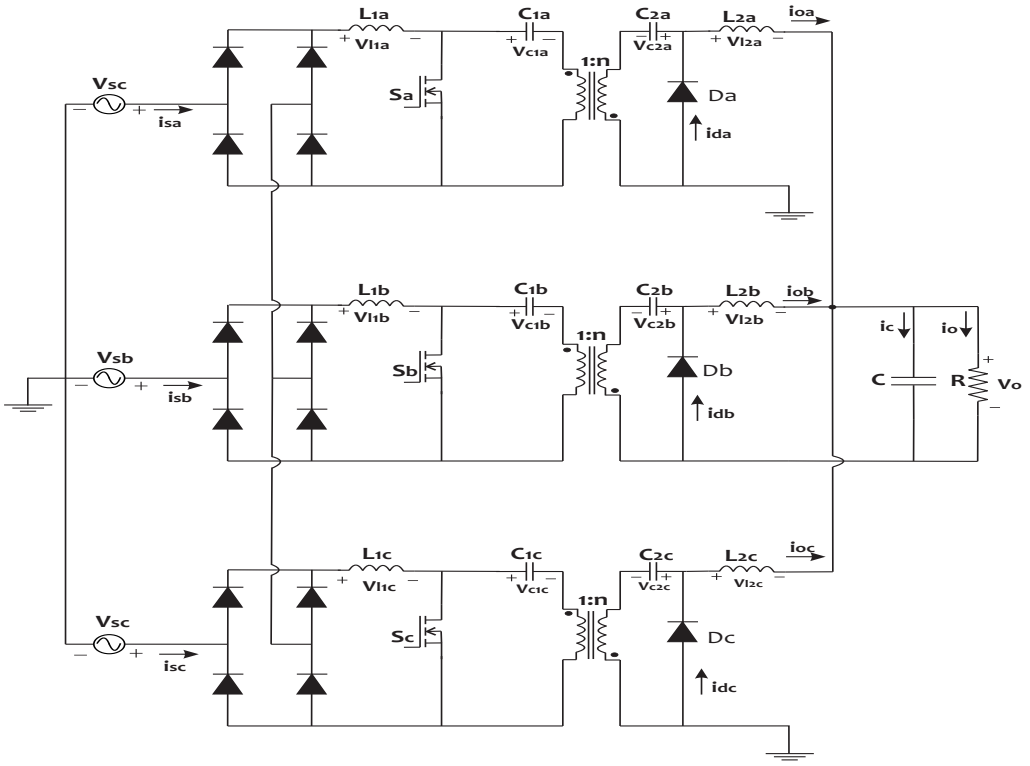

Figure 5.1 : Power circuit of the modular three-phase ac-dc converter using Ćuk rectifier modules.

As shown in Fig. 5.1, the bridge rectifier at the front end is fed by an AC voltage supply V_s and at the other end, a Ćuk converter is connected. Each module consists of two inductors L_1, L_2 and two capacitors C_1, C_2. The output of the three modules are connected in parallel to DC-link capacitor C_o and feed i_o to load .

5.1.1 System Dynamics

The circuit of the equivalent non-isolated, single-phase module from the three-phase PFC Ćuk converter is presented in Fig. 5.2. It consists of two inductors L_1, L_2' and two capacitors C_{in}, C_o. The output inductor L_2, transferred to the primary side becomes, $L_2' = \frac{L_2}{n^2}$, and $C_{in} = \frac{C_1 C_2'}{C_1 + C_2'}$, where $C_2' = n^2 C_2$ The output voltage is represented as V_o/n, S is an active switch, D is a freewheeling diode. As, the phases are balanced, the output current of a single phase is one-third of the total output load current. The converter dynamics is described by state-space averaging method and by using

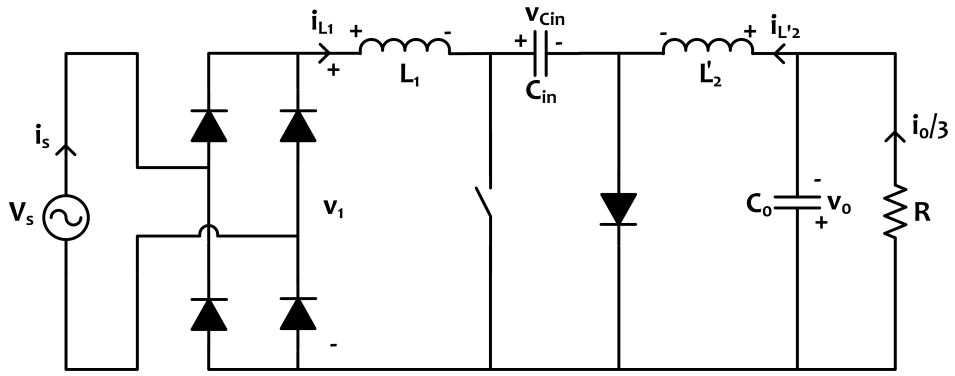

Figure 5.2 : Equivalent circuit of the isolated PFC based Ćuk converter when referred to the primary side

the same method, the state equations during switch-on and switch-off conditions are combined as:

$$\dot{x_1} = \frac{-x_3}{L_1}(1-u) + \frac{v_1}{L_1} \tag{5.1a}$$

$$\dot{x_2} = \frac{x_3}{L'_2}u - \frac{x_4}{L'_2} \tag{5.1b}$$

$$\dot{x_3} = \frac{-x_2}{C_{in}}u + \frac{x_1}{C_{in}}(1-u) \tag{5.1c}$$

$$\dot{x_4} = \frac{x_2}{C_o} - \frac{x_4}{3RC_o} \tag{5.1d}$$

Where, transformer ratio, n, is taken as 1. v_1 is the rectified input voltage. x_1, x_2, x_3, x_4 are the current through the input inductor (i_{L1}), current through the output inductor ($i_{L'2}$), voltage across the transfer capacitor (v_{Cin}), and voltage across the output capacitor (v_o), respectively. u is the control input. The design procedure of system parameters, to achieve the continuous conduction operation mode, is discussed in the following subsection.

5.1.2 Design for CCM operation

Design specifications for the converter operating in CCM are tabulated in Table 5.1

Table 5.1 : System specification and parameters

Parameter	Value
Input Phase Voltage V_s	120 V, 60Hz
Output Voltage V_{ref}	400 V
Total Output Power P_o	1000W
Transformer Ratio n	1:1

The condition to operate the converter in CCM is derived as follows

- The DC voltage conversion ratio $m(\theta) = \frac{V_o}{V_s|sin(\theta)|}$, the M ratio is

$$M = \frac{V_o}{V_s} = 2.357 \tag{5.2}$$

- The critical value of conduction parameter for this converter is ([Gangavarapu *et al.*, 2018])

$$k_{a,crit} = \frac{3}{2}\frac{1}{(n+M)^2} = 0.133 \tag{5.3}$$

where, $n = 1$.

- For CCM, $k_a > k_{a,crit}$. Hence, the conduction parameter k_a is chosen as 0.266.

- The equivalent inductance is

$$L_{eq} = \frac{RT_sK_a}{2} = 0.532mH \tag{5.4}$$

The design of L_1 is carried out using the desired ripple in the input current.

$$L_1 = \frac{V_s}{\Delta I_s} dT_s \tag{5.5}$$

The inductor L_1 of size $2.15mH$ is chosen.
The output inductor

$$L_2' = \frac{L_1 Leq}{L_1 - L_{eq}} \tag{5.6}$$

where, $L_{eq} = \frac{RT_sk_a}{2}$. Hence $L_2 = 707\mu H$.

5.2 PROPOSED CONTROL SCHEME

An adaptive sliding mode based LFR was proposed in Chapter 4. The controller emulates a loss-free resistor (r), which dynamically adapts, for a wide range of operating conditions, thus allowing power factor correction at different line and load conditions. This Chapter extends the proposed theory for a three-phase converter, and a comprehensive analysis is carried out in this section.
As described in [Singer and Erickson, 1992], an ideal loss-free resistor (LFR) is a two-port switching structure which satisfies two basic conditions of current proportionality and power balance.

- The input current is following the input voltage.
  $V_{in} = rI_{in}$

- The input power absorbed is completely fed to the output. $V_{in}I_{in} = V_{out}I_{out}$

Where, V_{in}, I_{in}, V_{out}, and I_{out} are the averaged equilibrium values of the variables. The proportionality constant r is the input resistive impedance that the circuit presents itself as, under steady state.

A three-phase converter, made using three single-phase modules, is considered as shown in Fig. 5.1. For a three phase balanced converter the power equation becomes

$$P_a + P_b + P_c = P_o \tag{5.7}$$

Where, P_a, P_b, P_c are the power outputs of the modules connected with phase A, B, and C respectively.

Since a symmetric, balanced system is considered each module works independently and delivers equal amount of power $P_a = P_b = P_c = P_i = \frac{P_o}{3}$. For power factor correction application,

each module must emulate itself as a resistance to its respective Phase voltage supply. Analysis is carried out for Phase A module, which can be extended to other modules in identical way.

In the proposed work, the surface for the SMC is chosen as $s = \alpha(I_{L_{1a}} - g(t)v_1) + (V_o - V_{ref})$, where, i_{L1a} is the input inductor current of Phase A, v_1 is the rectified AC Phase A input voltage. $g = r^{-1}$ is called the admittance of the resistor r. This is discussed in detail in the next section. For an ideal switching converter module, input power is equal to output power, hence making a case of POPI (Power Out=Power In) structure. Under steady state, when $s = 0$, $i_{L1a} = gv_1$ is satisfied, the input phase current will follow the input phase voltage. Hence, the LFR is realized using SMC.

From the power balance equation of a loss less resistive impedance for one module (similar derivation can be obtained for other two modules as well.)

$$\begin{aligned} P_a &= \frac{P_o}{3} \\ \frac{V_1^2}{r} &= \frac{V_o^2}{3R} \\ V_o &= V_1\sqrt{\frac{3R}{r}} \end{aligned} \tag{5.8}$$

where, V_1 is the rms value of the rectified AC Phase A input, V_o is the output voltage, R is the load resistance and r is the emulated resistance at the input port.

In this work, the LFR r, is kept fixed but not constant; it is changed to accommodate load and line variations. It varies with the change in load or line operating condition. In order to realize an ideal loss-less resistive input impedance r, let us re-write the power balance equation to obtain the input LFR r

$$r = 3\frac{V_1^2}{V_o^2}R \tag{5.9}$$

As long as R stays fixed, for the given input voltage and power, r stays fixed.

The equation (5.9) has been leveraged, to adapt r for any changes sensed in line or load, to ensure that the system always keeps the output voltage regulated. Let δv_1 be the variation in RMS value of the Phase A input voltage, δR is the load variation and δr is the adapted change which occurs in the emulated input impedance. Here V_1, R, r, and V_{ref} are the nominal values of the designated variables. Then,

$$r + \delta r = 3\frac{(V_1 + \delta V_1)^2(R + \delta R)}{V_{ref}^2} \tag{5.10}$$

Expanding (5.10) and comparing the first order terms, we get

$$\delta r = 3\frac{(V_1^2\delta R + 2V_1 R\delta V_1)}{V_{ref}^2} \tag{5.11}$$

This r will adapt itself dynamically with the varying load, line and required output voltage, whenever a change in either of the three variables is detected. Thus giving a robust behaviour.

As the load demand is increased/decreased, the input current increases/decreases in response, so as to regulate the output voltage to its reference value irrespective of any load variation. And all this is carried out while following the principle of *POPI*. Hence, an adaptive loss free resistance is synthesized for Phase A using SMC, under steady state.

5.2.1 Switching function

The switching surface for the sliding mode, consists of an input inductor current error term and a output voltage error term. Moreover, a tuning parameter α is included in the surface to provide a trade-off between the precise regulation and unity power factor. In the present work, the surface is chosen as :

$$\begin{aligned} s &= \alpha(I_{L1a} - I_{L1a,ref}(t)) + (V_o - V_{ref}) \\ &= \alpha(I_{L1a} - \frac{v_1}{r(t)}) + (V_o - V_{ref}) \\ &= \alpha(I_{L1a} - g(t)v_1) + (V_o - V_{ref}) \end{aligned} \tag{5.12}$$

Where, I_{L1a}, V_o are Phase A input inductor current and output voltage and $I_{L1a,ref}$, V_{ref} are their reference value respectively. Parameter $r(t)$ is the dynamically adaptive input resistance as given by (5.10) and $g(t) = r(t)^{-1}$.

5.2.2 Reference current generation

In the present scope of work, the LFR r changes dynamically, as explained in earlier section of the Chapter. The emulated input resistance is calculated as per the operating conditions, following (5.10).

Then, the reference inductor current, used in the surface, is generated depending on the obtained r, as

$$I_{L1a,ref}(t) = v_1/r(t) \tag{5.13}$$

Since the proportionality constant r varies with the settings, the generated reference current varies not only with the input voltage but also with the load. Hence, the proposed work presents itself as an effective control technique for PFC circuits.

5.2.3 Control Law

The transversality condition evaluates the existence of the control input in the derivative of the sliding-surface. It is a necessary condition to ensure the ability of the sliding mode controller to modify the system behaviour. It requires

$$\frac{d}{du}(\frac{ds}{dt}) \neq 0$$

In this case, it can be seen that

$$\frac{d}{du}(\frac{ds}{dt}) = \alpha\frac{x_3}{L_1} > 0 \tag{5.14}$$

The design parameter α is chosen such that from (5.14), the transversality is positive for all the conditions. Since (5.14) is true, then the adopted switching law must follow

$$u = \begin{cases} 0, & \text{if } s > 0. \\ 1, & \text{if } s < 0. \end{cases} \tag{5.15}$$

Therefore, the control law is chosen in this work is given as:

$$u = \frac{1}{2}[1 - sign(s)] \tag{5.16}$$

5.2.4 Equivalent Control

As established from transversality condition

$$\frac{d}{du}(\frac{ds}{dt}) \neq 0$$

Then, the continuous equivalent of the control law (5.16) is derived by imposing

$$\frac{ds}{dt}\Big|_{u=u_{eq}} = 0$$

Using (5.1), the derivative of (5.12) is obtained, assuming g to be constant for an operating condition, as

$$\dot{s} = \alpha(\frac{-x_3}{L_1}(1-u) + \frac{v_1}{L_1}) - \alpha g\frac{dv_1}{dt} + \frac{x_2}{C_o} - \frac{x_4}{3RC_o} \tag{5.17}$$

Replacing u by u_{eq} and equating it to 0, leads to the following expression for equivalent control.

$$u_{eq} = \frac{\alpha(\frac{x_3 - v_1}{L_1}) + \alpha g\frac{dv_1}{dt} - \frac{x_2}{C_o} + \frac{x_4}{3RC_o}}{\alpha\frac{x_3}{L_1}} \tag{5.18}$$

5.3 ANALYSIS OF THE SLIDING MODE CONTROL

The present section deals with the analysis of the sliding mode to establish the existence of sliding mode and the stability of the proposed surface.

5.3.1 Reachability Condition

This condition ensures the existence of the sliding mode i.e. the chosen control law will make the system trajectories reach the designed sliding surface in finite time and will maintain sliding motion then on. It requires to satisfy the η-reachability condition.

$$s\dot{s} < -\eta|s| \tag{5.19}$$

for some $\eta > 0$.
Using (5.17), the following can be obtained

$$s\dot{s} = s\{\alpha(-\frac{x_3}{L_1}(1-u) + \frac{v_1}{L_1}) - \alpha g\frac{dv_1}{dt} + \frac{x_2}{C_o} - \frac{x_4}{3RC_o}\} \tag{5.20a}$$

$$= s\{(1-u)(-\frac{\alpha x_3}{L_1}) + \frac{x_2}{C_o} - \frac{x_4}{3RC_o} + \Gamma\} \tag{5.20b}$$

$$= s\{\frac{1}{2}(1+sign(s))(-\frac{\alpha x_3}{L_1}) + \frac{x_2}{C_o} - \frac{x_4}{3RC_o} + \Gamma\} \tag{5.20c}$$

Where,

$$\Gamma := \alpha\{\frac{v_1}{L_o} - g\frac{dv_1}{dt}\} \tag{5.21a}$$

$$= \alpha\{\frac{V_{sa}|sin(\omega t)|}{L_1} - gV_{sa}\omega|sin(\omega t)| * cot(\omega t)\} \tag{5.21b}$$

where, V_{sa} is the peak input phase A AC voltage, $\omega = 2\pi f$ is the supply frequency.
Remark: v_1 is a periodic function with a period of π. The derivative for v_1 exists for the entire period

except at the corner point i.e. it exists for $(\omega t) \in \Re - n\pi$. Thus, Γ is also a bounded, periodical function with period π. It is analysed for a single period to find the maximum and minimum bounds. And they are given as

$$\Gamma_{max} = \alpha\{\frac{V_{sa}}{L_1\sqrt{1+(g\omega L_1)^2}} + \frac{V_{sa}g^2\omega^2 L_1}{\sqrt{1+(g\omega L_1)^2}}\} \tag{5.22}$$

$$\Gamma_{min} = \alpha g\omega V_{sa} \tag{5.23}$$

When $s > 0$, from (5.15) $u = 0$, thus, (5.20c) becomes

$$s\dot{s} = |s|(-\alpha\frac{x_3}{L_1} + \frac{x_2}{C_o} - \frac{x_4}{3RC_o} + \Gamma) \tag{5.24}$$

In order to satisfy (5.19), the bounds obtained over Γ is used to get the following inequality

$$-\Gamma_{max} - \eta + \frac{x_4}{3RC_o} + \alpha\frac{x_3}{L_1} > \frac{x_2}{C_o} \tag{5.25}$$

When $s < 0$, (5.20c) becomes

$$s\dot{s} = -|s|(\frac{x_2}{C_o} - \frac{x_4}{3RC_o} + \Gamma) \tag{5.26}$$

then, to fulfil (5.19)

$$\Gamma_{min} - \eta + \frac{x_2}{C_o} > \frac{x_4}{3RC_o} \tag{5.27}$$

Therefore, as long as the states satisfy the inequalities given by (5.25) and (5.27), the system trajectory continuously moves towards the sliding manifold. Hence, the reachability condition is established.

5.3.2 Stability of the closed loop system during Sliding mode

Once the trajectories reach the sliding surface, it is to be ensured that the states converge to their equilibrium points.

For the ease of analysis, the system dynamics (5.1) is written in error co-ordinates as

$$\dot{e_1} = \frac{1}{L_1}(v_1 - (1-u_{eq})(e_3 + x_{3r}) - g\frac{dv_1}{dt}) \tag{5.28a}$$

$$\dot{e_2} = \frac{1}{L_2'}((e_3 + x_{3r})u_{eq} - (e_4 + x_{4r})) \tag{5.28b}$$

$$\dot{e_3} = \frac{1}{C_{in}}(-(e_2 + x_{2r})u_{eq} + (e_1 + x_{1r})(1-u_{eq})) \tag{5.28c}$$

$$\dot{e_4} = \frac{1}{C_o}((e_2 + x_{2r}) - \frac{(e_4 + x_{4r})}{3R}) \tag{5.28d}$$

The state variables are the inductor current error (e_1, e_2) and capacitor voltage error (e_3, e_4), such that $e_i = x_i - x_{ir}$. The control input on the surface is given by its equivalent control u_{eq}. Here, the stability of the sliding mode is proved using Eigen values plot of the Jacobian matrix obtained from the linearisation of the non-linear closed-loop model of a Ćuk converter about operating point

$(e_1 = 0; e_2 = 0; e_3 = 0; e_4 = 0)$. The non-linear closed-loop system dynamics in error co-ordinates obtained by substituting the value of u_{eq} (5.18) in (5.28), is given as:

$$\dot{e_1} = \left(-\frac{e_2 + x_{2r}}{\alpha C_o} + \frac{e_4 + x_{4r}}{3\alpha R C_o} + (1 - \frac{1}{L_1}) g \frac{dv_1}{dt} \right) \tag{5.29a}$$

$$\dot{e_2} = \frac{1}{L_2'} \left((e_3 + x_{3r} - v_1 + L_1 g \frac{dv_1}{dt} - \frac{L_1}{\alpha C_0}(e_2 + x_{2r}) - (1 - \frac{L_1}{3\alpha R C_0})(e_4 + x_{4r}) \right) \tag{5.29b}$$

$$\begin{aligned} \dot{e_3} = \frac{1}{C_{in}} \Bigg(& -(e_2 + x_{2r}) + \frac{(e_2 + x_{2r})}{(e_3 + x_{3r})}(v_1 - L_1 g \frac{dv_1}{dt}) + \frac{(e_2 + x_{2r})^2}{(e_3 + x_{3r})} \frac{L_1}{\alpha C_0} \\ & - \frac{(e_2 + x_{2r})(e_4 + x_{4r})}{(e_3 + x_{3r})} \frac{L_1}{3\alpha R C_0} - \frac{(e_1 + x_{1r})(e_4 + x_{4r})}{(e_3 + x_{3r})} \frac{L_1}{3\alpha R C_0} \\ & + \frac{(e_1 + x_{1r})(e_2 + x_{2r})}{(e_3 + x_{3r})} \frac{L_1}{\alpha C_0} + \frac{(e_1 + x_{1r})}{(e_3 + x_{3r})}(v_1 - L_1 g \frac{dv_1}{dt}) \Bigg) \end{aligned} \tag{5.29c}$$

$$\dot{e_4} = \frac{1}{C_o} \left((e_2 + x_{2r}) - \frac{(e_4 + x_{4r})}{3R} \right) \tag{5.29d}$$

The stability is analysed for the Sliding mode. During which, $(s = 0)$,

$$\alpha e_1 + e_4 = 0 \quad Or, \;\; e_1 = \frac{-e_4}{\alpha} \tag{5.30}$$

Using (5.30), it is possible to obtain a reduces order model. Substituting value of e_1 in terms of e_4, gives reduced order Jacobian as

$$A_C = \begin{bmatrix} \frac{\delta \dot{e_2}}{\delta e_2}\Big|_{e=0} & \frac{\delta \dot{e_2}}{\delta e_3}\Big|_{e=0} & \frac{\delta \dot{e_2}}{\delta e_4}\Big|_{e=0} \\ \frac{\delta \dot{e_3}}{\delta e_2}\Big|_{e=0} & \frac{\delta \dot{e_3}}{\delta e_3}\Big|_{e=0} & \frac{\delta \dot{e_3}}{\delta e_4}\Big|_{e=0} \\ \frac{\delta \dot{e_4}}{\delta e_2}\Big|_{e=0} & \frac{\delta \dot{e_4}}{\delta e_3}\Big|_{e=0} & \frac{\delta \dot{e_4}}{\delta e_4}\Big|_{e=0} \end{bmatrix}$$

where,

$$\frac{\delta \dot{e_2}}{\delta e_2}\Big|_{e=0} = \frac{-L_1}{L_2' \alpha C_0}; \qquad \frac{\delta \dot{e_2}}{\delta e_3}\Big|_{e=0} = \frac{1}{L_2'}; \qquad \frac{\delta \dot{e_2}}{\delta e_4}\Big|_{e=0} = \frac{1}{L_2'}(\frac{L_1}{3\alpha R C_0} - 1);$$

$$\frac{\delta \dot{e_3}}{\delta e_2}\Big|_{e=0} = \frac{1}{C_{in}} \left(-1 + \frac{(v_1 - L_1 g \frac{dv_1}{dt})}{x_{3r}} + \frac{2x_{2r}}{x_{3r}} \frac{L}{\alpha C_0} - \frac{x_{4r}}{x_{3r}} \frac{L_1}{3\alpha R C_0} + \frac{x_{1r}}{x_{3r}} \frac{L_1}{\alpha C_0} \right);$$

$$\frac{\delta \dot{e_3}}{\delta e_3}\Big|_{e=0} = \frac{-1}{C_{in} x_{3r}^2} \left((x_{1r} + x_{2r})(v_1 - L_1 g \frac{dv_1}{dt}) + x_{2r}^2 \frac{L_1}{\alpha C_0} - x_{2r} x_{4r} \frac{L_1}{3\alpha R C_0} - x_{1r} x_{4r} \frac{L_1}{3\alpha R C_0} + x_{1r} x_{2r} \frac{L_1}{\alpha C_0} \right);$$

$$\frac{\delta \dot{e_3}}{\delta e_4}\Big|_{e=0} = \frac{1}{C_{in}} \left(-\frac{x_{2r}}{x_{3r}} \frac{L_1}{3\alpha R C_0} - \frac{x_{1r}}{x_{3r}} \frac{L_1}{\alpha C_0} \right);$$

$$\frac{\delta \dot{e_4}}{\delta e_2}\Big|_{e=0} = \frac{1}{C_0}; \qquad \frac{\delta \dot{e_4}}{\delta e_3}\Big|_{e=0} = 0; \qquad \frac{\delta \dot{e_4}}{\delta e_4}\Big|_{e=0} = \frac{-1}{3RC_0}$$

The Eigen values of this Jacobian are plotted for varying values of load, α and V_1. The plots for the three cases is presented in Fig. 5.3, Fig. 5.4 and, Fig. 5.5, respectively.

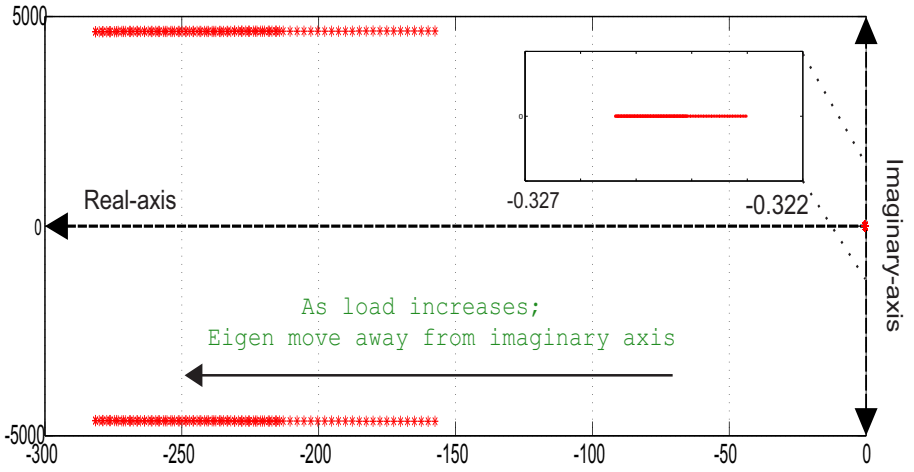

Figure 5.3 : Eigen value plot: variation in load

For Fig. 5.3, the output load for the Ćuk module is varied from 10 % to 110 %, keeping all other parameters to their nominal values given in Table 5.1. The corresponding locus of the Eigen values is presented. As seen, the values are in left half of the plane through out and with the increase in load, they move away from the imaginary axis.

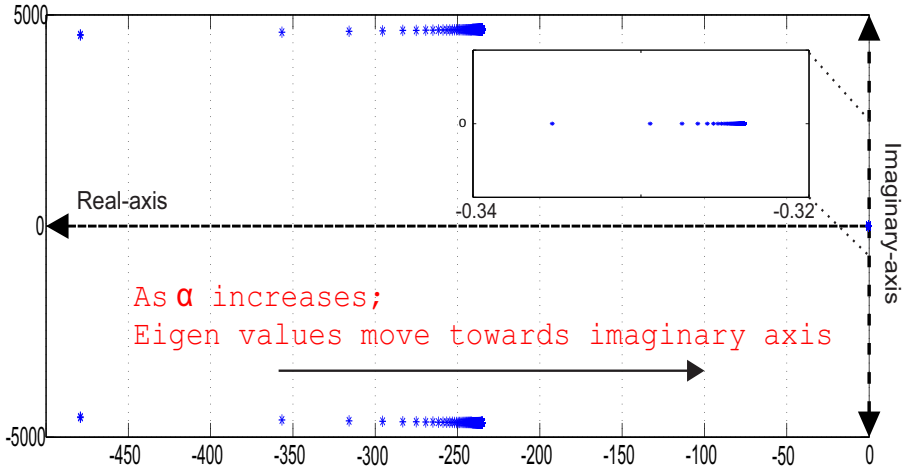

Figure 5.4 : Eigen value plot: variation in α

In Fig. 5.4, the locus of Eigen values corresponding to the change in tuning parameter α is presented. The value of α is varied from 1 to 500, at nominal operating conditions. The values remain in left half of the plane always with move towards the imaginary axis with the increase in α.

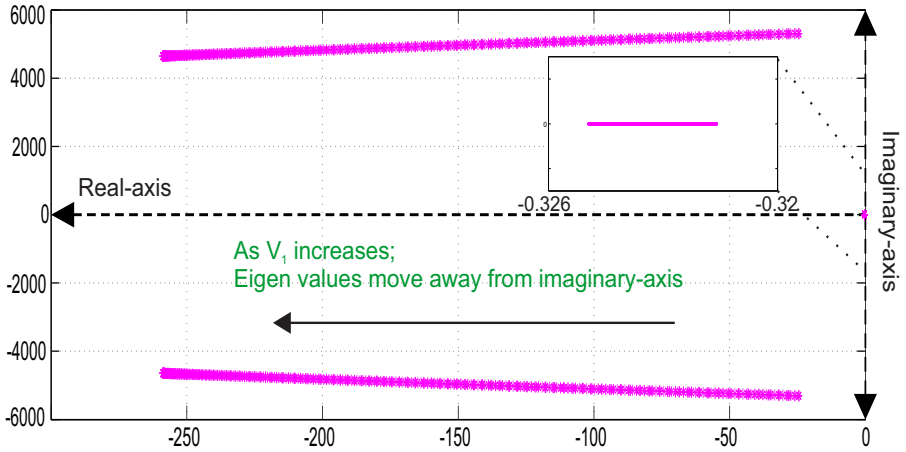

Figure 5.5 : Eigen value plot: variation in line voltage

The Eigen values locus for the change in line conditions is presented in Fig. 5.5. The value of V_1 is changed from minimum 0 to maximum 120 V, and as seen the corresponding values always remain in the left half of the plane. Furthermore, as V_1 is increased, the values move away from the imaginary axis.

The stability of the sliding mode is established against all line and load conditions. By plotting the Eigen values of the linearised Jacobian, around operating points, it is shown that since Eigen values always stay negative, the system is stable throughout.

5.4 SIMULATION STUDIES

Simulation studies are carried out to validate the proposed scheme. The Ćuk converter specifications are kept as shown in Table 5.1 for CCM operation. The simulations are carried out in MATLAB-Simulink environment. The study is categorized into two sections. The first section illustrates the adaptive nature of the emulated SLFR *r*. A comparative analysis is shown in the second section, between the proposed work, and the work presented in [Kamnarn and Chunkag, 2009].

5.4.1 Adaptive nature of proposed SLFR

This section is further divided into different subsections to explore the adaptive nature of SLFR *r* with respect to variation in load resistance *R*, input voltage V_s and reference output voltage V_{ref}. Since all the phases are symmetrical, only one phase is explored. In this section, the adaptive nature of LFR *r* is explored for variable load resistance *R*, input voltage V_{sa} and reference output voltage V_{ref}. The nominal values of the system operating conditions are taken as: V_{sa}=120 V(RMS) 60 Hz, V_{ref}=400 V, load resistance *R*= 160 Ω.

- **Load Change:** The load resistance is changed from 160 Ω to 200 Ω (1000 W to 800 W) at 0.3 sec while keeping the other parameters to their nominal value. Corresponding waveform of interest are shown in Fig. 5.6.

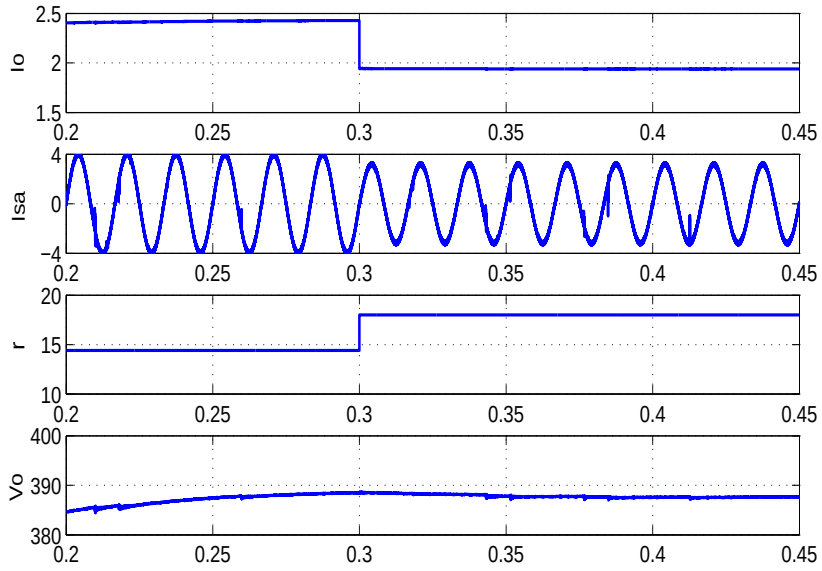

Figure 5.6 : Adaptiviy of *r* to load resistance variation

- **Input voltage Change:** A change in the input voltage from 120V (RMS) to 140V (RMS) is brought about at 0.3 sec with no change in other parameters. Fig. 5.7 presents the response of the system.

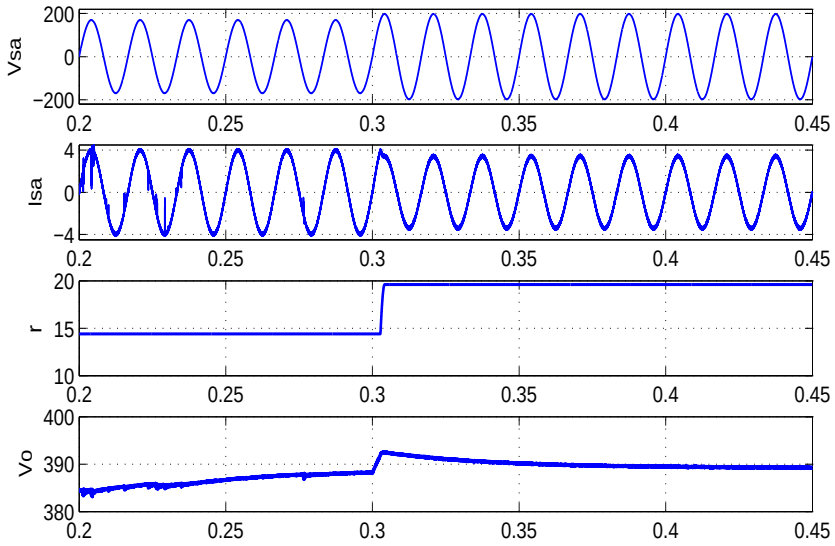

Figure 5.7 : Adaptiviy of *r* to input voltage variation

- **Reference Voltage Change:** Fig. 5.8 shows the system response when the reference output voltage is changed from 400V to 300V at 0.3 sec with other parameters kept to their nominal value.

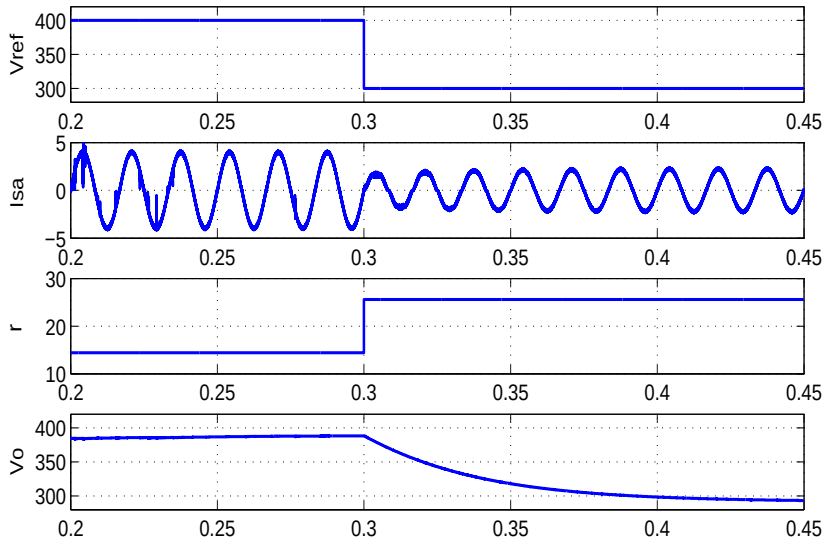

Figure 5.8 : Adaptiviy of *r* to reference voltage variation

All the results presented demonstrate the adaptive nature of the emulated resistance r, per phase, with the variation in operating conditions. The change in value of *r* causes the inductor reference current to change, in order to achieve the dual aim of maintaining a near unity power factor and regulating the output voltage.

5.4.2 Comparative Analysis

This section presents comparison of the system response, at steady state and also in the event of load change. The comparison is carried out between the proposed controller and the work which proposed the Ćuk converter based modular three phase converter [Kamnarn and Chunkag, 2009]. The referred work uses PI controller with power balancing technique and load feed-forward to improve system dynamics, for telecommunication application. The system gives good voltage regulation and power factor correction at higher loads. However, it suffers with current quality degradation at lower loads. In order to provide the proper comparison, the proposed control scheme is implemented to the set-up presented in [Kamnarn and Chunkag, 2009].

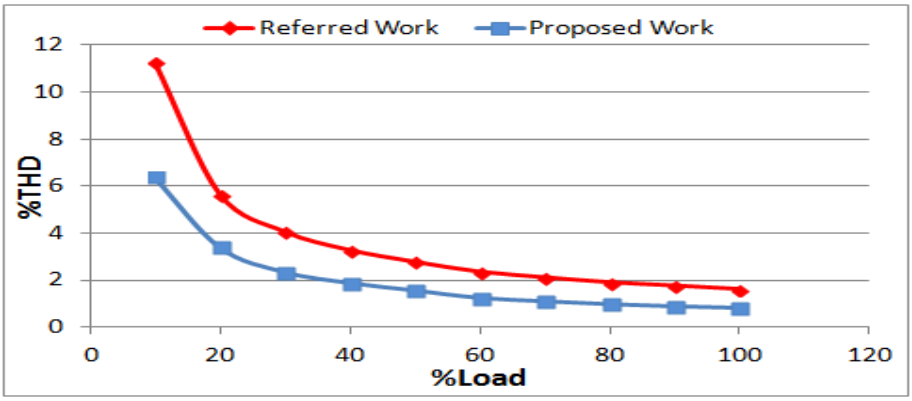

Figure 5.9 : %THD in Phase A input current for the two controllers under comparison.

The phase A input current %THD is plotted for the two cases under consideration at different output power in Fig. 5.9. It can be seen that for the referred work, lower loads have higher distortion, while for the proposed controller the current quality is better at all load levels.

The simulation results of the work in [Kamnarn and Chunkag, 2009] and the proposed controller are summarized in Table 5.2. Moreover, the controller in [Kamnarn and Chunkag, 2009] has high starting current and undershoot, whereas, no undershoot/overshoot and in-rush current at starting is observed for the proposed controller. However, the proposed controller suffers with the steady state error but is less than < 2 % for entire load range.

Table 5.2 : Comparison of simulation results

Parameter	Controller in Kamnarn and Chunkag [2009]	Proposed ASLFR Controller
Inductors L_1, L_2	5.069 mH, 10.44 μH	5.069 mH, 10.44 μH
Output capacitor	1360 μF	1360 μF
Input voltage	220 V, 50 Hz	220 V, 50 Hz
Reference output voltage	-48 V	-48 V
Starting peak rush current	13 A	Not observed
Starting voltage undershoot	23V	Not observed
Load Transients	10% to 100%	10% to 100%
Steady state error	0.05V, 0.05V	-0.2V, 0.78V
% THD	11.26%, 1.61%	6.39%, 0.81%

5.5 EXPERIMENTAL STUDIES

The proposed theory has been experimentally validated, analogous to the simulation study cases. The experimentation study was carried out at the Electrical and Computer Engineering department of Concordia University, Montreal, Canada. A 1 kW laboratory prototype of the converter was made for the purpose. Fig. 5.10 shows the set-up for experimentation consisting of the designed converter, with the specifications provided in Table 5.3.

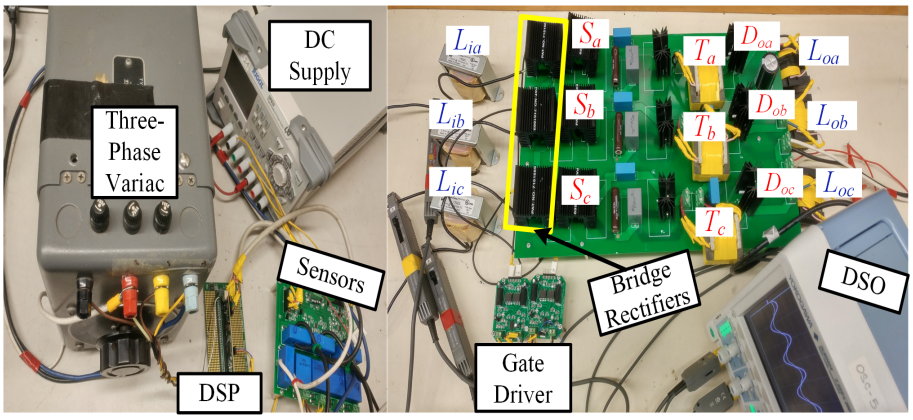

Figure 5.10 : Experimental setup

In Fig. 5.10, a three-phase variac connected to the supply (120 V, 60 Hz), the three-phase modular Ćuk converter, a gate driver unit, sensor board consisting of current & voltage sensors

and a DC supply for them, DPO and control platform are shown. TMS320F28335 Series Digital Signal Processors & Controllers is used for implementing the control. Experimental parameters are kept same as the simulation parameters.

Table 5.3 : Experimental Set-up Component Specifications

Component	Specification
Power switches, S_a, S_b, S_c	C2M0080120D, 1200 V SIC MOSFET
Output diodes, D_a, D_b, D_c	IDP30E120, 1200 V, 30 A
Rectifier modules	FBO16-12N, 1200 V, 16 A
Energy transfer capacitors	B32674D8105K, 1 μF
Clamping diodes	IDP30E120, 1200 V, 30 A
Clamping capacitors, c_s	R76UR32204030J, 220 nF
Clamper resistors, R_s	B20J10KE, 10 kΩ, 20 W
Output capacitor, C	LGN2W471MELC45, 2 x 470 μF
Input inductors L_{1a}, L_{1b}, L_{1c}	159ZL, 2.5 mH, 10A
Output inductors L_{2a}, L_{2b}, L_{2c}	59 x 31 x 22, ETD Ferrite cores
Transformers	55 x 28 x 21, EE Ferrite cores

In this section, the experimental results corresponding to the system's steady state as well as transient response are presented. The cases involve (I) Steady state Response at the rated load, (II) Response to Load transients, (III) Response to Input voltage variation and, (IV) Response to change in Reference output voltage. Additionally, the harmonic content of the input current, for the proposed system, with regard to the variation in load is also presented. The magnitude of the measured input current harmonics is compared with the regulation limits of EN 61000-3-2 Class A devices.

5.5.1 Test Case-I: Steady state Response

This subsection presents the proof of concept, steady state behaviour of the proposed system. The results are corresponding to the rated power of 1kW. The three-phase source currents are captured in Fig. 5.11, the power factor correction in Phase A along with tight voltage regulation is demonstrated in Fig. 5.12, and the harmonic content in the input phase current is Fig. 5.13. In the captured screens the output voltage V_o is set to 200 V/div, input voltage V_s is 100 V/div and the input current I_s is set to 5 A/div. The time base is 5 ms/div.

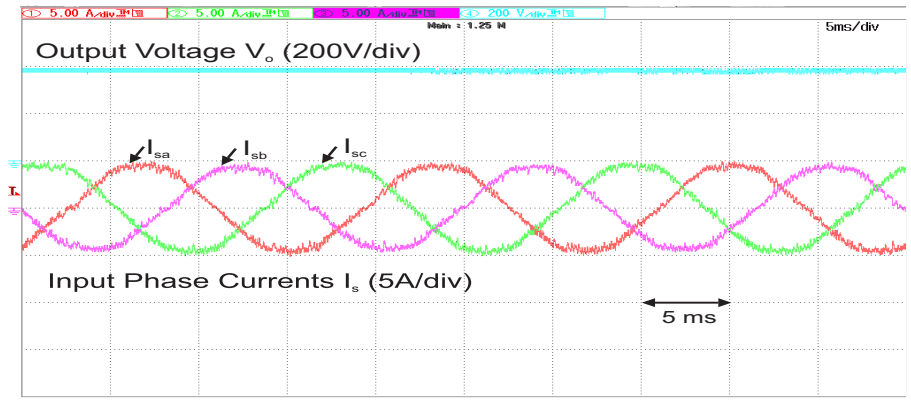

Figure 5.11 : Three-phase source currents at 1kW

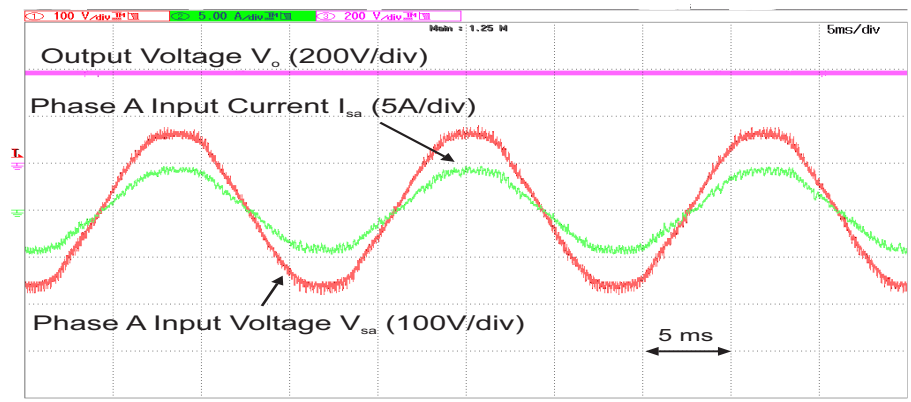

Figure 5.12 : Unity power factor correction in Phase A

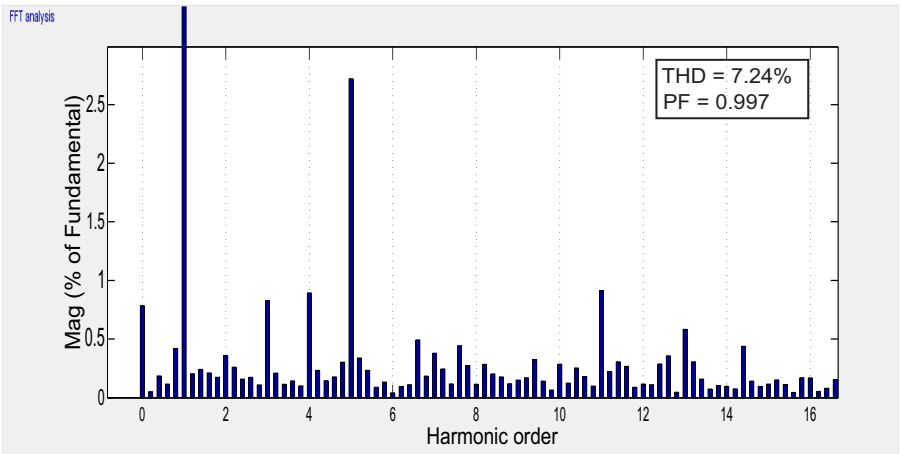

Figure 5.13 : Harmonic content of input current 1kW

As seen, the input currents are sinusoidal and the output voltage is settled at 400 V. The

measured input power factor (PF) is 0.997 and THD is 7.24 % at 1 kW output power.

5.5.2 Test Case-II: Response to Load Transient

The adaptive nature of the proposed controller to load change is demonstrated in this subsection. The transient response of the system for load step change from 500 W to 750 W and *viceversa* are shown in Fig. 5.14 and 5.15. The oscilloscope capture demonstrates the input phase voltage V_{sa}, input current I_{sa}, output voltage V_o, and output load current I_o under variable load conditions. The channels have been set to 100 V/div for V_{sa}, 5 A/div for I_{sa}, 200 V/div for V_o and 1 A/div for I_o. Time base is set to 20 ms/div.

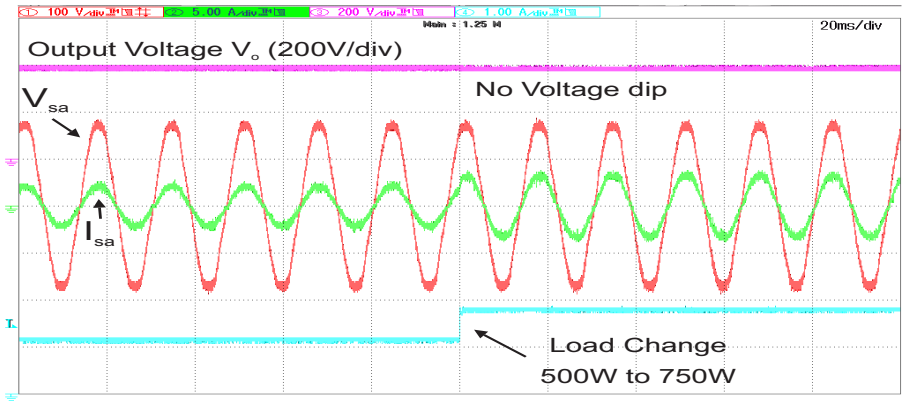

Figure 5.14 : System response to Test Case-II: Load change from 500W to 750W. Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa} (5 A/div), Output voltage V_o (200 V/div), Load current I_o (1 A/div), Time base 20 ms/div.

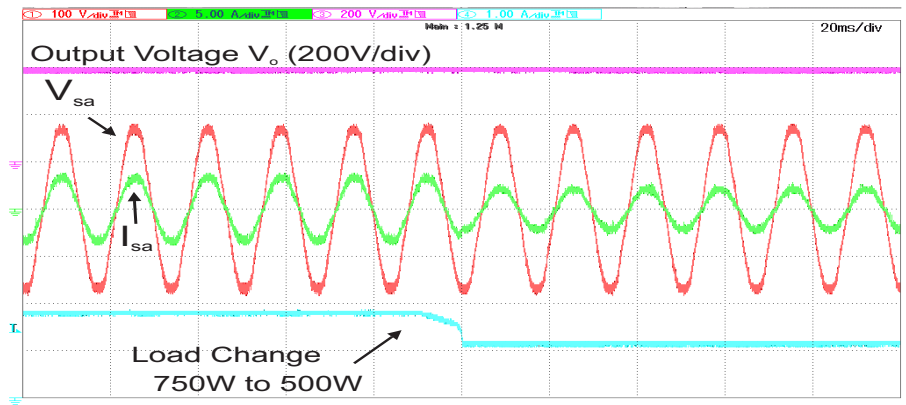

Figure 5.15 : System response to Test Case-II: Load change from 750W to 500W. Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa} (5 A/div), Output voltage V_o (200 V/div), Load current I_o (1 A/div), Time base 20 ms/div.

These results show the robustness of the system to load variation. The controller reacts sufficiently fast to the load transients. The output voltage is regulated to its reference value in a single cycle with no undershoots.

5.5.3 Test Case-III: Response to Line Variation

The system response to line variation is shown in Fig. 5.16. A transition in input phase voltage is made using a three-phase Variac, from 140 V to 120 V. The waveforms corresponding to the variation, is captured in the oscilloscope. It includes V_{sa} (100 V/div), I_{sa} (2 A/div), and V_o (200 V/div).

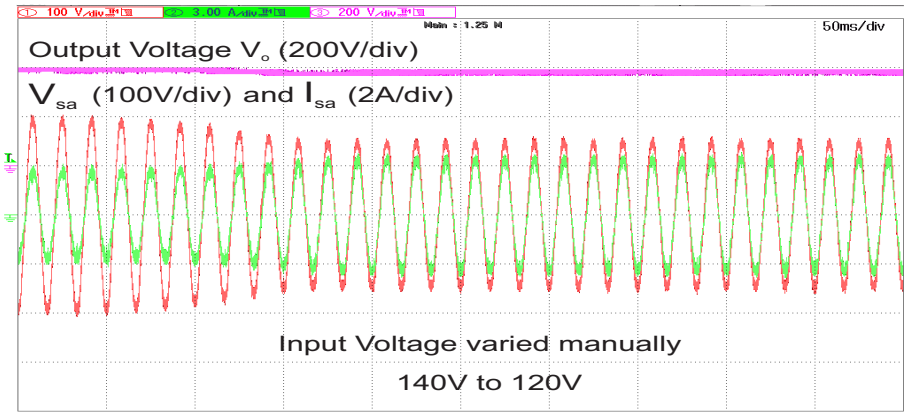

Figure 5.16 : System response to Test Case-III: Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa} (2 A/div), Output voltage V_o (200 V/div), Time base 50 ms/div.

From the results it can be seen that, as the input voltage decreases, the emulated input resistor increases, causing a rise in input current, so as to meet the required power demand while maintaining the voltage regulation.

5.5.4 Test Case-IV: Response to change in Reference Output Voltage

The robustness of the system to a change in reference output voltage, from 400 V to 300 V, is shown in Fig. 5.17. The oscilloscope capture shows the waveform for V_{sa} (100 V/div), I_{sa} (2 A/div), and V_o (200 V/div).

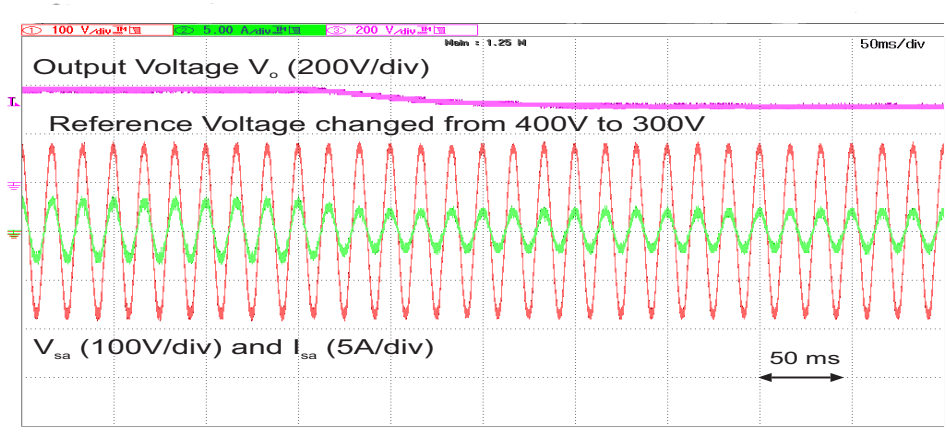

Figure 5.17 : System response to Test Case-IV: Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa} (2 A/div), Output voltage V_o (200 V/div), Time base 50 ms/div.

The system responds to the new output voltage demand fast and reaches the desired output voltage while maintaining a high input power factor.

The variety of test cases conducted, experimentally, establish the effectiveness of the proposed ASLFR based controller. The robustness of the system to the load and line variations is proven, as it enables excellent dynamic performance in maintaining output voltage as well in providing harmonics-free rectification.

5.5.5 Harmonic Analysis

This section provides the distortion data for input current under various operating conditions. The work in this Chapter has been proposed in light of IEC 61000-3-2:2014 [IECLimits, 2014]. The aforementioned regulation deals with the equipment working with input power exceeding 75 W and categorizes them into four classes. The EV charger application falls in Class A devices, as discussed earlier in the Chapter. Fig. 5.18 presents a comparative graph showing the measured and the permissible current harmonics for Class A equipment as per IEC 61000-3-2:2014 [IECLimits, 2014] at different load values.

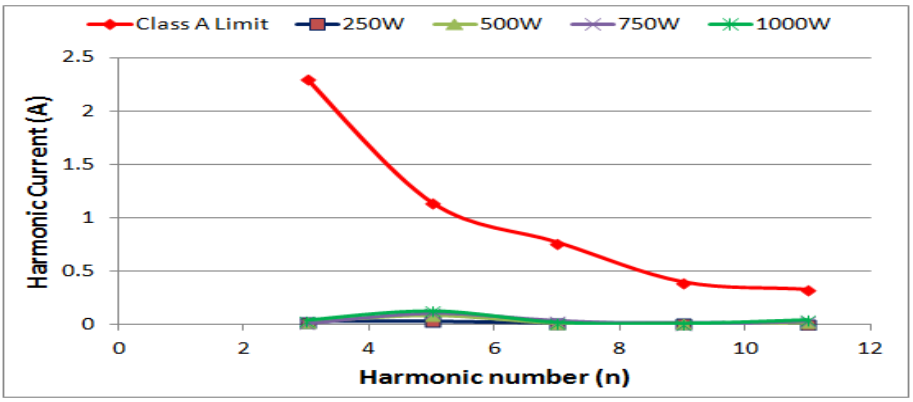

Figure 5.18 : Harmonics current as a function of harmonic order and output power versus IEC 61000-3-2 Class A limits.

It is shown that the magnitude of the measured input current harmonics for the three-phase system, are well within limits at all power levels. Thus the system comply with the set regulatory standards as per IEC 61000-3-2:2014 Class A limits.

5.6 SUMMARY

The Chapter used adaptive LFR controller for presenting a three-phase AC/DC converter, using Ćuk rectifier modules, as an effective single-stage solution for three-phase PFC in EV chargers. The main purpose of the proposed scheme is to reduce the number of the conversion stages while offering improved dynamic response. It provides with nearly unity power factor and fast dynamic transient based on emulating an adaptive LFR. A comparative study is done to validate the effectiveness of the adopted novel scheme over the existing single-stage three-phase modular Ćuk converters employed for telecommunication application. The %THD in the referred work increases at low loads (at 10% load % THD is 11%) whereas the proposed scheme maintains better input current quality at all load levels (at 10% load, %THD is 6%). The simulation and experimental results establishes that the proposed system gives excellent power factor correction and tight voltage regulation simultaneously. Steady-state and dynamic analyses have been discussed. At the steady state nominal load of 1 kW the system provides a power factor of 0.997. Under

load transient, the proposed controller recovers the voltage within a single cycle with effectively no undershoot. The proposed approach offers the following advantages: simple control and fast dynamic response. It meets the harmonic regulations as per IEC 61000-3-2 class A limits.

Sliding mode control makes the system robust against the disturbances once the system trajectories are on the switching surface. However, during the reaching phase i.e. the time taken by the system trajectories to reach the surface, the system is susceptible to disturbances. In the next Chapter, an integral sliding mode based controller will be discussed. There is no reaching phase in the integral sliding mode control. Thus integral sliding mode control ensures the robustness against the matched uncertainty and disturbances from the beginning of the system response. Moreover, the integral sliding mode control allows to merge SMC with the classical control methodologies such as optimal control, H_∞, PID Control.