List of Figures

Figure	Title	page
1.1	An ideal switch and it's switching waveform (voltage, current, and power)	2
1.2	Switching waveform for a practical switch (voltage, current, and power)	3
1.3	Sources of power loss in a synchronous buck converter [Qahouq et al., 2007].	4
1.4	Plots for typical buck converter [Qahouq et al., 2007].	5
1.5	Variation of losses in a converter with load [Erickson and Maksimovic, 1995].	6
1.6	Mode hopping with load [Erickson and Maksimovic, 1995], [Zhou et al., 1997].	7
1.7	Three control modes converter and their efficiency as functions of output current.	
	[Huang et al., 2006].	8
1.8	The operation principle of the conventional burst mode [Lee et al., 2013].	9
1.9	Types of sampling. (a) Fixed time period and variable threshold, (b) Variable time period	
	and fixed threshold, (c) Variable time period and variable threshold.	14
1.10	Concept of Sliding mode control	16
1.11	Front end circuitry of a typical electronic equipment.	19
2.1	Isolated Half Bridge Converter	26
2.2	Switching waveform for a Half Bridge Converter	26
2.3	(a).Block diagram for classical implementation of SMC. (b).Block diagram for Event-	
	triggered implementation of SMC.	32
2.4	Hysteresis modulation based SMC (HM-SMC).	32
2.5	(a).Block diagram for HM-SMC. (b).Block diagram for ET-SMC.	33
2.6	Comparison of the fixed size sliding band for HM-SMC (in blue) and load adaptive sliding	
	band for ETSMC (in red).	33
2.7	Voltage Regulation for SMC and ETSMC and the corresponding switching signal	35
2.8	Evolution of error for SMC and ETSMC and occurrence of events	36
2.9	ETSMC and Load Variation: Event density for load change	36
2.10	ETSMC and Load Variation: Load variation with corresponding variation in switching signal	36
2.11	Experimental setup	37
2.12	Experimental demonstration of Classical SMC and ETSMC: output voltage and switching actions	38
2 13	Experimental results for the proposed theory: output voltage and switching actions	00
2.1.9	under variable input.	38
2.14	Experimental results for the proposed theory: output voltage and switching actions under variable load conditions.	39
2.15	Experimental results for the proposed theory: Switch voltage and switching actions under variable load at Load 300W.	39
2.16	Experimental results for the proposed theory: Switch voltage and switching actions under variable load at Load 100W.	40
2.17	Experimental results for the proposed theory: Saving in losses with respect to load conditions.	40
_		4-
3.1	(a) Uncompensated (b) Compensated	45
3.2	A circuit of LFR as a two-port network.	46
3.3	PFC based on a boost converter	47

3.4	Event-triggered SMC for PFC	50
3.5	Principle of HM-SMC	51
3.6	Power factor correction for SMC and ETSMC and the corresponding switching signal	51
3.7	Adaptive band for Event-triggered SMC for PFC	52
3.8	Fixed band for HM-SMC	52
3.9	Experimental setup	53
3.10	Experimental validation. CH1: Rectified AC Input Voltage V_1 (50 V/div). CH2: Inductor	
	Current I_L (100 mA/div). CH3: Switching Pulses	54
4.1	Block diagram of switching converter emulated as ASLFR	58
4.2	PFC based on a boost converter	59
4.3	Region of Existence	62
4.4	Adaptiviy of <i>r</i> to load resistance variation	65
4.5	Adaptiviy of <i>r</i> to input voltage variation	65
4.6	Adaptiviy of <i>r</i> to reference voltage variation	65
4.7	Representing a combination load as equivalent resistive load $R_{eq}=rac{V_o}{I_o}$	66
4.8	System response and R_{eq} profile for a CPL load	66
4.9	Output Voltage waveform under load change	67
4.10	%THD in input current for the three controllers.	67
4.11	Experimental setup	68
4.12	Response of ASLFR based controller to Test Case-I. CH1: Rectified AC Input Voltage V_1	
	(40 V/div). CH2: Inductor Current I_L (500 mA/div). CH3: output capacitor voltage V_o (100	
	V/div). Time base 10 ms/div.	69
4.13	Input Current, Input Voltage and Output Voltage waveform for Test Case-I	69
4.14	Harmonic spectrum of the input current for the two loads of Test Case-I	70
4.15	Response of ASLFR based controller to Test Case-II. CH1: Rectified AC Input Voltage V_1	
	(40 V/div). CH2: Inductor Current I_L (200 mA/div). CH3: output capacitor voltage V_o (100	70
	V/div). Load Resistance 300 Ω and V_{ref} 150 V.	70
4.16	Input Current, Input voltage and Output voltage waveform for Test Case-II	/1
4.1/	Kesponse of ASLFR based controller to fest Case-III. CH1: Rectified AC input voltage	
	V_1 (40 V/div). CH2: Inductor Current I_L (200 IIIA/div). CH3: output capacitor voltage V_o	71
4 4 9	(100 V/div). The base 20 ms/div. Load Resistance 300 s2 and V_{in} 100 V.	71
4.10	Permissible and measured 3 rd Harmonic current at different load operating points	72
4.19	Single stage Power factor correction for Classical and Event triggered ASLER	72
4.20	Single stage rower factor correction for classical and Event triggered ASE N .	73
4.21	Evolution of error for Classical and Event-triggered ASI FR	74
4.22	Input Current for the two cases	74
4.24	Permissible and measured Harmonic current for 150 W load	75
4.24	Event-triggered ASI FR adoption at different load levels	75
4.26	Permissible and measured 3^{rd} harmonic at different load conditions.	76
5 1	Power circuit of the modular three-phase ac-dc converter using Cuk rectifier modules	79
5.2	Fourier circuit of the isolated PEC based $Cuk converter when referred to the primary side$	80
53	Figen value plot: variation in load	87
5.4	Figen value plot: variation in α	87
5.5	Figen value plot: variation in line voltage	88
5.6	Adaptivity of r to load resistance variation	89
5.7	Adaptiviy of <i>r</i> to input voltage variation	89
5.8	Adaptiviv of <i>r</i> to reference voltage variation	90
5.9	%THD in Phase A input current for the two controllers under comparison.	90
5.10	Experimental setup	91

5.11	Three-phase source currents at 1kW	93
5.12	Unity power factor correction in Phase A	93
5.13	Harmonic content of input current 1kW	93
5.14	System response to Test Case-II: Load change from 500W to 750W. Input Phase Voltage	
	V_{sa} (100 V/div), Input Current I_{sa} (5 A/div), Output voltage V_o (200 V/div), Load current I_o	
	(1 A/div), Time base 20 ms/div.	94
5.15	System response to Test Case-II: Load change from 750W to 500W. Input Phase Voltage	
	V_{sa} (100 V/div), Input Current I_{sa} (5 A/div), Output voltage V_o (200 V/div), Load current I_o	
	(1 A/div), Time base 20 ms/div.	94
5.16	System response to Test Case-III: Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa}	
	(2 A/div), Output voltage V_o (200 V/div), Time base 50 ms/div.	95
5.17	System response to Test Case-IV: Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa}	
	(2 A/div), Output voltage V_o (200 V/div), Time base 50 ms/div.	95
5.18	Harmonics current as a function of harmonic order and output power versus IEC 61000-	
	3-2 Class A limits.	96
6.1	PFC based on a boost converter	103
6.2	Dual loop control structure	104
6.3	Frequency domain plots for open-loop transfer function and closed-loop gain of the	
	current-loop: (a) magnitude and (b) phase.	105
6.4	Frequency domain plot for open-loop transfer function and closed-loop gain of the	
	volatge-loop: (a) magnitude and (b) phase.	106
6.5	Load transient operation results with proposed ISM based controller	108
6.6	Plot of the switching function <i>s</i>	108
6.7	Steady state response using nominal controller.	109
6.8	System response using nominal controller against the external disturbance.	109
6.9	System response using nominal controller +ISMC against the external disturbance.	110
6.10	Steady state result for reduced parameters using nominal control.	110
6.11	Steady state result for reduced parameters using nominal with ISM based control.	111
6.12	A Z source converter	111
6.13	Pole zero map of control-to-capacitor-voltage transfer function for a symmetrical full	
	order and reduced order ZSC	113
6.14	Dual loop control structure	114
6.15	Current-loop frequency domain plot for open-loop transfer function and closed-loop	
	gain: (a) magnitude and (b) phase.	115
6.16	Voltage-loop frequency domain plot for open-loop transfer function and closed-loop	
	gain: (a) magnitude and (b) phase.	115
6.17	Pole zero map with $L_2 < L_1$ full order and reduced order ZSC	116
6.18	Effect of asymmetry due to reduction in sensed inductor L_1 size	117
6.19	Effect of asymmetry due to reduction in unmodeled inductor L_2 size	118
6.20	System response to external disturbance in the input channel	118
6.21	System response to external disturbance in the generated reference current	119
6.22	Transient response to load change	119
6.23	Switchng variable for load variation in ZSC	120