# 2

# Analysis of Substrate Integrated Coaxial Line & Transitions

Novel technologies developed in the recent times have paved the way for high-speed data transmission [170, 18, 171]. Transmission lines that support wide-bandwidth, low-dispersion, low-loss, and easily integrated with other planar technologies has been of keen interest to researchers. Substrate integrated coaxial line (SICL) stands out as an emerging technology [51] that can address the upcoming needs of low-delay/ non-dispersive 5G communication and deliver high performance in terms of overall loss and size. SICL realizes a traditional coaxial in planar form using multi-layer printed circuit board (PCB) technology. Further, in order to ease the fabrication process the design and implementation of planar coaxial resonators [172] using low profile substrate have gained popularity for their performance. The self-packaged SICL structure is electromagnetically robust as the inner conducting strip sandwiched between a pair of dielectrics is covered with an outer conductor formed by top and bottom ground planes connected by electroplated via holes..Traditionally the lateral metalized vias in SICL based circuits have been employed to obtain better signal integrity owing to its shielded nature [7]. The characteristic impedance of SICL line is considered to be a function of the width of inner conducting strip ($W_{in}$) to height of substrate ($H$) ratio ($2H/W_{in}$) [51] and is usually determined through optimization using a full-wave simulator. This brings the need for a closed form SICL formula to eliminate the need for optimization. A technique to approximately synthesize the characteristic impedance of SICL proposed in [174] is hard to evaluate since it is not derived as a closed form expression. In an U. S patent exploring SICL array for high speed multichannel data transmission [175], a closed form expression for the characteristic impedance of a SICL line has been derived. But this expression does not take the width of outer conductor formed by vias in to consideration. An asymmetric planar coaxial line [176] modeled using substrates of different thickness also did not show any variation in characteristic impedance of SICL line for small change in width of outer conductor width. Similar observation was made by the authors in [177] where the upper substrate height was chosen only to be 0.254 mm. Contrary, to the notion of metallic vias in SICL being only useful of lateral shielding, a novel perturbation technique has been demonstrated utilizing the metallic vias to perturb the characteristic impedance SICL by utilizing to lateral vias in a SICL line with small width of inner conductor to height of substrate (Win/2H) ratio to design highly selective low loss $K_u$-band BPF [92]. Therefore, it is evident that there is a need for a closed form expression for SICL line taking all its physical parameters in to consideration in order to design various microwave and millimeter-wave circuits with ease.

Further in this chapter various wideband transitions to feed SICL line using coaxial and microstrip transmission line with DC isolation has been explored. Novel topology to facilitate a transition from microstrip line to SICL without the need for any blind is discussed in detail. A new SICL based wideband transition to isolate DC bias circuitry required for active circuit from the system is also proposed for X-band. The ease of integration of SICL technology with existing technology makes to highly desirable in small-factor microwave/ millimeter-wave components with good performance.

## 2.1 DETERMINATION OF CHARACTERISTIC IMPEDANCE OF SUBSTRATE INTEGRATED COAXIAL LINE (SICL)

Fabrication of a planar coaxial line requires two dielectric substrate layers with copper cladding on both sides of the substrate. The inner conductor of the planar coaxial is realized by developing a rectangular conducting strip on the bottom side of the top substrate as shown in Fig. 2.2. The dielectric enclosure around the inner conductor is formed by sandwiching the top substrate with the bottom substrate using a prepreg bond layer. 3 stacks (top substrate, prepreg bond layer & bottom substrate) is loaded in to into the bonding press. This press comprises of plates pre-heated to a certain temperature that enforces the substrate layers to bond together. The high temperature plates melts and binds the epoxy resin in the prepreg and the applied pressure forms the multi-layer PCB. Rows of via holes are drilled in the top and bottom substrate along both sides of the outer conducting strip using a milling machine. These vias are electroplated using PTH (plated through hole) technology to connect the top and bottom ground to form the outer conductor of this planar coaxial line. Further, rectangular metallic strip is enforced through the side vias to improve the performance of SICL section.

Determination of characteristic impedance of a lossless TEM based transmission line is given by:

$$Z_o = \frac{1}{vC} \tag{2.1}$$

where $v$ is the velocity of propagation of light in free space and C is capacitance of the line. To simplify the computation, a rectangular coaxial line is considered with continuous perfect electric (PEC) boundary along the inner conducting strip as shown in Fig. 2.1. So from (2.1) it is clear that the capacitance of the line has to be determined in order to calculate the characteristic impedance. The fringing field capacitance $C_{f1}$ and capacitance with the outer conductor $C_{o1}$ [173] is given as

$$C_{f1} = \frac{4\varepsilon}{\pi}\left[\log\frac{g_s^2 + h_{sub}^2}{4h_{sub}^2} + 2\left(\frac{h_{sub}}{g_s}\right)\arctan\frac{g_s}{h_{sub}}\right] \tag{2.2}$$

$$C_{o1} = 2\varepsilon\left(\frac{w_{in}}{h_{sub}} + \frac{t_s}{g_s}\right) \tag{2.3}$$

The total capacitance of the conducting strip with assumed zero thickness is given by:

$$C_{eff} = C_{f1} + C_{o1} \tag{2.4}$$

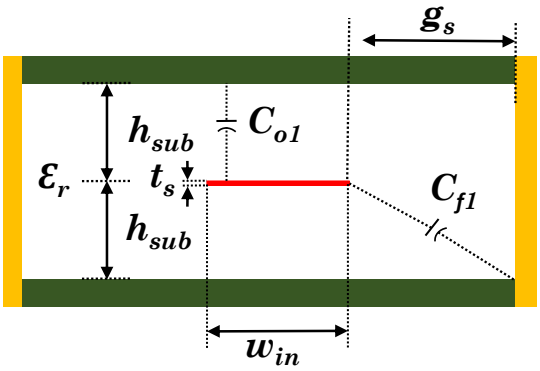



**Figure 2.1 :** Equivalent rectangular coaxial line for determination of effective capacitance of the line.

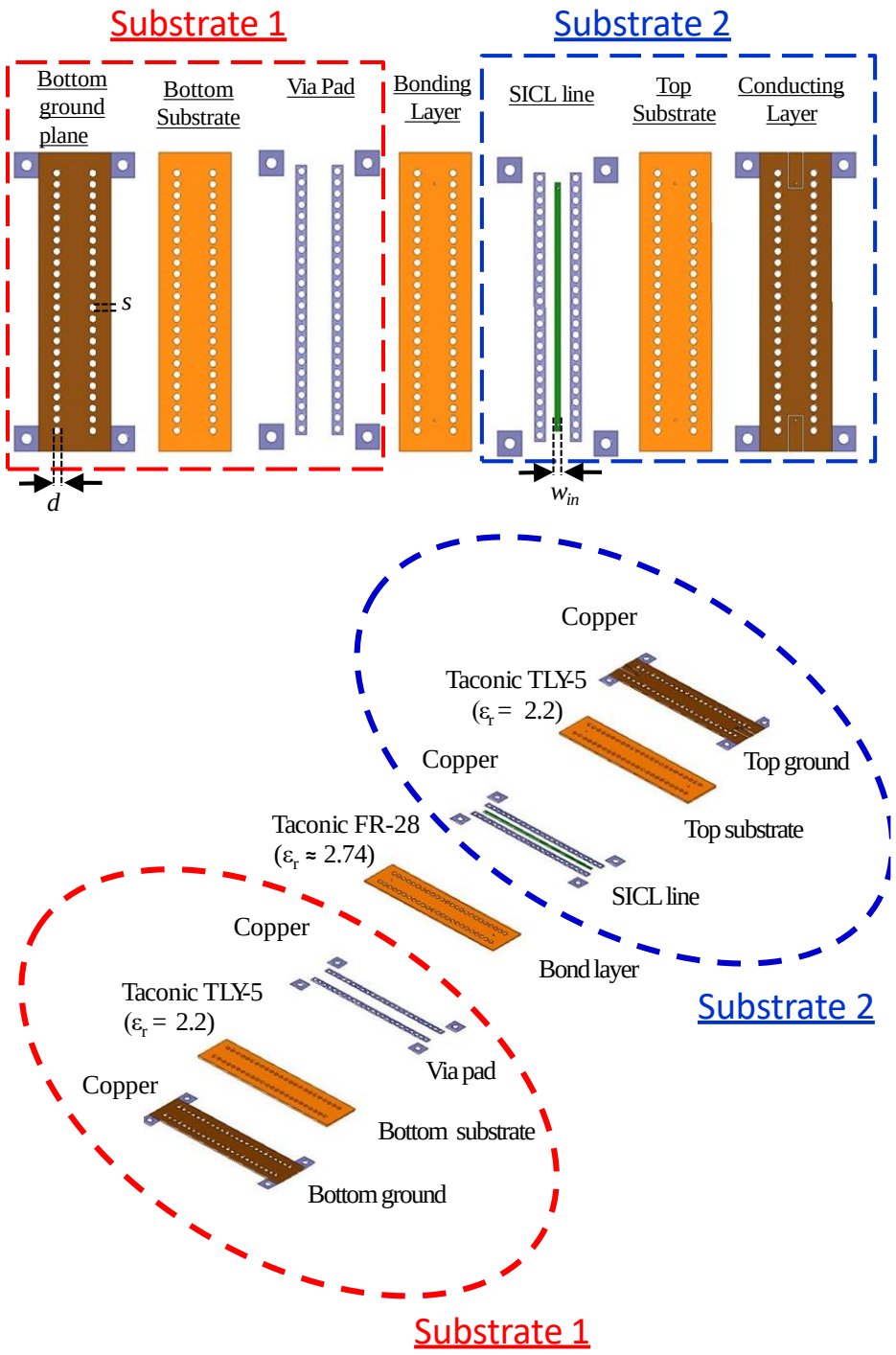



**Figure 2.2 :** Layer-wise stack up of SICL line for fabrication using multilayer-PCB technology.

On substituting equation (2.4) in (2.1) the characteristic impedance of a rectangular coaxial is derived as:

$$Z_o = \frac{376.62}{4\sqrt{\varepsilon_r}\left(\frac{w_{in}}{H_{sub}} + \frac{2}{\pi}\log\left(1+\coth\left(\pi\frac{g_s}{H_{sub}}\right)\right)\right)} \tag{2.5}$$

Where, $g_s$ is the gap between inner and outer conductor, $\varepsilon_r$ is the dielectric constant of substrate, $H_{sub}$ is the height of single layer of substrate, and $w_{in}$ is the width of the inner conducting strip of the rectangular coaxial line. The conducting sidewall is realized by rows of metallic vias which

are inherently inductive in nature contrary to the perfect electric conductor that is for a continuous sidewall. To compensate the effect, transverse resonance method (TRM) can be used in SICL line to conceptualize extended electrical width with conducting wall instead of the actual physical width with via wall. The relationship between effective width and physical dimension is as follows [178]

$$w_{\text{eff}} = A - \frac{d^2}{0.95s} \tag{2.6}$$

The equation (2.6) produces slight error as the height of substrate increase. A better empirical expression [178] which takes in to effect the $2H_{sub}/w_{eff}$ is given by

$$w_{\text{eff}} = A - 1.08\frac{d^2}{s} + 0.1\frac{d^2}{A} \tag{2.7}$$

Where, $A$ is the distance between two via rows that forms the outer conductor of this planar coaxial line, $d$ is the diameter of via and $s$ is the pitch or spacing between vias in a row. The gap between inner and outer conductor formed by cylindrical vias can be written in terms of $g_s$ as

$$g_s = \frac{A - w_{in}}{2} - 0.59\frac{d^2}{s} + 0.05\frac{d^2}{A} \tag{2.8}$$

Upon substituting $g_s$ derived in (2.8) in to (2.5) the characteristic impedance of substrate integrated coaxial relating to its physical and electrical parameter is derived as

$$Z_o = \frac{376.62}{4\sqrt{\varepsilon_r}\left(\frac{w_{in}}{H_{sub}} + \frac{2}{\pi}\log\left(1+\coth\left(\pi\left(\frac{A-w_{\text{in}}}{2H_{\text{sub}}} - 0.59\frac{d^2}{sH_{sub}} + 0.05\frac{d^2}{AH_{sub}}\right)\right)\right)\right)} \tag{2.9}$$

### 2.1.1 Results & Discussion

To validate the derived closed form expression in (2.9) for characteristic impedance of SICL line several full-wave simulations are performed and are compared with the derived formula as shown in Fig. 2.3. After varying physical parameters ($w_{in}$, $H_{Sub}$, $A$) and electrical parameter ($\varepsilon_r$) it is observed that the error between the characteristic impedance computed through the derived data and HFSS is less than 10%. Table 2.1 lists the parameters that are varied for conducting the analysis in Fig. 2.3. One of the important findings of this work is the dependence of characteristic impedance ($Z_o$) of SICL on the outer conductor width. In Fig. 2.4 the variation of $Z_o$ of SICL line as a function of ratio of inner to effective outer conductor ($W_{in}/W_{eff}$) is shown. The change in $Z_o$ is

**Table 2.1 :** Details of the analysis conducted in Fig. 2.4 to validate the accuracy of proposed closed form expression

| Fig. no | Parameter fixed (in mm) | Parameter varied |
|---|---|---|
| 2.3 (a) | $\varepsilon_r$ = 2.2, $A$ = 3, $H_{sub}$ = 0.25 | $w_{in}$ |
| 2.3 (b) | $\varepsilon_r$ = 2.2, $A$ = 3, $w_{in}$ = 0.44 | $H_{Sub}$ |
| 2.3 (c) | $\varepsilon_r$ = 2.2, $H_{sub}$ = 0.5, $w_{in}$ = 0.86 | $A$ |
| 2.3 (d) | $A$ = 3, $H_{sub}$ = 0.5, $w_{in}$ = 0.86 | $\varepsilon_r$ |

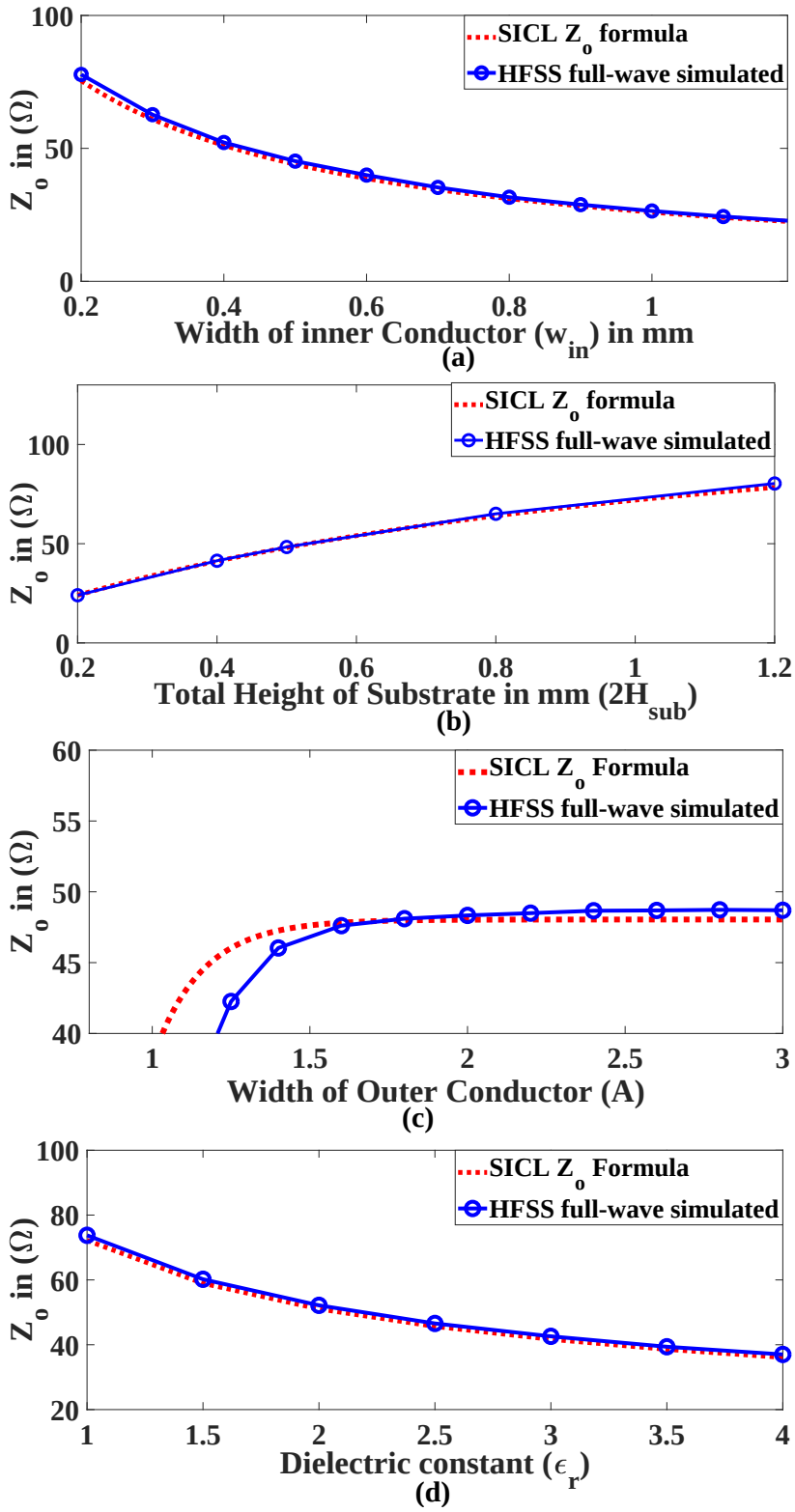



**Figure 2.3 :** Comparison of characteristic impedance of SICl line computed using proposed formula with the HFSS full-wave simulated data by varying (a) width of inner conductor ($w_{in}$) (b) total height of substrate ($2H_{sub}$) (c) width of outer conductor ($A$) (d) dielectric constant of substrate ($\varepsilon_r$).

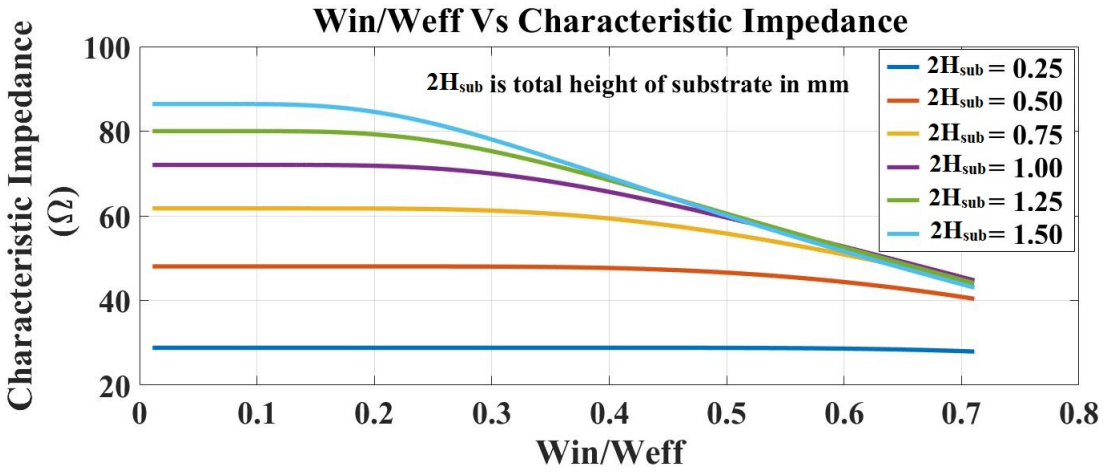



**Figure 2.4 :** Relationship between characteristic impedance and $W_{in}/W_{eff}$.

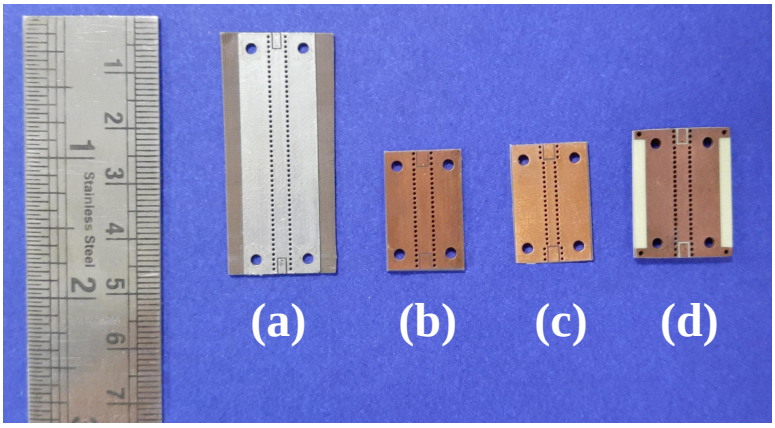



**Figure 2.5 :** Photograph of fabricated prototypes of SICL transmission lines with back to back GCPW transmission lines with different length, substrate thickness, dielectric constant and inner/outer conductor widths (a) $\varepsilon_r$ = 2.2, $H_{sub}$ = 0.25mm (b) $\varepsilon_r$ = 2.2, $H_{sub}$ = 0.508mm, $A$ = 3.5mm, $w_{in}$ = 1.3 (b) $\varepsilon_r$ = 2.2, $H_{sub}$ = 0.508mm, $A$ = 1.8mm, $w_{in}$ = 1.3 (d) (b) $\varepsilon_r$ = 3.55, $H_{sub}$ = 0.8mm, $A$ = 4mm, $w_{in}$ = 1.76 mm

minimal when SICL line is designed with a low profile substrate of thickness of 0.127mm. But as the substrate thickness increases, the outer-conductor width plays an important role in determining the characteristic impedance of SICL line. Four experimental prototypes of SICL transmission lines with back to back GCPW transmission lines have been fabricated with different length, substrate thickness, dielectric constant and inner/outer conductor widths as shown in Fig. 2.5. The first prototype 2.5(a) is developed using Taconic TLY-5 ($\varepsilon_r$ = 2.2, $\delta$ = 0.0009) with thickness 0.25 mm for the upper and lower substrate and Taconic FR-28 as prepeg ($\varepsilon_r$ = 2.8, tan$\delta$ = 0.0014). The computed width of inner conductor is 0.43 mm for 50Ω characteristic impedance with outer conductor width $A$ = 3mm is utilized to fabricate this SICL line. The full-wave simulated response generated using Ansys HFSS is confirmed by measuring the S-parameters of proposed prototype using Agilent N5234A vector network analyzer. The measured scattering parameters depicted in Fig. 2.6 (a) insertion loss is 4.02 dB at 40 GHz with return loss close to 10 dB. The next two prototypes in Fig.

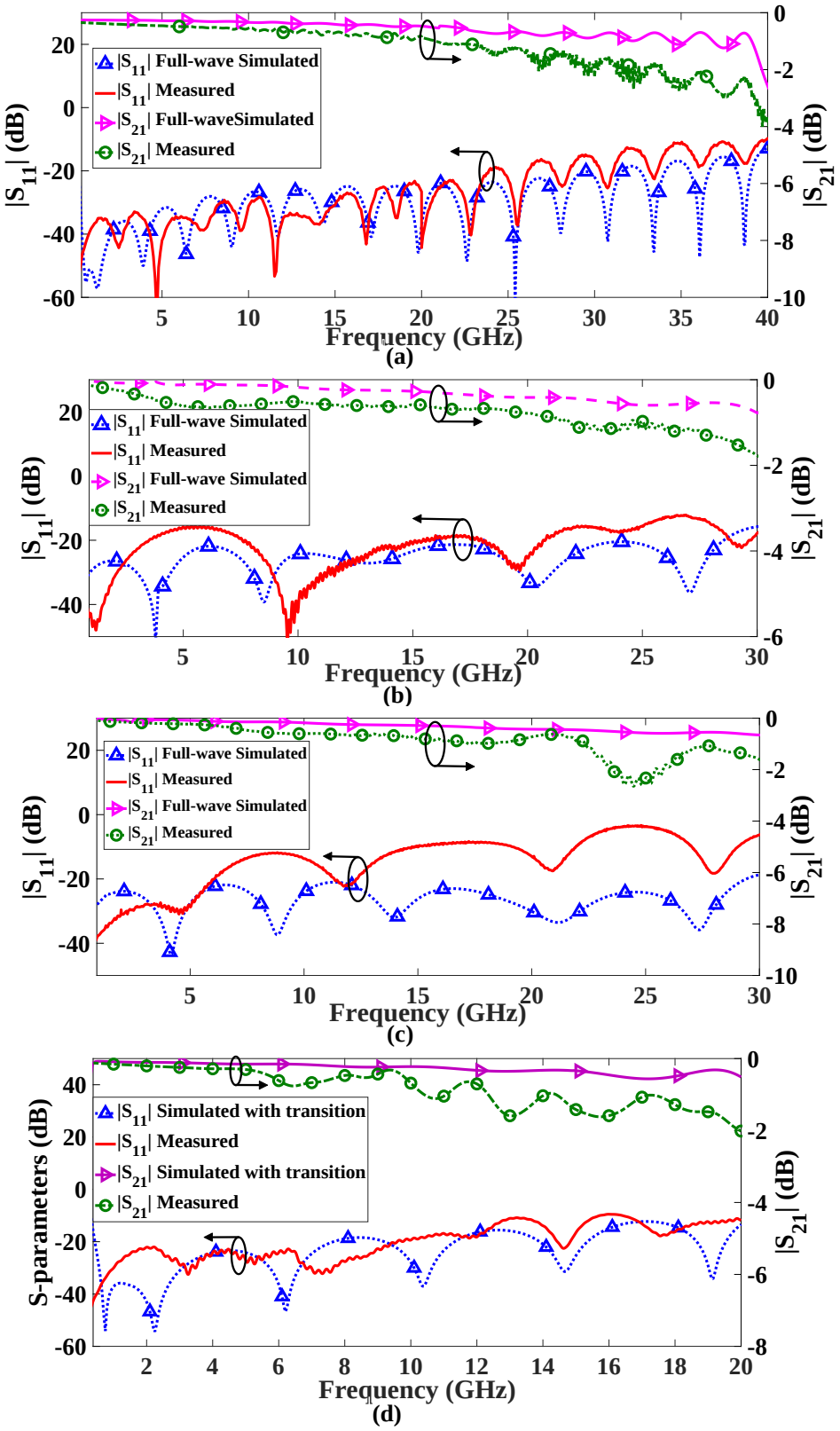



**Figure 2.6 :** Comparison between full-wave simulated and measured S-parameters of the 50 Ω SICL transmission line fabricated with different length, substrate thickness, dielectric constant and inner/outer conductor widths.

2.5(b) & (c) are fabricated using a pair of Taconic TLY-5A ($\varepsilon_r$ = 2.2, $\delta$ = 0.0009) substrate, each of thickness 0.508 mm is bonded using Taconic FR-28 prepreg ($\varepsilon_r$ = 2.74, tan$\delta$ = 0.0014) for different outer conductor width $A$ = 3.6 mm and 3.2 mm, respectively. The experimental prototypes are developed with inner conductor $w_{in}$ of 0.86mm, 0.83mm for outer conductor width $A$ = 3.6 mm and 3.2 mm, respectively. The characteristic impedance of SICL lines in 2.5(b) & (c) computed using (2.9) is 49.144Ω and 49.918Ω respectively. The measured S-parameters of the prototype with $A$ = 3.6mm demonstrates with less than 1.9 dB insertion loss at 30 GHz in Fig. 2.6 (b). In Fig. 2.6(c), the SICL line with outer conductor width $A = 3.2mm$ exhibits a measured insertion loss less than 2.2 dB up to 30 GHz. Finally, a SICL line design with Rogers 4003C ($\varepsilon_r$ = 3.38, tan$\delta$ = 0.0027) substrates each of thickness 0.8 mm. The fabricated prototype length 24mm has back to back GCPW transition A comparative study of experimentally tested SICL line with its full-wave simulated indicates a measured insertion loss of 2 dB with return loss better than 10 dB at 20 GHz in Fig. 2.6 (d) and affirms the proposed design methodology. In this work a closed form expression as a function of the physical and electrical parameters of SICL line is derived. The derived formula is in excellent agreement with full-wave simulated obtain using a FEM solver and all the fabricated experimental prototypes support the rigorous analysis conducted in section 2.1.

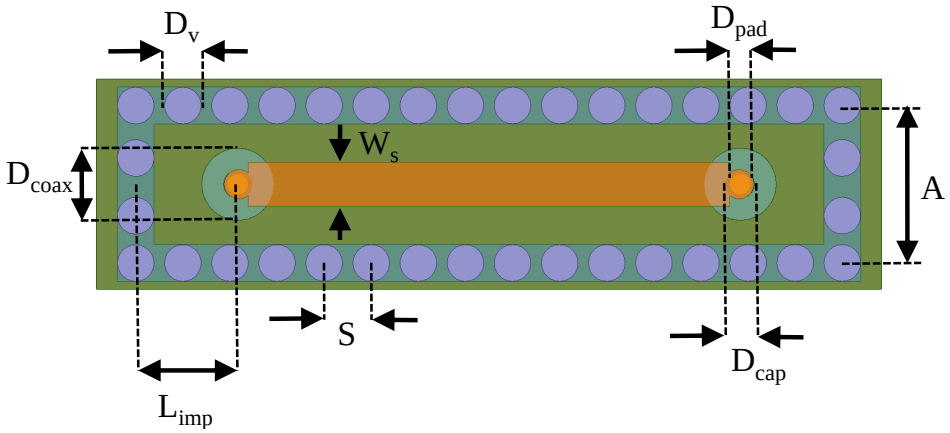
## 2.2 DESIGN OF WIDEBAND COAXIAL-TO-SUBSTRATE INTEGRATED COAXIAL LINE (SICL) PLANAR TRANSITION

In the previous section the design considerations and fabrication of SICL line were discussed. The following work attempts to address one the main challenges in utilization of SICL line, which is design of a broadband transition. A planar implementation of the male to female connection usually observed in conventional coaxial circuits is proposed in this work. Firstly, a 50 Ω SICL section is designed. The coaxial probe of equal impedance passing through a metallic via with slightly greater diameter is then connected to the inner conductor of SICL. The reactive component produced at the SICL-Coaxial junction is nullified by placing a short-circuit section at an optimal distance from it. The complete modeling of proposed planar transition is presented and the robustness of the design is validated for different dielectric constant and thickness. The fabricated back to back transition is easy to implement and exhibits wide-bandwidth making it worthy for practical applications.

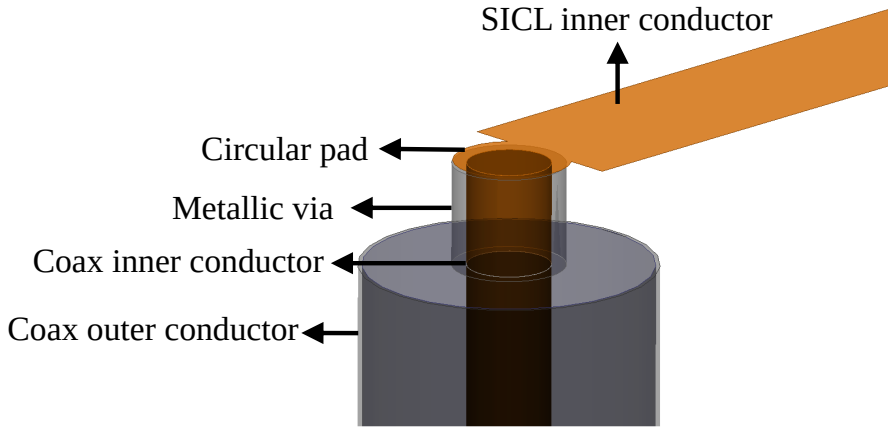
### 2.2.1 Working Principle of proposed SICL Transition

The layout of the proposed transition is depicted in Fig. 2.7(a). The designed model is a back to back coaxial-to-SICL transition. The SICL section comprises of a conducting strip rested between dielectric substrate with conducting planes covering it. Rows of metallic via connecting the top and bottom conducting plane are placed on both sides of the inner conductor. Further, rectangular metallic strip is enforced through the side vias to improve the performance of SICL section. Similar to a conventional coaxial line, SICL permits TEM mode of propagation. The SICL section is excited by a coaxial line in the configuration as portrayed in Fig. 2.7(b). The outer conductor of the coaxial cable is connected to the bottom ground plane. A hole of size $D_{coax}$, which is diameter of the coaxial dielectric is cut in the ground plane to facilitate connection between in the inner conductor of coaxial cable $D_{in}$ and inner conductor of the SICL section. As shown in Fig. 2.7(b) the inner conductor of the coaxial line is enclosed by a conducting metallic via of slightly greater diameter $D_{cap}$. An arrangement of this sort essentially replicates the male to female connector in planar form. The working principle of the proposed transition can be explained through its equivalent circuit representation as shown in Fig. 2.8. The coaxial connector with its inner conductor enclosed by metallic via is modeled as a $\pi$-network. The inductance offered by the inner conductor of coaxial cable is represented by an inductor $L_I$, and the inductance due to metallic via is given by $L_C$. The capacitance produced due to the coupling effect between probe

and the lower ground plate is modeled as $C_{IL}$, and $C_{CL}$ is the capacitance formed between the metallic via and lower ground plate. Similarly, $C_{IU}$ represents the capacitance created between the coaxial probe and upper ground plane, and $C_{CU}$ is the capacitance generated by metallic via with the upper ground plane. The connection between the coaxial line and inner conductor of the SICL can be modeled as a 90° bend in planar form. The reactive loading effect produced by this 90° bend is compensated by carefully adjusting the distance $L_{imp}$ from the 90° bend to the short circuited section, which is approximately $0.27\lambda_g$ in the proposed model. Optimal choice of $L_{imp}$ enhances impedance matching at the coaxial-SICL junction. The equivalent capacitance $C_{1eq}$, $C_{2eq}$ and inductance $L_{eq}$ of the proposed transition are derived from the Y-parameters of the optimized design after dembedding upto coaxial-SICL junction. The variation of the equivalent inductance and capacitances over the entire operating range is given in Fig. 2.8. Dimensions of the coaxial connector with dielectric constant $\varepsilon_r$ = 2.2 are calculated for an impedance of 50Ω. The impedance of the SICL section is a function of its substrate height to width of inner conductor ($2H/W_s$) [51]. Thus, a 50 Ω SICL section is designed by adjusting the width of inner conductor for a fixed substrate height (2H) of 1mm. Further, a circular pad is employed to enable the connection between SICL and coaxial probe to achieve broadband matching.




(a)




(b)

**Figure 2.7 :** (a) Top view (b) Enlarged view of the proposed back to back transition with dimensions.

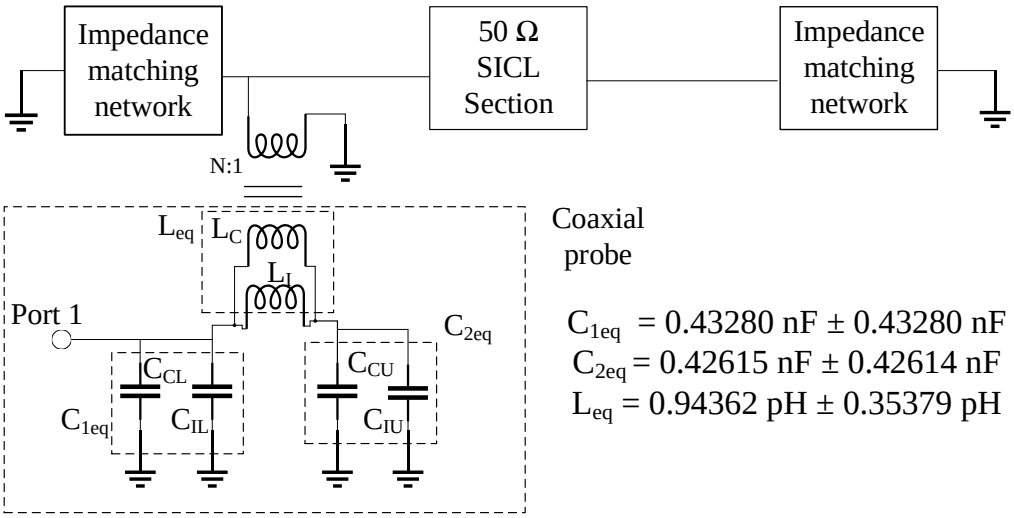



**Figure 2.8 :** Modeling of equivalent circuit for the proposed transition.

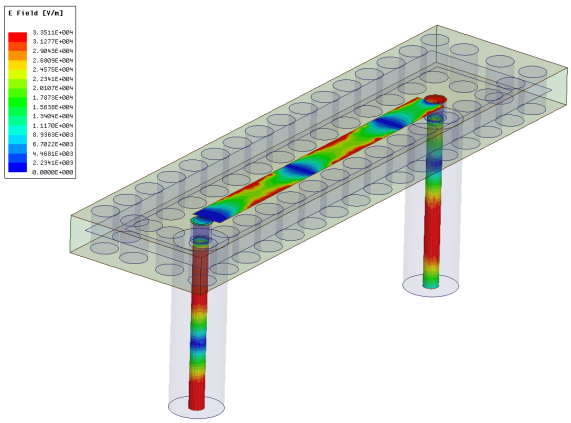


**Figure 2.9 :** Magnitude of E-field in the inner conductor of SICL and Coaxial line.

**Table 2.2 :** Dimensions of the proposed Back to Back Transition

| Parameter | Value (mm) | Parameter | Value (mm) |
|---|---|---|---|
| $D_{coax}$ | 0.69 | $D_{pad}$ | 0.56 |
| $D_v$ | 0.7 | $D_{in}$ | 0.4 |
| S | 0.9 | $W_s$ | 0.84 |
| $D_{cap}$ | 0.54 | $L_{imp}$ | 1.95 |
| A | 3 | H | 0.5 |

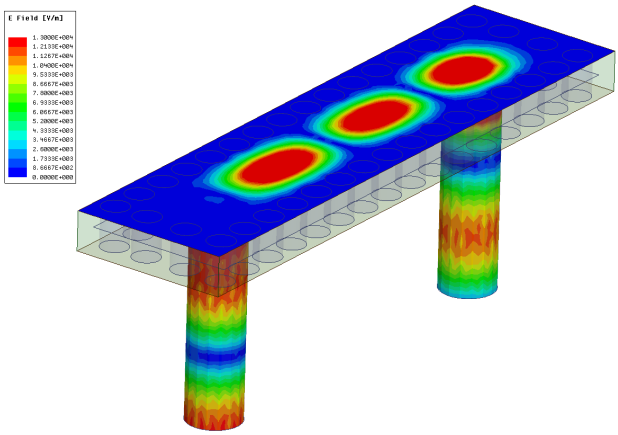


**Figure 2.10 :** Magnitude of E-field on the top ground plane of SICL and outer conductor of coaxial line.

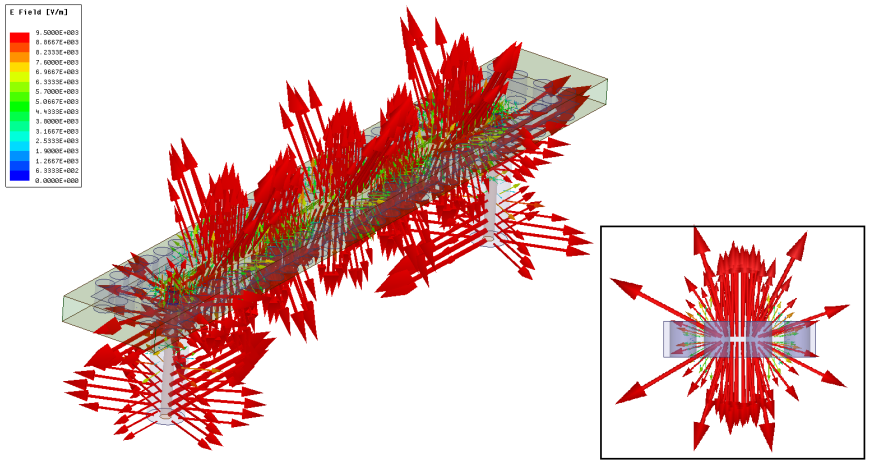


**Figure 2.11 :** E-field vector plot in the proposed back to back transition

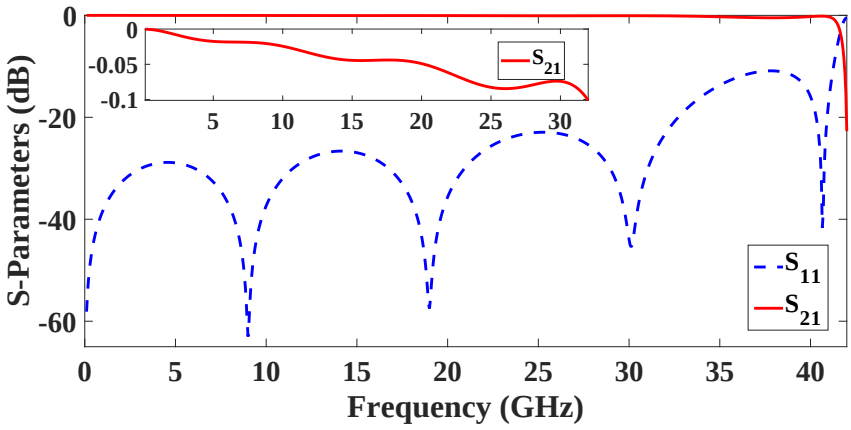



**Figure 2.12 :** S-parameters of the proposed back to back transition.

**Table 2.3 :** Width of SICL Inner conductor ($W_s$) for various Dielectric constant and height

| $\varepsilon_r$ | 2H (mm) | Impedance (Ω) | $W_s$ |
|---|---|---|---|
| 2.2 | 1 | 50 | 0.84 |
| 2.2 | 0.508 | 50 | 0.45 |
| 2.2 | 0.254 | 50 | 0.22 |
| 3.55 | 0.504 | 50 | 0.3 |

### 2.2.2 Results and Discussion

Two sheets of Taconic TLY-5, each having a thickness 0.508mm bonded using prepeg Taconic FR28 ($\varepsilon_r$ = 2.74, tan$\delta$ = 0.0014) is used to design the proposed coaxial to SICL transition. The dimensions of the proposed back to back to transition are listed in Table 2.2. The impedance matching between the coaxial line and SICL section can be clearly understood from the E-field distribution in the inner conductor of SICL and coaxial line as shown in Fig. 2.9. Magnitude of E-field distributed on the top conducting plane of SICL and outer conductor of coaxial probe have been shown in Fig. 2.10. Substrate integrated coaxial line operating as a coaxial line in planar from can be confirmed from the radially outward directed E-field vector as depicted in Fig. 2.11. In the inset, there is the E-field vector plotted across the cross section of SICL. The full-wave simulated scattering parameters of the proposed coaxial to SICL transition computed using Ansoft HFSS as shown in Fig. 2.12. The full-wave simulated S-parameters of the proposed transition confirms a broadband impedance matching of better than 20 dB for DC to 32.7 GHz with a very low insertion loss 0.1 dB throughout the band. The performance of the proposed transition is analyzed for various commercially available substrate thickness keeping other parameters of the transition unchanged. To maintain the 50 Ω impedance in SICL section $W_s$ is selected as shown in Table 2.3. A single dielectric layer of thickness H = 0.127 mm and H = 0.254 mm is considered for this analysis. The S-parameters of the back to back transition with different substrate thickness is depicted in Fig. 2.13. The return loss is better than 15 dB with insertion loss less than 0.8 dB is observed through full-wave simulation in the frequency range DC to 30 GHz. Further the robustness of the proposed transition is verified by validating it for a different dielectric constant and thickness. The SICL section is designed with Rogers R04003 ($\varepsilon_r$ = 3.55, $\delta$ = 0.0027) of single layer thickness H = 0.254

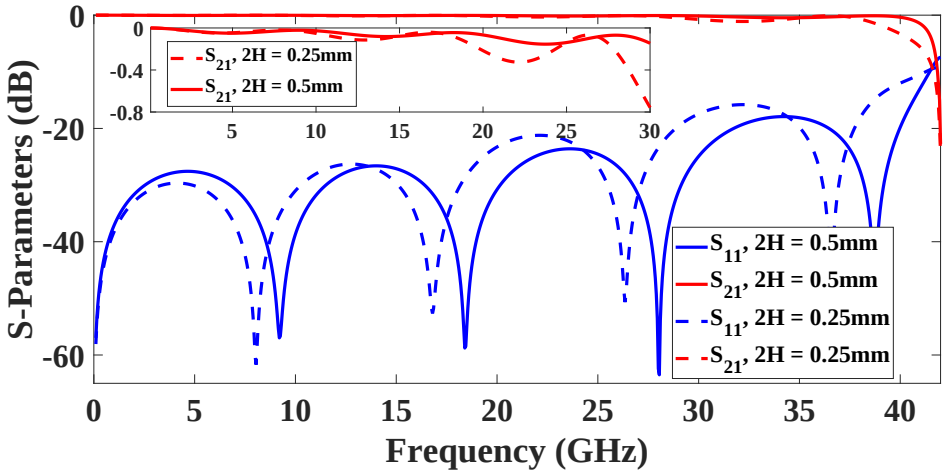



**Figure 2.13 :** S-parameters of the transition with variation in SICL section substrate thickness.

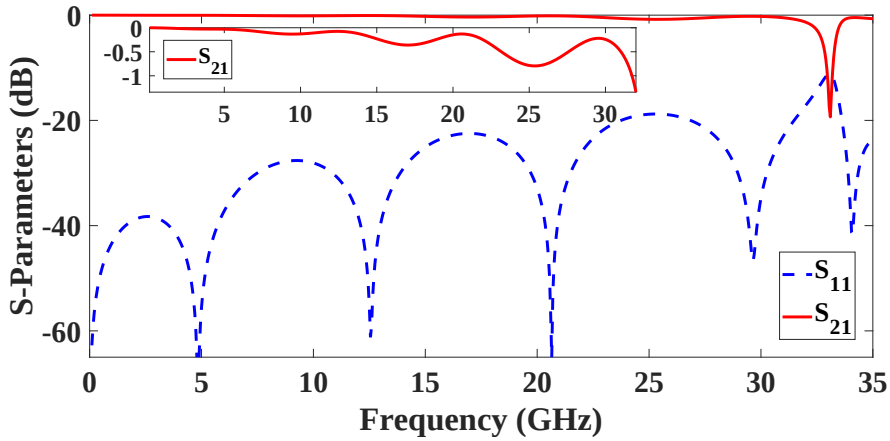



**Figure 2.14 :** S-parameters of the proposed transition with SICL section of Rogers R04003 ($\varepsilon_r$ = 3.55, $\delta$ = 0.0027)

mm. From Fig. 2.14, it can be observed that the designed back to back transition exhibits return loss better than 14.5 dB with insertion loss of at least 1.2 dB throughout the band from DC to 32 GHz. The increase in insertion loss can be accounted to the greater loss tangent of chosen substrate. Further, decrease in the cut-off wavelength is observed as a result of increase in dielectric constant ($\varepsilon_r$). This can be modified by changing the distance between the vias ($A$) or diameter of the via ($D$) [51]. It is to be noted that the results obtained are with parameters shown in Table 2.2 for a 50Ω SICL section. The performance of the transition can be further improved by optimizing the parameters of proposed transition for different dielectric constant and thickness.

## 2.3 DESIGN OF WIDEBAND MICROSTRIP TO SICL TRANSITION FOR MILLIMETER-WAVE APPLICATIONS

Transitions are commonly used to facilitate interconnection between different kinds of transmission lines. The main role of transitions is to minimize the mismatch between two transmission lines and provide seamless integration. SICL technology presents itself in a packaged form factor and requires transition for testing as well as integration with other technologies. It is desired that the designed transition has wide bandwidth to make use of the wideband TEM mode of wave propagation in SICL which can simultaneously support the operating bands of upcoming 5G communication and also provide backward compatibility to 3G/4G. In this section, the design and working principle of a wideband microstrip to substrate integrated coaxial line (SICL) planar transition for millimeter-wave applications is presented. In the proposed work, along with tapering of microstrip line, two triangular slots in the top ground plane are utilised to compensate for the discontinuity arising at the microstrip-SICL junction & minimize reflections over a wide bandwidth. Effortless integration of SICL with the widely used microstrip transmission line simplifies the feeding process of SICL based broadband antennas & microwave circuits.

### 2.3.1 Design of 50 Ω SICL section

The 50 Ω SICL section is fabricated by sandwiching a conducting strip between a pair of low loss Taconic TLY-5 ($\varepsilon_r$ = 2.2, tan$\delta$ = 0.0009) substrate each of thickness $H$ = 0.25 mm. This configuration is bounded by two rows of metallic vias connecting the top and bottom plane with a metallic sheet enforced through the vias to enhance the coaxial nature of SICL section as shown in Fig. 2.15(a). The characteristic impedance of the SICL is a function of substrate thickness to width of inner conductor ($2H/W_s$) ratio. Here the substrate thickness is fixed and width of SICL inner

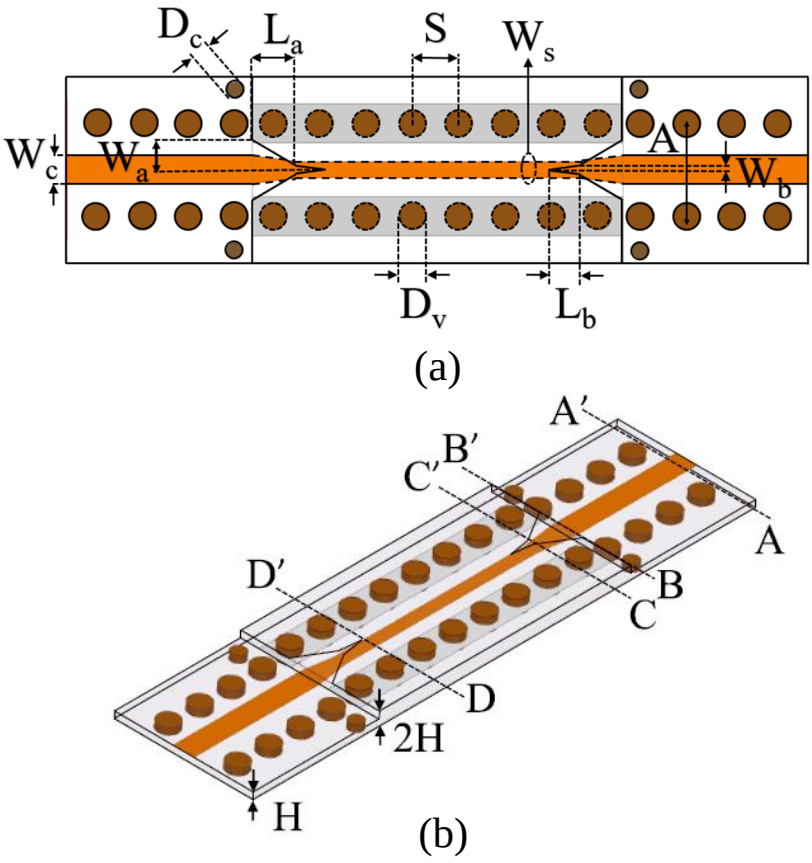



**Figure 2.15 :** Geometrical model of the proposed microstrip to SICL transition (a) Top-view (b) Isometric view.

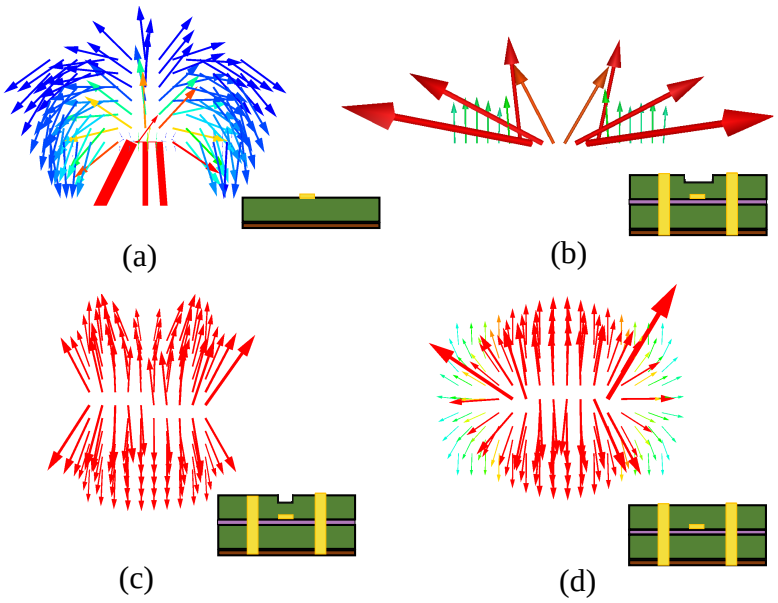
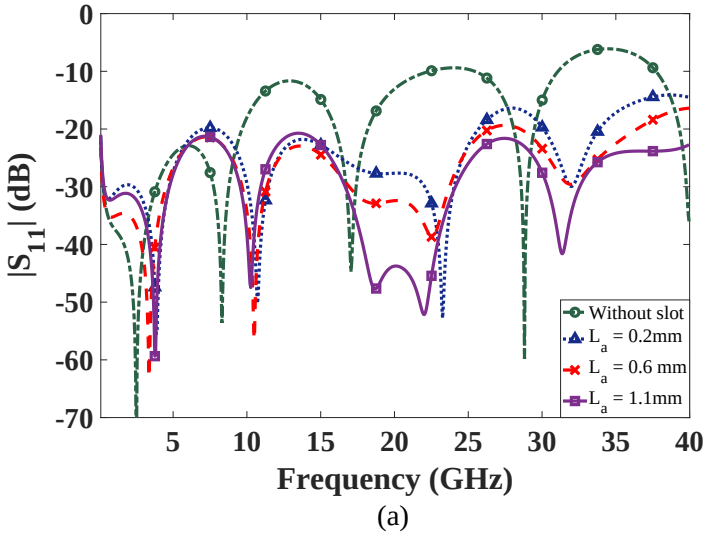
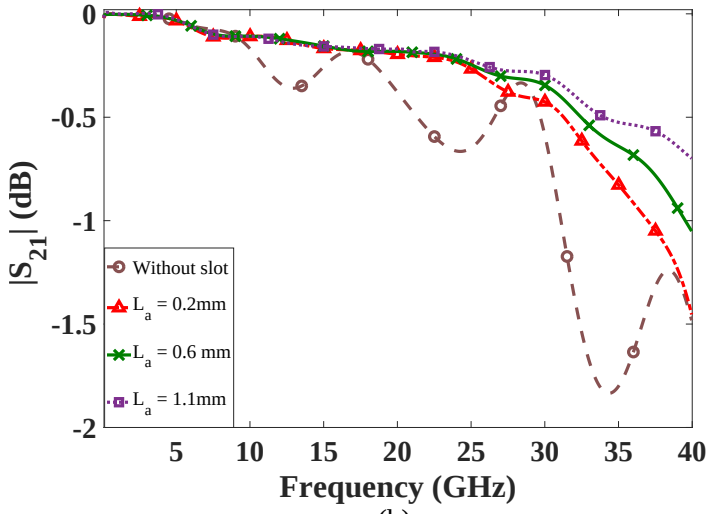


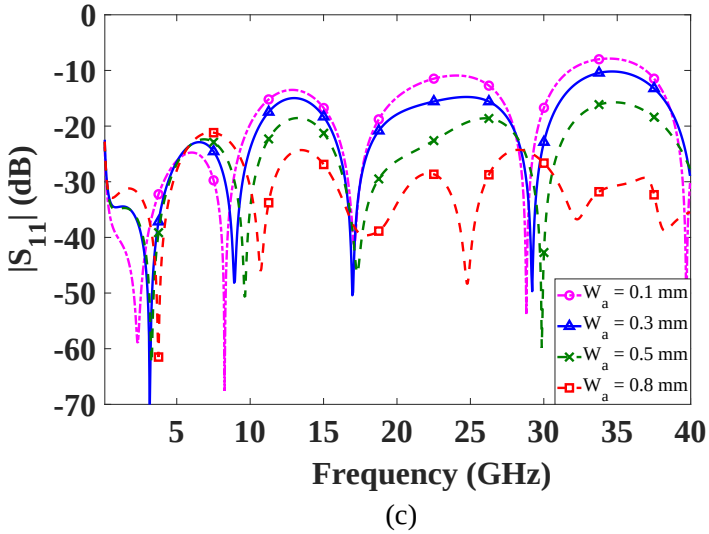

**Figure 2.16 :** Vector E-field across planes (a) AA' (b) BB' (c) CC' and (d) DD'.




(a)




(b)




(c)

**Figure 2.17 :** Study on performance of proposed microstrip to SICL transition with: Variation in slot length $L_a$ (a) Reflection coefficient (b) Insertion loss and, (c) Slot width $W_a$

**Table 2.4 :** Dimensions of the proposed 50 Ω microstrip to SICL transiton

| | $L_a$ (mm) | $L_b$ (mm) | $W_a$ (mm) | $W_b$ (mm) | $W_c$ (mm) | $W_s$ (mm) |
|---|---|---|---|---|---|---|
| $\varepsilon_r$ = 2.2* 2H = 0.5mm | 1.2 | 0.8 | 0.8 | 0.1 | 0.75 | 0.43 |
| $\varepsilon_r$ = 6.15 2H = 0.5mm | 1.4 | 0.4 | 1 | 0.14 | 0.36 | 0.18 |
| $\varepsilon_r$ = 10.2 2H = 0.5mm | 0.4 | 0.8 | 0.42 | 0.27 | 0.22 | 0.12 |
| $\varepsilon_r$ = 2.2 2H = 1.0mm | 1.8 | 1.2 | 1.1 | 0.3 | 1.58 | 0.9 |

*: Fabricated

conductor is optimized to obtain 50 Ω characteristic impedance. The diameter of via $D_v$ = 0.75mm and pitch between them $S$ = 1.25mm are selected so as to minimize electromagnetic wave leakage from the designed SICL section. The parameters $S$ & $D_v$ also play a crucial role in determining the TEM mode bandwidth of SICL. A wideband TEM mode propagation is ensured by controlling the operating frequency of next higher order mode $TE_{10}$ which is shown below $f_{TE_{10}}$ [51].

$$f_{TE_{10}} = \frac{c}{2\sqrt{\varepsilon_r}}\left(A - \frac{D^2}{0.95S}\right)^{-1} \tag{2.10}$$

### 2.3.2 Wideband mechanism of the proposed microstrip to SICL transition

At the microstrip−SICL juction two triangular slots of length $L_a$ and $L_b$ with widths $W_a$ and $W_b$ respectively are etched on the top ground plane as shown in Fig. 2.15(a) and (b). These two triangular slots of unequal length and width aid in mitigating abrupt variation in electric field caused at the junction of transition. The E-field along cross section AA′ of microstrip line is shown in Fig. 2.16(a). As expected there exists quasi-TEM based E-field from top microstrip line to bottom ground plane along with fringing fields. The proposed transition is devised by connecting a SICL section to a substrate truncated microstrip line. Due to the introduction of top conductor of SICL at the junction of transition, horizontal component of E-field ceases to exist, therefore a mismatch in field configuration before and after the transition degrades the overall performance. To mitigate that, a small slot in the top conductor is introduced which helps to orient the field from middle layer to either half of the top conductor as shown in Fig. 2.16 (b). As the slot is gradually tapered inwards, it is observed in Fig. 2.16(c) the E-field smoothly transitions in to a radially outward configuration. Finally, electric field with radially outward orientation similar to conventional coaxial line is observed across the cross-section DD′ of second triangular slot in Fig. 2.16(d). Further, the microstrip line is gradually tapered inwards over length $L_a$ in a linear fashion to facilitate broadband matching. The tapering of the line along with slots on the top plane of microstrip-SICL junction compensates for any discontinuity arised and minimizes reflections over a wide bandwidth. The copper plated via holes along the microstrip line prevent excitation of spurious parallel plate waveguide mode between the ground and top conducting line. Further, metallic vias of diameter $D_c$ = 0.5mm are placed along the microstrip and SICL boundary to mitigate wave leakage. The performance of microstrip to SICL transition with variation of slot length $L_a$ is studied in Fig. 2.17(a) and (b). The total length of slot in top conductor is kept approximately at $\lambda_g/4$. It is observed that the return loss and insertion loss at higher frequencies improve significantly with inclusion of proposed slot in top ground plane. In

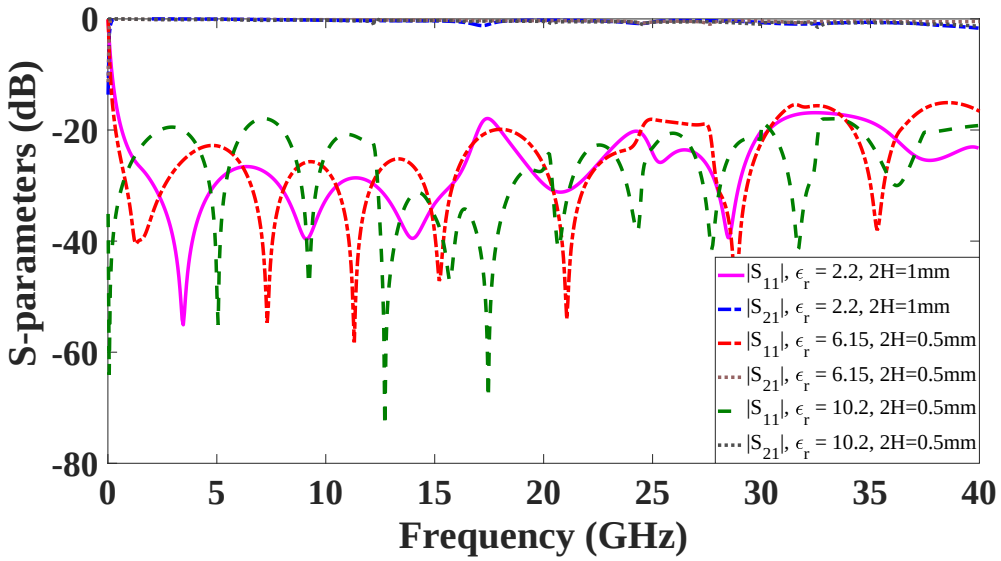
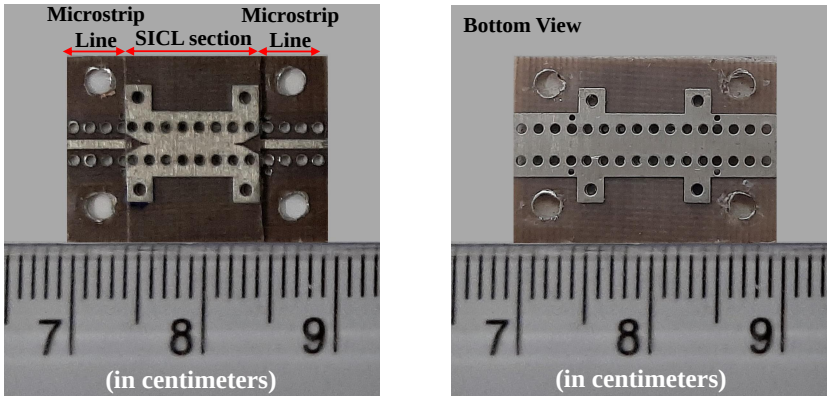



**Figure 2.18 :** Full-wave simulated S-parameters of proposed microstrip to SICL transition with change in dielectric constant and thickness.




(a) (b)

**Figure 2.19 :** Photograph of the proposed wideband microstrip to SICL transition (a) Top View (b) Bottom view.

Fig. 2.17(c), the performance of proposed transition with variation in width of slot in top conductor is investigated. The slot opening from the center of microstrip line ($W_a/2$) is estimated to $\lambda_g/20$ ($\pm 0.03\lambda_g$) for the electric field to progressively adapt to SICL based TEM configuration along the tapered section. The robustness of the proposed transition is confirmed by modeling it for different dielectric constant and thickness. The simulated results in Fig. 2.18 indicate a return loss of at least 18 dB in the operating band 0.51 GHz to 40 GHz with insertion loss less than 1.4 dB. Dimensions of the proposed transition for different dielectric constant and thickness is listed in Table 2.4.

### 2.3.3 Results and Discussion

The proposed back to back microstrip to SICL transition is tested with the help of a K-Type (2.4mm) end-launcher using Agilent E8361C PNA. Photograph of the fabricated prototype is depicted in Fig. 2.19. The back to back microstrip to SICL transition is simulated using Ansys

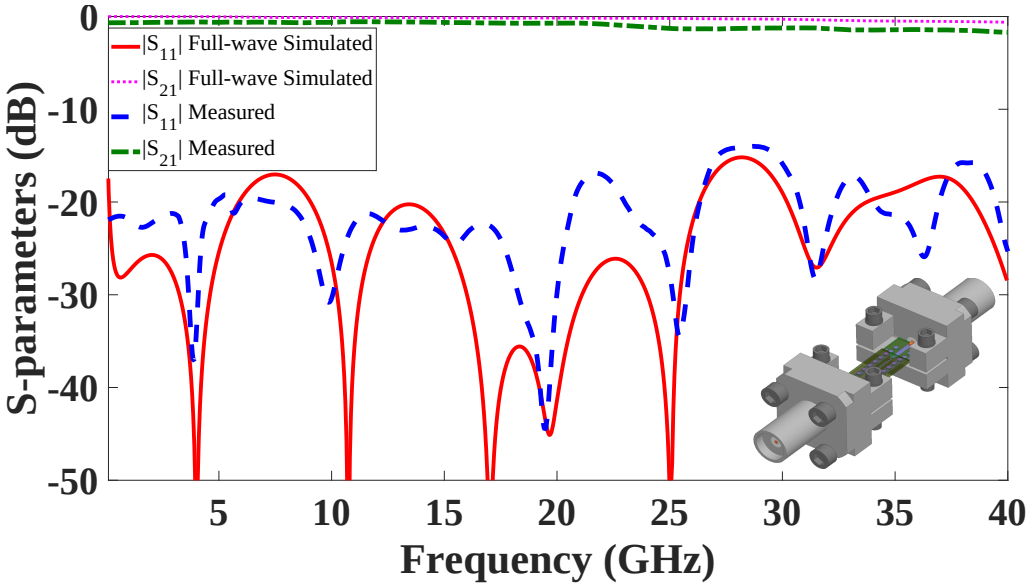



**Figure 2.20 :** Simulated and measured S-parameters of the proposed wideband microstrip to SICL transition.

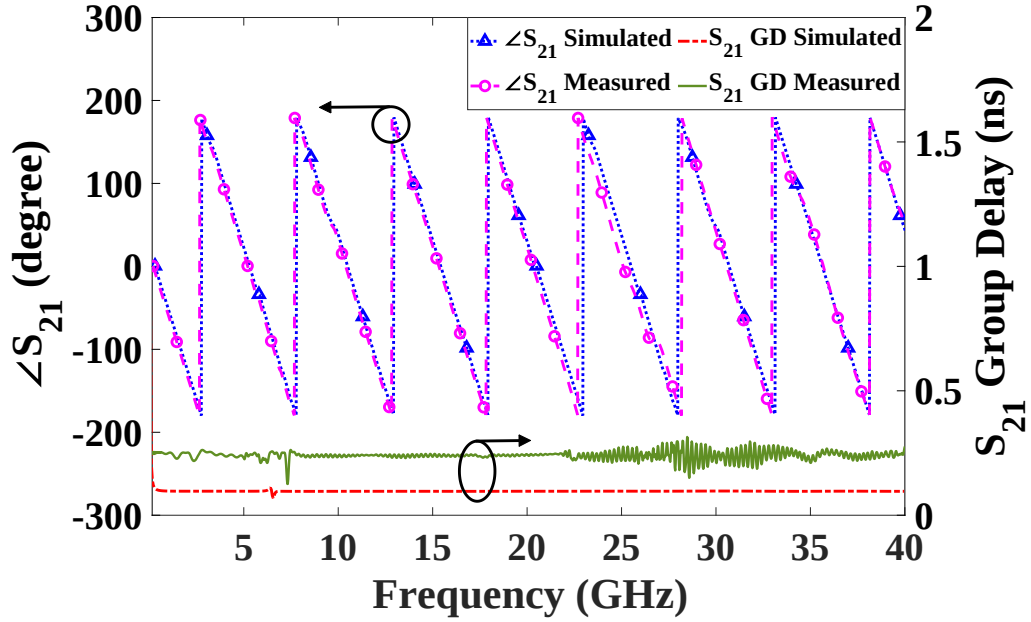



**Figure 2.21 :** Measured phase and group delay (GD) characteristics of the proposed microstrip to SICL transition.

HFSS and the simulation model is depicted in inset of Fig. 2.20. The measured results demonstrate wideband impedance matching with better than 14 dB return loss and less than 1.78 dB insertion loss up to 40 GHz (19 dB bandwidth up to 20 GHz with insertion loss less than 0.71 dB) as illustrated in Fig. 2.20. It is to be noted the measured insertion loss takes in to account the two K-type connectors used to facilitate the testing of the proposed prototype. The discrepancy between measured and simulated results can be attributed to fabrication tolerances and air gap in bonding

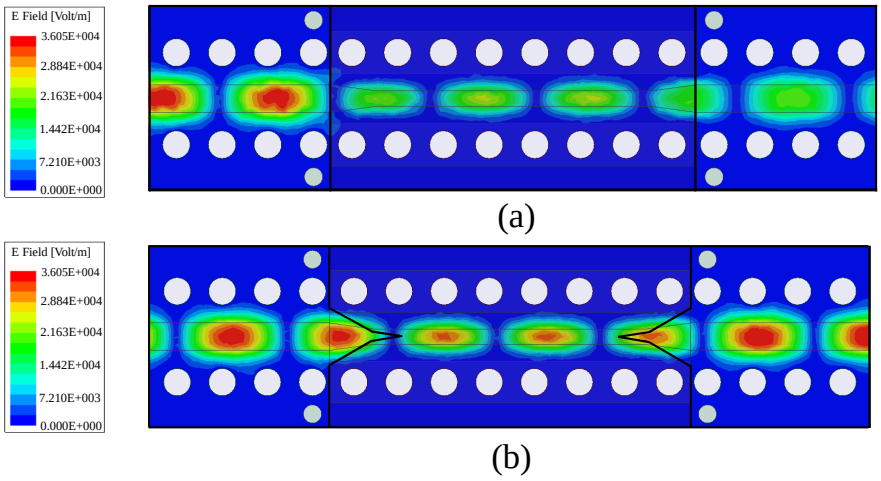



**Figure 2.22 :** Magnitude of electric field in bottom ground plane at 35 GHz (a) Without proposed slots etched in top ground (b) With proposed slots etched in top ground.

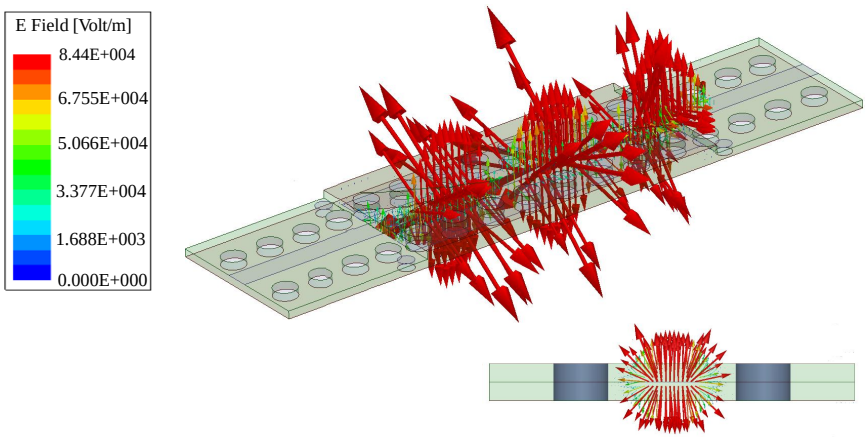



**Figure 2.23 :** Vector electric field plot along the length of SICL section of the proposed back to back transition at 28 GHz

the two substrate layers. From Fig. 2.21 it is observed the proposed slot in top conductor does not cause any abrupt variation in phase and supports wave propagation with a low peak to peak group delay variation of 0.16 ns. The variation of E-field at microstrip-SICL junction at higher frequencies can be analyzed through Fig. 2.22. The magnitude of electric field without slots on the top ground plane as depicted in Fig. 2.22(a) causes reflections due to abrupt variation of impedance at microstrip-SICL junction. Whereas, the proposed slot in top ground plane as portrayed in Fig. 2.22(b) helps to transform the E-field uniformly from quasi-TEM mode of microstrip to broadband TEM mode of SICL minimizing mismatch between these two transmission lines. Further, in Fig. 2.23 the similarity of the radially outward electric field vector in the SICL section with its non-planar counterpart affirms coaxial nature of SICL in planar form. The performance of designed back to back microstrip to SICL transition is compared with previously reported state of the art SICL transitions in Table 2.5.

**Table 2.5 :** Comparison of the proposed microstrip to SICL transition with previously reported works

| Ref. | Technique | Frequency Range | Max. $\lvert S_{21} \rvert$ (dB) | Blind Via |
|---|---|---|---|---|
| [26] | SICL to Coaxial | DC to 32.7 GHz | $\leq 0.1^*$ | Yes |
| [41] | SICL to Coaxial | 12 to 14 GHz | N.M | Yes |
| [179] | SICL to Waveguide | 71 to 78 GHz | N.M | Yes |
| [24] | SICL to CPW | DC to 40 GHz | $\leq 2$ | Yes |
| [12] | SICL to CBCPW | DC to 13 GHz | $\leq 1.72$ | Yes |
| [42] | SICL to SIW | 6.7 to 7.42 GHz | $\leq 1.4$ | Yes |
| **This work** | SICL to Microstrip | DC to 40 GHz | $\leq 0.71$ dB up to 20 GHz<br>$\leq 1.78$ dB up to 40 GHz | No |

*: Simulated Data,
NM: Not Mentioned

## 2.4 A WIDEBAND DC ISOLATED SUBSTRATE INTEGRATED COAXIAL LINE TRANSITION FOR SYSTEM INTEGRATION

In the previous works design and realization of wideband transitions have been explored. Often for active circuits there is a stringent need for DC block at the input & output as shown in Fig. 1.9. This DC block protects the test equipment & without interfering with the fixed bias point. Further, in literature so far the SICL based transitions and components are proposed using thin substrates ($\leq$0.5mm). Moreover, the popularly used SICL to grounded coplanar waveguide (GCPW) requires additional blind via and suffers from higher parasitics associated with increase in substrate height as well as fabrication complexity. In this work, a wideband DC isolated substrate integrated coaxial line (SICL) transition for thick substrates is analyzed. The planar transition is devised utilizing a substrate truncated microstrip line as a transition to SICL section. Trapezoidal slots etched on the top ground plane aid in improving the transition characteristics over a wide bandwidth. Development of DC isolated transition for the self-packaged & electromagnetically shielded SICL simplifies integration of active components for superior performance of the communication system.

### 2.4.1 Design of a wideband SICL based transition working in DC to 20 GHz.

The three dimensional view of the proposed transition is shown in Fig 2.24(a). The SICL section comprises of an inner conductor with metallic vias running along its length. The pitch and diameter of metallic vias are chosen such that they eliminate crosstalk with neighboring circuits and keep the first higher order mode above 25 GHz [51]. These metallic plated through holes are connected to each other through top and bottom conducting ground plane forming the outer conductor of this planar coaxial line. The required characteristic impedance of SICL is realized by selecting the appropriate width of inner conducting strip and outer conductor by using the equation (2.9). The TEM based SICL section is fed by a quasi-TEM based microstrip line. A microstrip line designed on substrate with thickness $T$ is connected to a SICL section of total substrate thickness $2T$ as shown in 2.24(b). This topology facilitates the microstrip line and SICL inner conductor to remain on same plane and eliminate the need for blind via. The inner conductor is tapered along length ($D_1$) to ensure impedance matching. It is to be noted as the substrate height increases the discontinuity between microstrip line and SICL section increases. The length of taper ($D_1$) needs to be selected appropriately to get wide band impedance matching. The tapered slot in the top ground plane aids the E-field to progressively adapt to the TEM based SICL mode and

helps in improving the insertion loss and return loss characteristics as discussed in section 2.3. The same has been affirmed from Fig. 2.25. The full-wave simulated wideband transition demonstrates return loss better than 14 dB and insertion loss less 1.4 dB up to 20 GHz as shown in Fig. 2.26 (20 dB return loss bandwidth with less than 0.4 dB insertion loss up to 10 GHz). The upper bound on operating frequency is mainly dependent on the discontinuity at the junction since it plays a greater role at higher frequency. The loss characteristics of the transition are studied in Fig. 2.27. It observed that the losses for this shielded structure fed by a small section of microstrip line are within acceptable range.

### 2.4.2 Analysis of a DC isolated wideband SICL transition

A DC isolated wideband SICL transition is devised by integrating a printed interdigital capacitor shown in Fig. 2.28. Capacitance of an interdigital capacitor depends on number of fingers (n), length of overlap between fingers, width ($W_{idc}$), gap between the fingers ($G_{idc}$) and dielectric constant ($\varepsilon_r$) on which the interdigital capacitor is printed. The equivalent capacitance is derived from Z-parameters of the optimized design after de-embedding up to interdigital capacitor in Ansys HFSS. The effect on return loss of transition with variation in number of fingers is shown in Fig. 2.29(a). From Fig. 2.29(b), it can be observed for an interdigital capacitor printed on substrate

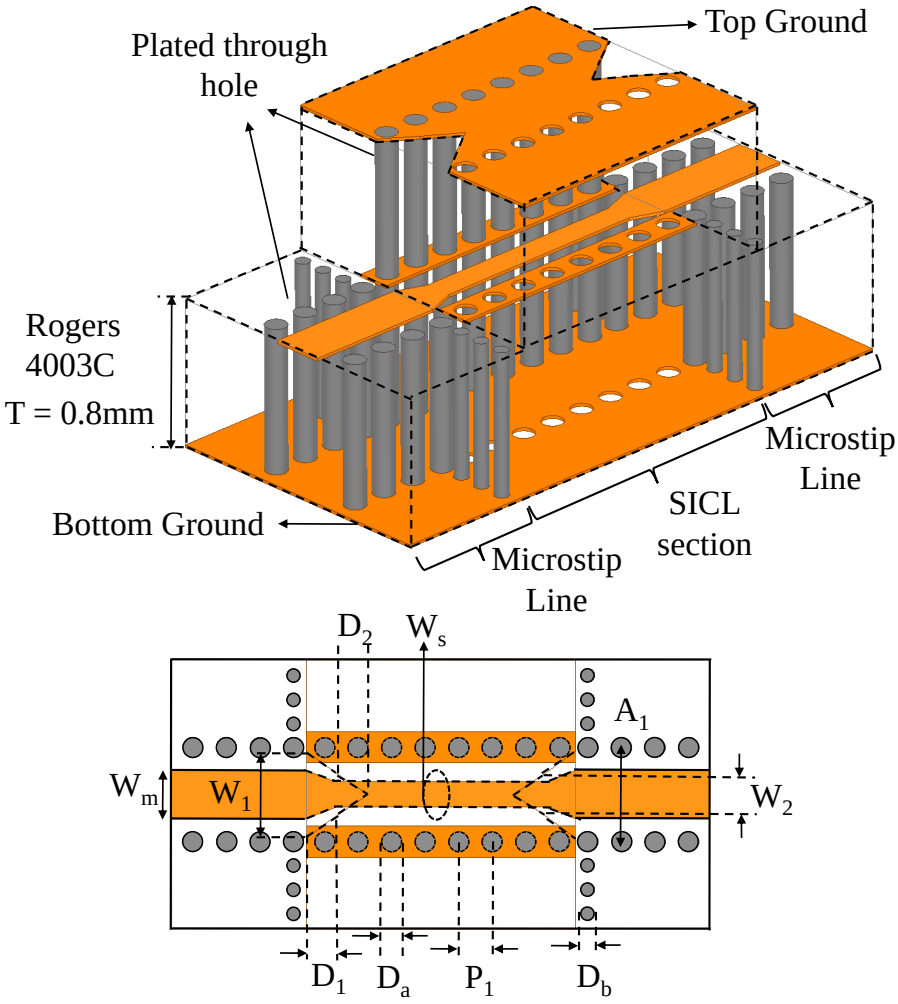



**Figure 2.24 :** Modeling of planar SICL transition (a) Three dimensional view (side vias not shown for clarity) (b) Top View with dimensions

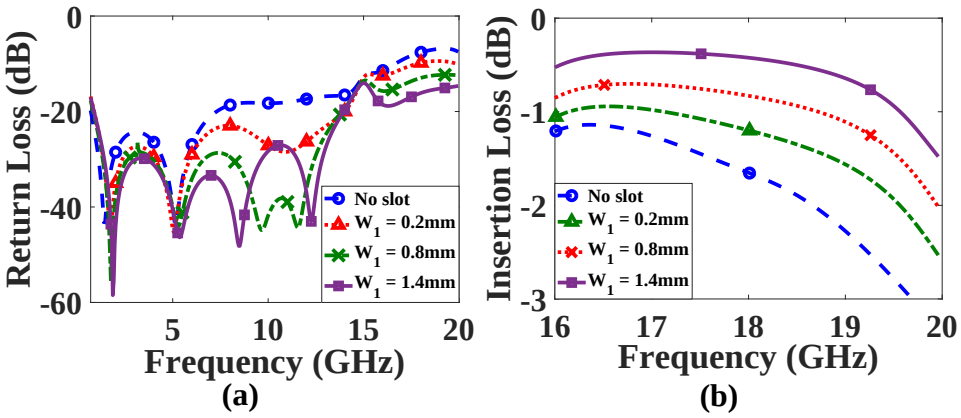



**Figure 2.25 :** Effect of slot opening ($W_1$) on performance of the transition (a) Return loss (b) Insertion loss

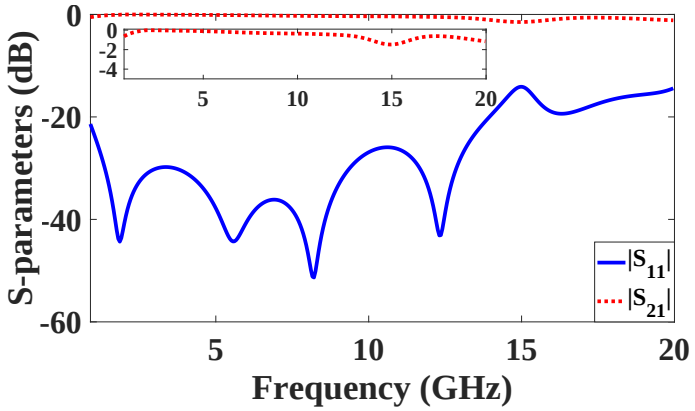



**Figure 2.26 :** Full-wave simulated S-parameters of the designed wideband SICL transition.

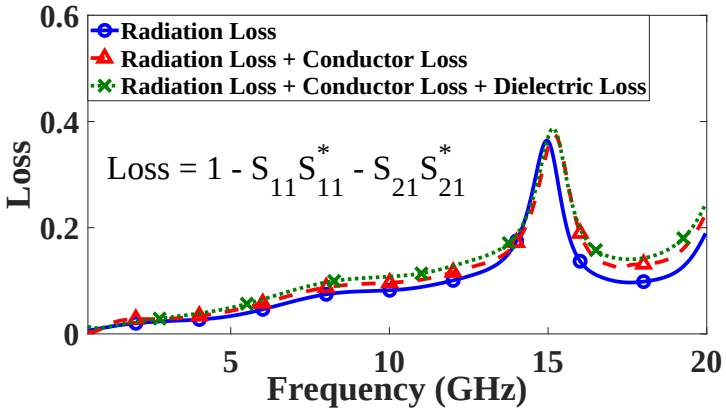



**Figure 2.27 :** Study on effect of different types of losses in wideband SICL transition

with ($\varepsilon_r$) = 3.55 and height 0.8mm, a capacitance between 0.23 pF to 0.38 pF can be achieved for a fixed $W_{idc}$ = 0.12mm and $G_{idc}$ = 0.13mm. However, the upper bound on achievable capacitance

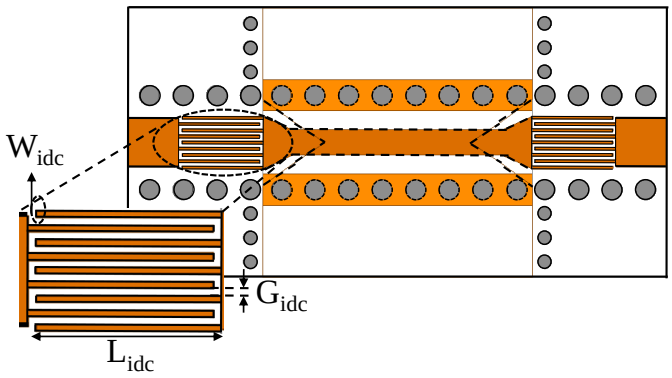



**Figure 2.28 :** Geometrical layout of the proposed DC isolated wideband transition with dimensions: $A_1$ = 3.5mm, $D_1$ = 1.1mm, $D_2$ = 1.2mm, $D_a$ = 0.75mm, $D_b$ = 0.5mm, $G_{idc}$ = 0.12mm, $L_{idc}$ = 3mm, $P_1$ = 1.25mm, $T$ = 0.8mm, $W_1$ = 2.4mm, $W_2$ = 1.6mm, $W_{idc}$ = 0.12mm, $W_m$ = 1.78mm, $W_s$ = 0.94mm

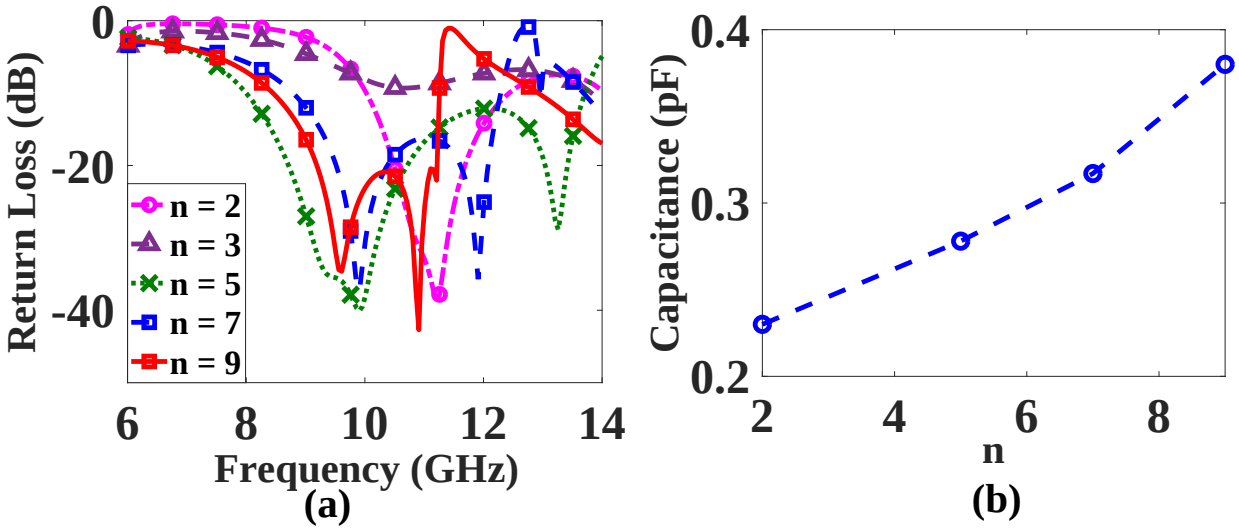



**Figure 2.29 :** Parametric analysis (a) Effect on return loss with variation in number of fingers (n) in interdigital capacitor embedded in microstrip line. (b) Equivalent capacitance of the interdigital capacitor.

is dependent of PCB fabrication limitation. It can be seen that the transition provides a fractional bandwidth of 22.3% with simulated insertion loss less than 0.54 dB utilizing 9 fingers (0.38 pF at 10 GHz).

### 2.4.3 Results and Discussion

The proposed DC isolated SICL transition is fabricated using a pair of Rogers 4003C ($\varepsilon_r$ = 3.55, tan$\delta$ = 0.0027) substrates each of thickness 0.8 mm. Photograph of the fabricated prototype depicting the top and bottom view is shown in Fig. 2.30. The proposed two port DC isolated SICL transition is tested with SMA end-launchers using Agilent E5071C vector network analyzer. In Fig. 2.31, measured return loss is better than 15 dB in the frequency range of 9.09 GHz to 11.38 GHz, equivalently 22.37% fractional bandwidth is observed. The mean insertion loss in this band is less than 1.2 dB. The loss characteristics of the wide band DC isolated transition are compared

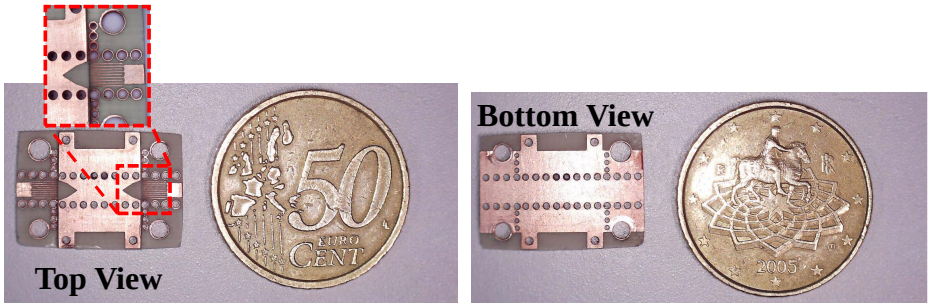



**Figure 2.30 :** Photograph of the fabricated DC decoupled SICL transition: (a) Top view (b) Bottom View

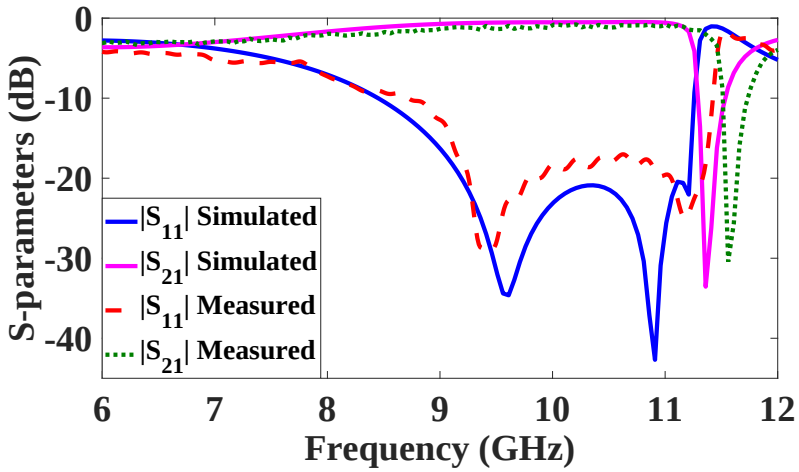



**Figure 2.31 :** Comparision between measured and full-wave simulated S-parameters of the proposed DC isolated SICL transition.

with its simulated counterpart in Fig. 2.32(a). The measured loss are well within the acceptable range of 0.24 and deviation between measured and simulated is due to the additional losses by SMA end launchers accounted in measurement. Group delay performance of the proposed wideband transition operating up to 20 GHz and DC decoupled transition are recorded in Fig. 2.32 (b). A measured group delay variation 0.28 nsec with maximum group delay peak of 0.44 nsec is observed. To affirm the DC isolation property of the proposed wideband transition the magnitude of electric field distribution is plotted as shown in Fig. 2.33. Near DC, it can be observed that almost no E-field exists and at 10 GHz good impedance matching is observed along with good shielding provided by the metallic vias running along the inner conductor. To understand the slight bandwidth enhancement in measured results as shown in Fig. 2.31, a sensitivity analysis is carried out. In this analysis, the parameters controlling the capacitance of interdigital capacitor namely, $G_{idc}$, $L_{idc}$, and $W_{idc}$ are randomly varied within the range of $\pm$0.5mm. It can be observed from Fig. 2.34 that the bandwidth of transition is dependent on fabrication tolerance. However, utilization of printed interdigital capacitors has better flexibility in terms tuning to the required capacitance than using the standard chip capacitors with fixed capacitance. Moreover, errors resulting from mounting and soldering chip capacitors can also be avoided by using of printed interdigital capacitor.

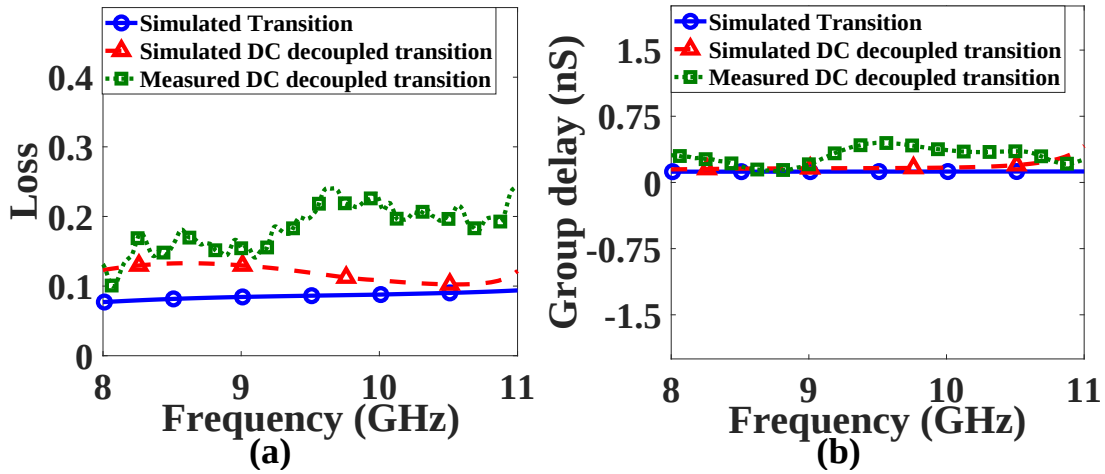



**Figure 2.32 :** Investigation on wideband DC isolated SICL (a) Loss characteristics (b) Group Delay

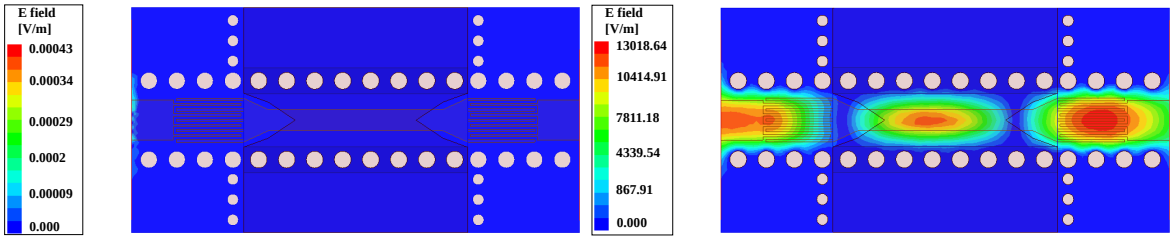



**Figure 2.33 :** Magnitude of electric field distributed in DC isolated SICL transition: (a) Near DC (b) At 10 GHz

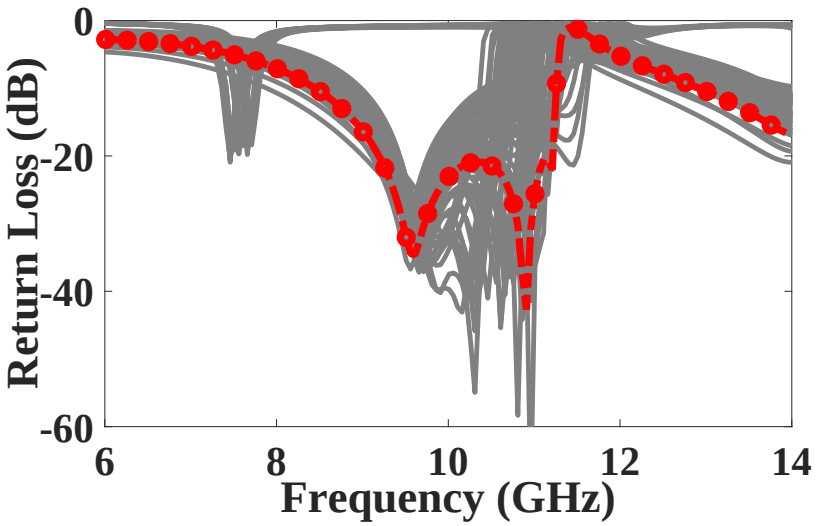



**Figure 2.34 :** Sensitivity analysis of proposed DC decoupled SICL transition with random variation (± 0.5mm) in $G_{idc}$, $L_{idc}$ and $W_{idc}$

## 2.5 CONCLUSION

This chapter discusses the design and fabrication of SICL transmission line and various types of transitions. Firstly, a closed form equation is derived to compute the characteristic impedance of SICL line as function of its physical and electrical parameters. Several experimental prototypes with different physical length, dielectric constant, thickness and outer conductor width have been tested and found in accordance to the proposed analysis. The second part of the chapter deals with design and analysis of different types of transitions to feed a SICL line. A two-port back to back transition for coaxial to SICL has been designed and discussed in detail. The proposed transition replicates the combination of male to female connector in a planar form. The proposed transition shows wide-bandwidth up to 32.7 GHz. Further, the effect of change in dielectric constant and thickness is investigated. The low-loss broadband planar implementation of the transition makes it an attractive alternative for many wide-band millimeter wave circuits.
The next work deals with a wideband transition which eliminates the need for blind via to feed the inner conductor of SICL line. The design and analysis of wideband microstrip to SICL transition is presented and the proposed transition is fed by a substrate truncated microstrip line. The effect of tapered line along with double triangular etched slot in top ground plane to reduce reflection at microstrip - SICL junction is investigated. A wideband 14 dB impedance bandwidth from DC to 40 GHz is achieved with insertion loss less than 1.78 dB (19 dB bandwidth up to 20 GHz with insertion loss better than 0.71 dB) using the proposed methodology. Further, the adaptability of transition for different dielectric constant and thickness is evaluated. Utilization of substrate truncated microstrip line eliminates the need of blind via thereby reducing the fabrication complexity. The superior integration capability of planar microstrip line with electromagnetically robust broadband monomode TEM operating SICL promotes the utilization of SICL for various practical applications.
Finally in this chapter the working of a DC isolated wideband planar SICL transition is presented. A printed interdigital capacitor embedded in substrate truncated microstrip line is utilized to design the planar DC isolated wideband transition to SICL section. A fractional bandwidth of 22.37% with DC blocking property is achieved in 9.09 to 11.38 GHz operating band. A comprehensive study carried out on loss and group delay characteristics of the DC isolated transition affirms good functionality in the operating band. Utilization of SICL based DC isolated transition, aids in integration of active components with RF front end in a compact form factor with good electromagnetic compatibility.

The studies presented in this chapters helps in design of SICL based circuits and systems for modern wireless communications system.

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