2
Transistors

The term "Transistor" was coined by J. R. Pierce, indicating the combination of the abbreviations for transconductance/transfer and varistor [Madou, 2011]. Transistors are key component for silicon technology, as well as for the emerging technologies. It is a three-terminal device, used widely for amplification and switching purposes in electronic circuits.

2.1 BACKGROUND

The first three-terminal electronic amplifying vacuum-tube device ("Triode") was invented by Lee De Forest in 1906 [Wikipedia, 2014], which enabled the amplified radio technology and long-distance telephony, but with the drawback of high power consumption. Twenty years later, in 1926, the first patent was filed on a field-effect transistor by J. E. Lilienfeld, which was granted in 1930 [Edgar, 1930]. However, none of Lilienfeld' patents and publications show the prototype of a working transistor [Streetman and Banerjee, 2005].

In 1947, John Bardeen and Walter Brattain at Bell Laboratories observed that a device composed of a crystal of germanium and two gold point contacts, generated higher power at the output compared to the applied input power [Bardeen and Brattain, 1948; Shockley, 1949]. After the successful demonstration of the point-contact transistor, William Shockley expanded the knowledge of semiconductors by explaining the physics behind the operation of point-contact transistors. The successful demonstration of the point-contact transistor had a large impact on the development of useful transistors. William Shockley, John Bardeen and Walter Houser Brattain were awarded a Nobel Prize in Physics for their scientific contribution and the discovery of the transistor effect. However, it was the discovery of a bipolar junction transistor. In 1953, the first high frequency surface-barrier germanium transistor was developed by Philco [Bradley, 1953].

The first silicon-based transistor was developed at Bell Laboratories in 1954, followed by the first commercial production of silicon transistors at Texas Instruments. In 1960, while solving the problem of the surface defects, the MOSFET was invented by Dawon Kahng and Martin Atalla, which played a huge role in the development of electronics for real-life systems such as analog and digital communication systems [Streetman and Banerjee, 2005]. The field-effect transistors are discussed in detail in the following Section.

2.2 FIELD-EFFECT TRANSISTORS

A field-effect transistor (FET) is a voltage-controlled device with major application in switching and amplification. It is a four-terminal device *i.e.* source, drain, gate, and body (or substrate which is usually connected to the source, *i.e.* grounded for n-channel devices, and connected to highest voltage for p-channel devices). The most commonly used FET is one with silicondioxide (SiO_2) as gate dielectric, called MOSFET. There are two types of MOSFET depending upon the formation of the channel between source and drain terminals namely, the n-channel MOSFET and the p-channel MOSFET. For n-channel MOSFETs, electrons are the charge transport carriers, the source and drain regions are heavily doped with n-type impurities

and a p-type substrate is used. For p-channel MOSFETs, holes are the charge transport carriers and the source and drain regions are heavily doped with p-type impurities on an n-type substrate. The schematic structure of an n-channel MOSFET is given in Figure 2.1.

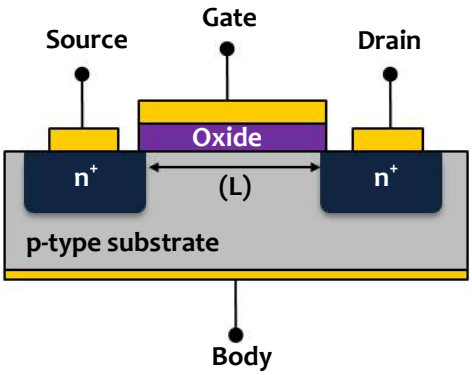

Figure 2.1 : Schematic structure of an n-channel MOSFET

The n-channel MOSFET consists of a lightly doped p-type silicon (Si) substrate which acts as the substrate and the semiconductor. The heavily doped n-regions are diffused or implanted in the substrate, forming the source and drain regions. The source and drain regions are separated from each other by a distance (L) which is called the channel length, which is a very important parameter in terms of technology advancement. W is the channel width and is defined as the extent of the transistor perpendicular to the direction of the L. The highly conducting gate is separated from the substrate by SiO_2 which acts as an insulator.

2.2.1 Operation

The switching of the MOSFET device depends on the applied gate voltages. The operation of the MOSFET is explained here with the help of applied voltages which is shown using the energy band diagrams in two directions, one in the direction perpendicular to the gate (gate, oxide, and bulk) and the other in the lateral direction (drain, semiconductor, and source). The gate in combination with the dielectric and the semiconductor form a metal-oxide-semiconductor (MOS) capacitor. The charges can be induced and controlled in the semiconductor by applying the gate voltage. Here the operation of n-channel MOSFETs is explained where the bulk and source terminals are grounded. Depending on the polarity and magnitude of the applied gate voltage, accumulation, depletion, and inversion of the channel occurs, all of which are schematically shown in the energy band diagram of the MOS structure in Figure 2.2.

Figure 2.2(a) shows the energy diagram when no external voltages are applied. The work function of the metal is $q\phi_M$, the work function of the semiconductor is $q\phi_S$ (the energy difference between the semiconductor Fermi level and the vacuum level), and silicon bulk energy is $q\phi_F$ (the difference between the intrinsic E_I and Fermi level in the bulk of semiconductor E_{FS}) [Streetman and Banerjee, 2005], which is given as,

$$\phi_F = {}^{kT}/_{q} \ln\left({}^{N_A}/_{n_i}\right) \tag{2.1}$$

where N_A is the acceptor doping concentration, and n_i is the intrinsic concentration of carriers. The work function of the metal (semiconductor) is defined as the energy that an electron requires to move outside of the metal (semiconductor) Fermi level. It is important to note that

when no gate bias is applied, the energy bands are flat. Hence, this condition is called flat band condition. The ideal case is considered here, where $\phi_M = \phi_S$, *i.e.* $\phi_{MS} = 0$.

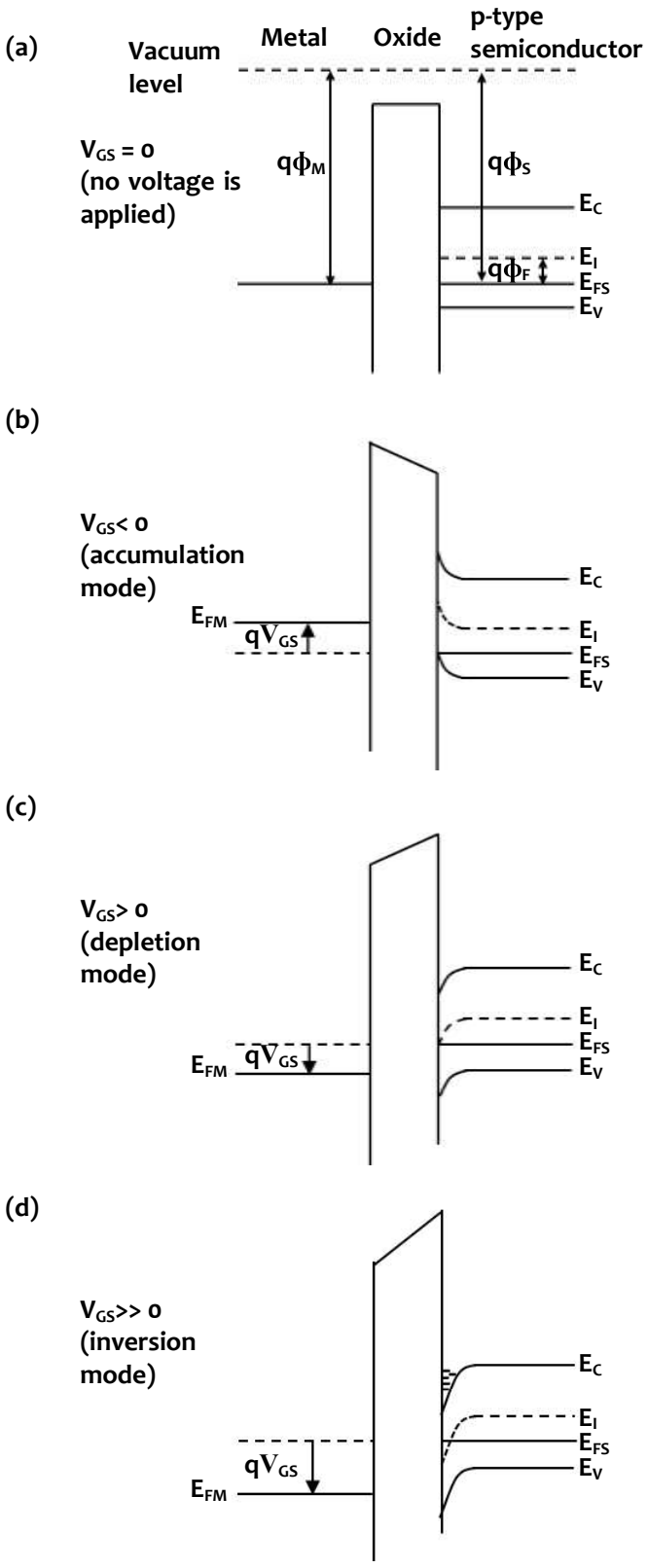

Figure 2.2 : Energy-band diagram showing various Modes of Operation in a MOS Device

When negative gate voltage is applied (V_{GS}< 0), negative charges are supplied in the gate metal contact, inducing opposite polarity charges in the capacitor (negative charges near semiconductor/dielectric interface), which results in accumulation of equal amount of positive charge-carriers (holes) in the semiconductor near the interface. This is called the accumulation mode, and the energy band bending for the same is shown in Figure 2.2(b). The Fermi level of metal move in the upward direction by amount qV_{GS}, due to which the valence band of p-type semiconductor moves more closer to the Fermi level, thereby making the surface more p-type than bulk of the semiconductor material. The potential barrier between source and drain is more in this region, and hence no current flow takes place.

When positive gate voltage is applied (V_{GS}> 0), positive charges are supplied in the gate, inducing opposite polarity charges in the capacitor (positive charge near semiconductor/dielectric interface). This repels the positive charge-carriers from the semiconductor leaving negative ionized acceptors in the semiconductor, which are negatively charged. This condition is called depletion region because the holes are depleted from the semiconductor near the interface forming a depletion region. The energy band diagram for this mode is shown in Figure 2.2(c). The Fermi level of metal moves in downward direction by amount qV_{GS}, due to which the valence band of p-type semiconductor moves far away from the Fermi level, thereby making the surface neither p-type nor n-type, though negative fixed acceptor ions are available (N_A^-).

If gate voltage is further increased, the energy bands of semiconductor move more in downward direction (the band bending ~ $2\phi_F$), inverting the surface of semiconductor towards n-type. This condition is called inversion mode, for which the energy band diagram is shown in Figure 2.2(d). Due to inversion, a conducting channel of electrons is formed between source and drain electrodes of MOSFET devices.

The potential barrier diagram for lateral direction *i.e.* from source to drain is given in Figure 2.3. As it can be seen in the Figure 2.3(a), there is a potential barrier in the bulk region for electrons to move down from source to drain, when no gate-source voltage and drain-source voltage is applied. When gate-source voltage is applied such that it is greater than the threshold voltage ($V_{GS} \geq V_{th}$), the barrier height decreases to nearly zero as can be seen in Figure 2.3(b). The barrier between source and drain decreases to zero, and electron transfer is possible between source and drain when small drain-source voltage is applied such that V_{DS}> 0. V_{th} is the threshold voltage and it is defined as the minimum applied gate-source voltage at which enough charge-carriers are created in the channel, resulting in the flow of drain current between source and drain terminals.

If no gate-source voltage is applied (V_{GS} = 0), there is no change in the barrier height, even if a high drain-source voltage of V_{DD} is applied (see Figure 2.3(c)). The potential barrier diagram for electrons in a completely ON, n-channel MOSFET device (V_{GS} = V_{DS} = V_{DD}) is shown in Figure 2.3(d), where electrons can easily move from source to drain electrode depending on applied drain-source voltages. The drain-source current increases almost linearly for V_{GS}> V_{th} and V_{GS} - V_{th}> V_{DS} and it is given as,

$$I_{DS} = \mu_n \cdot C_d \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{th}) \cdot V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (2.2)$$

where μ_n is the charge-carrier mobility of electrons in the channel and C_d is the capacitance of the dielectric, which is of SiO_2 in case of MOSFET. This mode of operation is called as linear/triode region. For a given applied gate-source voltage (V_{GS}> V_{th}), the drain current reaches saturation when V_{GS} -V_{th}< V_{DS}. This region of operation is called saturation regime and it is given as,

$$I_{DS} = \mu_n . C_d . \frac{W}{2L} . (V_{GS} - V_{th})^2 \quad (2.3)$$

The working principle of p-channel MOSFET is similar to that of n-channel MOSFET, however polarity of applied voltages, and currents are opposite. The n-channel MOSFET devices are more preferable than p-channel MOSFETs because the mobility of electrons is greater than that of holes in silicon.

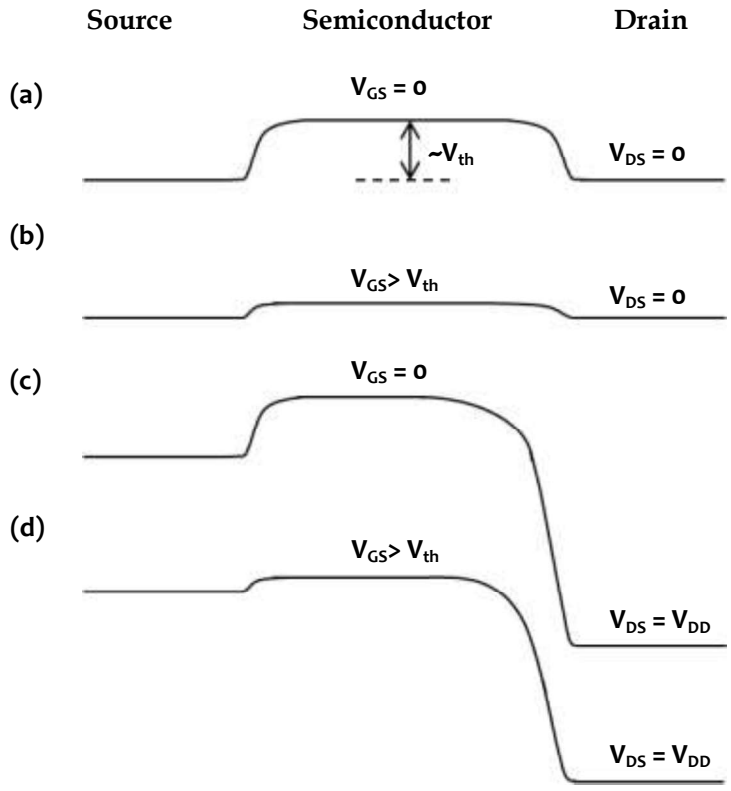

Figure 2.3 : Potential Barrier diagram between Source, Semiconductor, and Drain for Different Applied Voltages [Source : Sze and Ng, 1969]

2.2.2 Evolution of Transistors

MOSFET is the core discrete element of modern Integrated Circuits (ICs). An IC is a complex circuitry, which is a combination of many devices/components such as diodes, transistors, capacitors and resistors in a single chip. ICs are used widely in almost all electronic systems such as computers, laptops, mp3 players, calculators, televisions, mobile phones, and radios. One of the initial ideas given for the development of ICs was by W. Jacobi in 1949 [Wikipedia, 2014]. However, the first IC was demonstrated by J. Kilby in the year 1958 at Texas Instruments [Kilby, 1964]. J. Kilby was awarded a Noble Prize in Physics in year 2000, for the useful discovery of IC. Since then, a lot of research and development activities have happened for the improvement of ICs.

The complexity of an IC is measured in terms of the number of transistors present in that chip and a continuous increase has been observed over the years, since 1971. Figure 2.4 shows the increase in the number of transistors per chip from few thousands in 1971 to billions in year 2014. It has increased from 2,300 in year 1971 to more than 10^{10} [Wikipedia, 2014] in last three decades, following the trend which was predicted by Gordon Moore [Moore, 1998], according

to which the number of transistors in a chip doubles after each technology node which is approximately every two years.

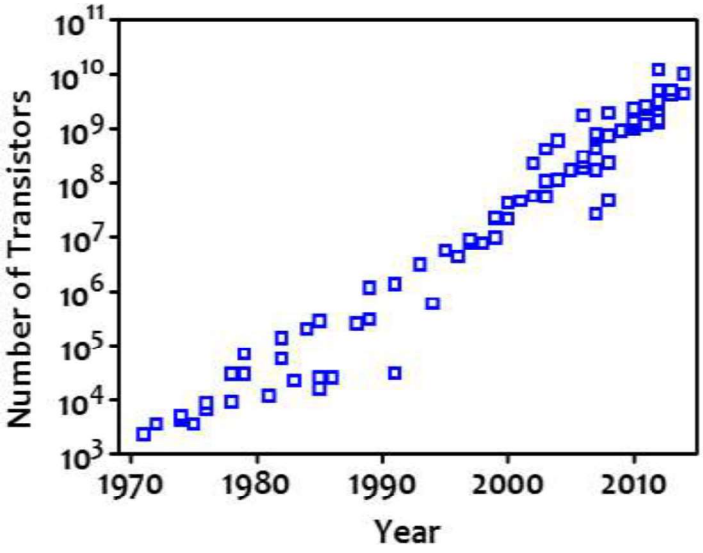

Figure 2.4 : Increase in the Number of Transistors in an Integrated Chip since 1971 (Data Points are Taken from [Source : Wikipedia, 2014]

The main factor behind the development of ICs is the possibility to reduce the size of transistors, specifically, the gate length of the transistors which is also referred as the minimum feature size in terms of process technology. The gate length has been reduced from 10 μm in year 1971 to 20 nm in 2014, allowing higher density of transistors to be fabricated in an IC. The development of the technology in terms of the reduction of the size of the transistor over years is depicted in Figure 2.5.

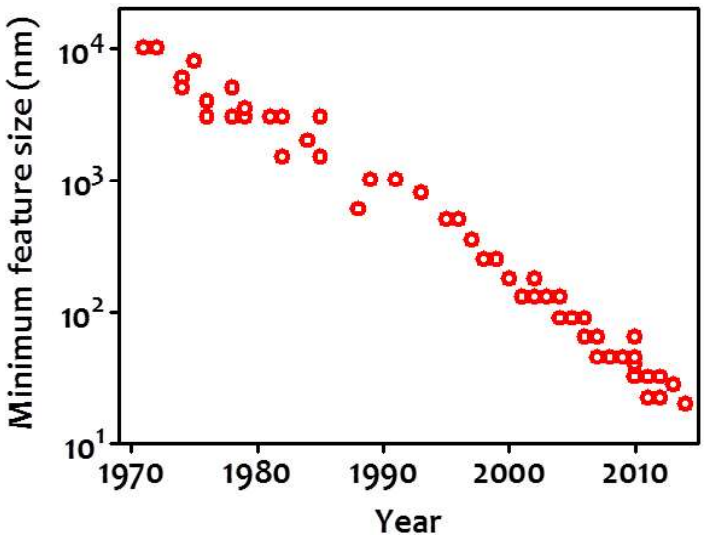

Figure 2.5 : Reduction in the Dimension of the Transistors since 1971 (Data Points are Taken from [Source : Wikipedia, 2014]

In the meantime, the requirement of low-cost, large-area, flexible electronics compelled many scientists and researchers to search for an alternative to crystalline silicon which lead to the development of TFT technology. Various TFT technologies based on poly-Si, a-Si:H, and organic semiconductors have gained a lot of attention to enable low-cost, large-area, and easy processing electronics. The comparison between above mentioned technologies is given in Table 2.1. The processing temperature of poly-Si TFTs is very high (~600°C) due to which using flexible plastic or glass materials as substrate is a huge challenge. Therefore, despite very high charge-carrier mobility and stability of poly-Si TFTs, they are not preferred for fabrication of large-area, low-cost and flexible systems. At the moment a-Si:H is most suitable for TFT technology because of its low processing temperature (~300°C) as compared to that required by poly-Si for TFTs. This processing temperature is suitable for substrates such as glass and metal foils. However, this processing temperature is not suitable for flexible substrates such as plastics which is a huge challenge for the already developed a-Si:H TFT technology.

Table 2.1 : Comparison of Different Thin-film Transistor Technology [Source : Klauk *et al*, 1999; Sirringhaus, 2014]

TFT Technology	Process temp.	Carrier mobility	Stability	Processing	Cost	Flexible substrate
Poly-Si	>> RT	High	High	New	High	Concern
a-Si:H	> RT	Low	Concern	Mature	Low	Concern
Organic	RT	Low	Concern	In research	Low expected	Compatible

Hence, there is a strong need for the development of low-cost, large-area, and flexible electronics. Organic TFTs are compatible with low-temperature processing and flexible substrates which makes it suitable for large-area, low-cost and flexible electronics. However, there are various issues associated with organic TFTs which need to be addressed before these TFTs can be employed in real life flexible system. Some of the challenges are discussed in Section 2.4.5. Most of the challenges faced by organic TFTs such as bias-stress stability, low field-effect mobility are similar to those faced by a-Si:H TFTs. The a-Si:H TFT is developed and matured, hence it is used for benchmarking purposes for all high performance organic TFT technology. The structure, operation, and challenges faced by a-Si:H TFTs are briefly discussed in the following Section.

2.3 HYDROGENATED AMORPHOUS SILICON TFTs

Amorphous silicon is the disordered arrangement of silicon atoms, with large number of defects referred to as dangling bonds. These dangling bonds are filled with hydrogen atoms, thereby resulting in a-Si:H. The a-Si:H semiconductor has less number of defect states as compared to a-Si, and it is used in various electronic applications. The first a-Si:H TFT with silicon nitride (Si_3N_4) as gate dielectric was discovered by Comber *et al* in 1979 [Comber *et al*, 1979] and it showed a charge-carrier mobility of less than 1 cm^2/Vs, current on/off ratio of more than 10^6 and subthreshold slope of less than 0.5 V/decade [Kuo, 2013]. These parameters of devices were good enough to incorporate a-Si:H TFT in driver circuits of displays. Hence, it boosted the research in TFT technology to a large extent. In present scenario, TFTs based on a-Si:H semiconductor is widely used in the backplane technology because of its applicability for large-area electronics. The n-type a-Si:H TFTs are widely used and preferred over p-type a-Si:H TFT due to the much higher mobility of the electrons *i.e.* 100 times than compared to the holes

in a-Si:H semiconductor [Moore, 1977]. The high charge-carrier mobility of electrons in n-channel a-Si:H semiconductor, leads to high current, low power consumption, and high operation speed of devices and circuits.

2.3.1 Structure and Operation

A simplified structure of an n-type a-Si:H TFT is shown in Figure 2.6. The a-Si:H TFTs fabricated by M. J. Powell *et al* have chromium (Cr) as the gate electrode, Si_3N_4 as the dielectric layer, intrinsic a-Si:H as semiconductor, heavily doped (n^+) a-Si:H is placed between the source/drain electrodes and intrinsic semiconductor by deposition and etching process before the deposition of a double layer of chromium/aluminium as the source and drain contacts [Powell, 1989]. The charge-carrier responsible for carrier transport in n-type a-Si:H TFT are electrons because of insignificant amount of holes due to the presence of n^+ a-Si:H below source and drain metal contacts which block the movement of holes between source and drain terminals.

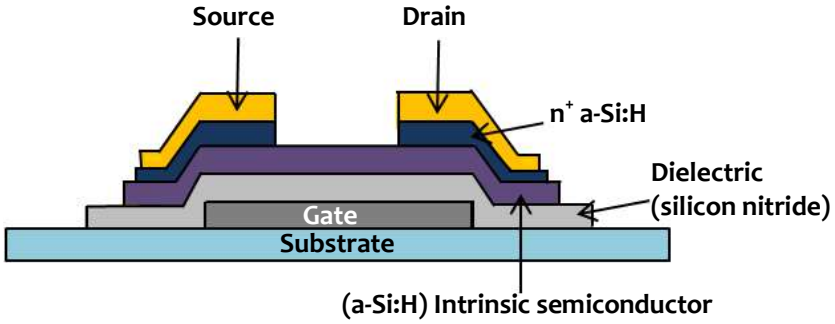

Figure 2.6 : Simplified structure of an n-type a-Si:H TFT

The operation of the a-Si:H TFT is similar to MOSFETs accumulation condition. The energy band model along with the presence of the localized states/traps is given in Figure 2.7. When no voltage is applied at the gate terminal, energy bands are flat and the Fermi level is at the middle of the mobility edge of CB and VB (see Figure 2.7(a)). When negative voltage is applied at the gate, equal and opposite charge-carriers (holes) are generated at the semiconductor/dielectric interface. However, the generation of holes are repelled by heavily doped a-Si:H, forming a depletion region. In this condition, the density of electrons in channel is low and the Fermi level moves close towards the VB, thereby passing the deep trap states (see Figure 2.7(b)). Hence, when no gate-source voltage is applied, no drain current flows even if a drain-source voltage ($V_{DS} = V_{DD}$) is applied and this condition is called as "OFF" state.

On applying a small positive voltage at the gate terminal ($V_{GS} < V_{th}$), energy bands move in downward direction and Fermi level moves closer towards the CB, thereby passing the deep trap states (see Figure 2.7(c)). During this transition, deep trap states are filled and only few charge-carriers contribute to the CB tail because the applied voltage is very low. In other words, when positive gate voltage is applied such that $V_{GS} < V_{th}$, electrons are attracted at the other end of the dielectric. However, there is no conduction of current because the applied voltage at gate is less than the threshold voltage.

On further increasing the applied voltage at gate ($V_{GS} > V_{th}$), the Fermi level shifts more towards the CB and band bending becomes more strong in downward direction (see Figure 2.7(d)). In other words, when applied gate-source voltage is greater than the threshold voltage ($V_{GS} > V_{th}$); a channel filled with electrons is formed between source and drain region due to

which drain current (I_{DS}) can flow between source and drain electrodes upon applying a voltage at drain-source terminal (V_{DS}). This is referred to as "ON" state.

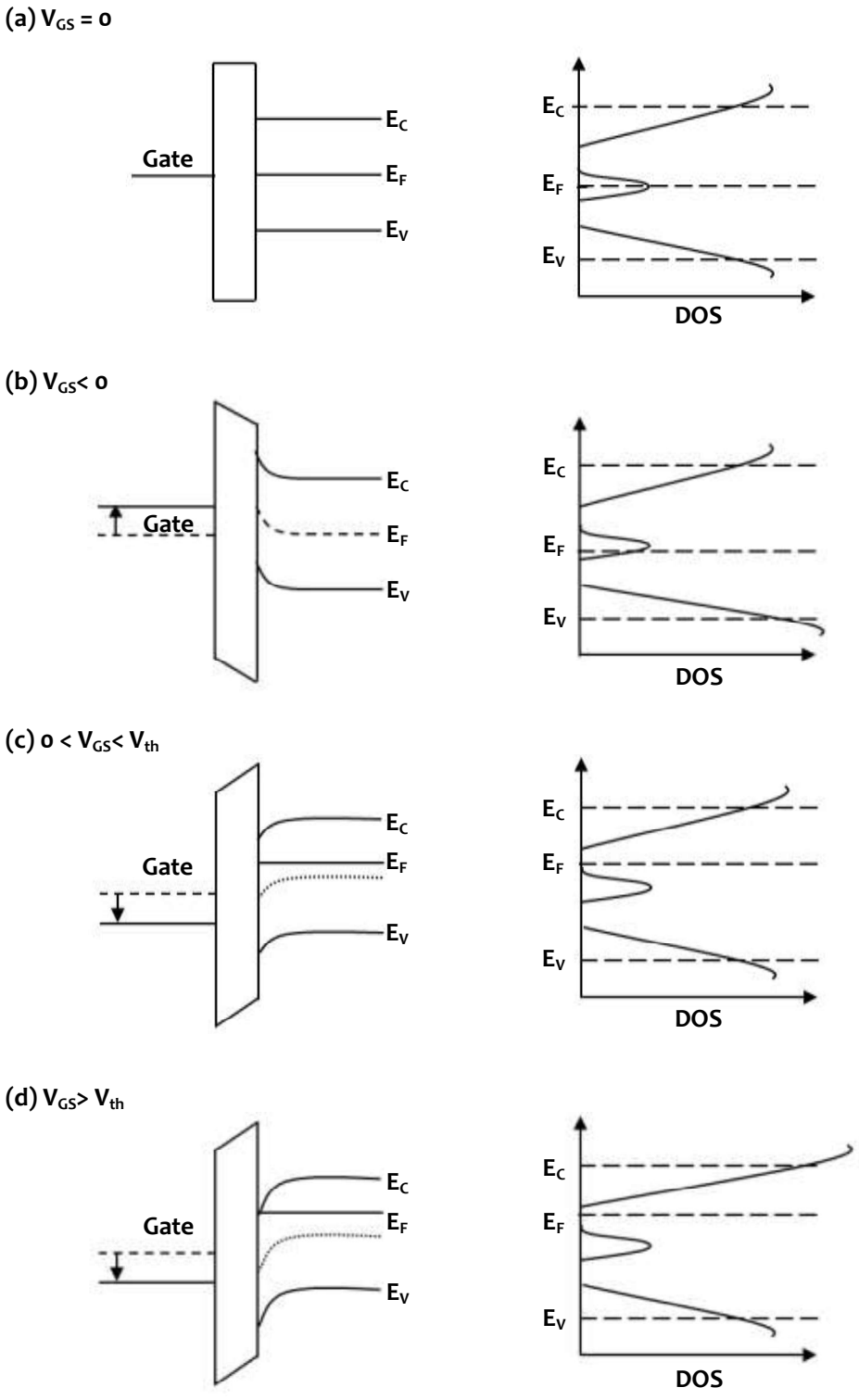

Figure 2.7 : Schematic diagram showing the Energy Band Model and presence of Localized States in various conditions [Source : Powell, 1989]

2.3.2 Challenges

The main challenges faced by a-Si:H TFTs are, low charge-carrier mobility, high leakage current, and low electrical stability which are discussed in this Section. The possible ways which are demonstrated in available literature to overcome or negotiate these challenges are also discussed here. The low mobility of a-Si:H TFT is due to the high defect density in a-Si, which limits the performance of devices. If high-performance of devices is an imperative part, then polycrystalline TFTs can be used in place of a-Si:H TFTs, which exhibit higher charge-carrier mobility of ~50 cm^2/Vs compared to the field-effect mobility of a-Si:H TFTs which is ~1 cm^2/Vs. However, polycrystalline TFTs are not suitable for large area and flexible electronics, due to its high processing temperature. Hence, it is a compromise between high performance and flexibility of devices. The high leakage current in the a-Si:H devices are primarily due to the photoconductive nature, which is dealt by protecting with an opaque material [Kuo, 2013].

The electrical instability of a-Si:H TFTs is also one of the challenges affecting the performance of systems driven by these TFTs. This electrical instability of the systems causes unsteadiness in the threshold voltage which directly affects the efficiency of devices. One of the main causes of shift in threshold voltage is bias-stress instability which is discussed in Chapter 4. For instance, a-Si:H TFTs are widely used as a driver circuit in Active Matrix Organic Light-Emitting Diode (AMOLED) and unsteadiness of threshold voltage causes the drop in the drain current given by TFT to drive AMOLED, leading to the reduction in the brightness of AMOLED. Hence, it is very important to compensate the unsteadiness of threshold voltage. Some of the techniques to compensate this unsteadiness in threshold voltage is to apply an on-pixel signal, and/or to apply an external circuitry in current technology using a-Si:H as driver circuit [Jafarabadiashtiani *et al*, 2005].

The schematic diagram of an AMOLED pixel circuit with the feedback circuitry is shown in Figure 2.8. The complete circuit consists of an external driver, two switching TFTs (T2 and T3), a storage capacitor (C_S), a driving TFT (T1), an OLED, and a feedback resistor (R_F). This circuit operates in two modes: programming and hold [Jafarabadiashtiani *et al*, 2005]. When select line is applied with high voltage (1), both the transistors T2 and T3 are turned on, as a result of which transistor (T1) is turned on and current (I_{ON}) flows through the T1. The feedback resistance (R_F) converts the current (I_{ON}) into feedback voltage (V_F) which is given as one of the input to differential amplifier. The differential amplifier compares V_F with input voltage (V_{IN}) and maintains the required voltage (V_G) at the gate terminal of transistor T1. This is called as programming mode and the amount of current flowing through T1 during this mode [Jafarabadiashtiani *et al*, 2005] is given as,

$$I_{ON} = {}^{V_{IN}}/_{R_F} \tag{2.4}$$

This equation shows that the I_{ON} flowing in the transistor (T1) depends only on the R_F and hence, it is very essential to have a balanced feedback resistor. When select is low voltage (1), all the transistors (T1, T2 and T3) are turned off and circuit is said to be in Hold state. In this mode, the driver circuit is no more connected to regulate the gate voltage. However, the current across T1 does not change much because the gate voltage of T1 is stored in the storage capacitor (C_S) [Jafarabadiashtiani *et al*, 2005]. This circuit shows one of the methods of reducing the control of the TFTs in controlling the performance of OLED displays by employing an external circuitry.

However, the system shown in Figure 2.8 has differential amplifier with finite gain (A_G) which causes imbalance in the system. Due to this imbalance in the system, the current during programming mode also slightly depends on the threshold voltage (V_{th}) of the a-Si:H TFT (T1) [Jafarabadiashtiani *et al*, 2005] is given as,

$$I_{ON} = {}^{V_{IN}}/_{R_F} - {}^{V_{th}}/_{A_G.R_F} \tag{2.5}$$

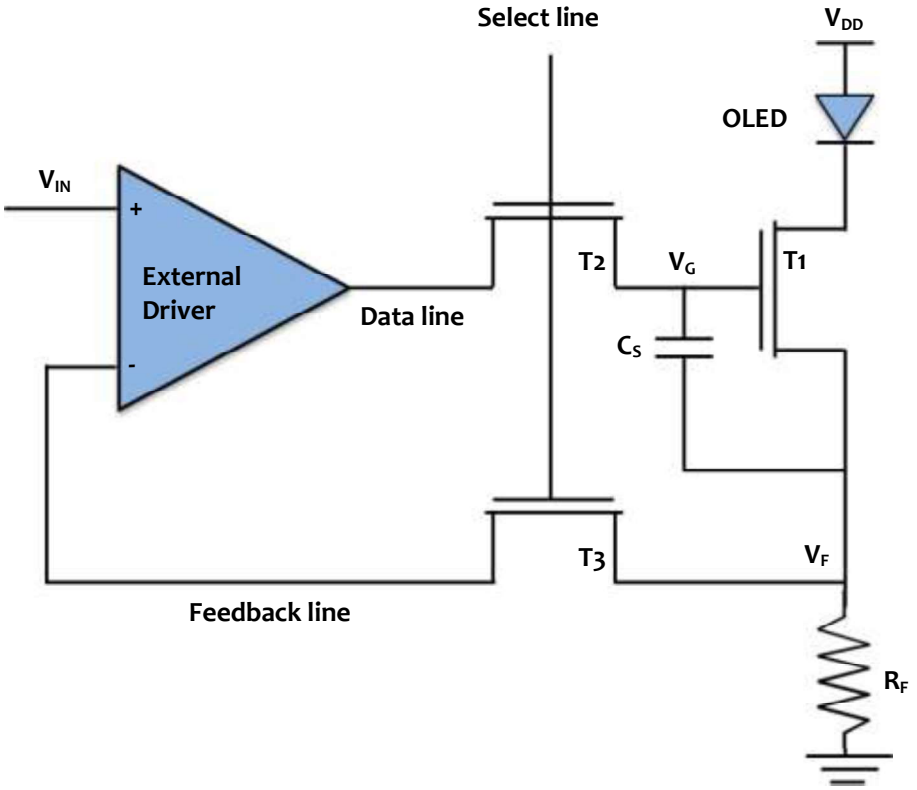

Figure 2.8 : Schematic diagram of Pixel Circuit using the Feedback Voltage to overcome the Drawbacks Laid by the Electrical Instability of TFTs [Source : Jafarabadiashtiani *et al*, 2005]

Threshold voltage shift on a-Si:H TFTs may occur due to various conditions such as, upon exposure to radiation, and other environmental effects and hence, it may not be same among various devices. This can cause the problem of non-uniformity in the brightness of the pixels of systems driven by a-Si:H TFTs. Hence, it is very essential to have good electrically stable and reliable a-Si:H TFTs for achieving long stability and reliability of systems driven by these TFTs such as AMOLEDs.

2.3.3 Bias-stress Instability

The stability of a-Si:H TFTs is very crucial for high performance and durability of systems (such as displays) driven by them. The bias-stress instability is well realized and understood for a-Si:H TFTs. The condition in which a constant continuous voltage is applied to the gate, source, and drain terminals of a-Si:H TFTs for longer duration of time is referred as bias-stress, and it causes shift in the threshold voltage. The shift in threshold voltage can either be due to the trapping of the charge-carriers in the dielectric [Powell *et al*, 1992; Karim *et al*, 2004] and/or due to the creation of defects in the channel [Powell *et al*, 1989; Libsch and Kanicki, 1993]. The threshold voltage shift for a-Si:H TFTs with time is modeled as two-stage model for predicting the lifetime under low gate-field [Libsch and Kanicki, 1993; Liu *et al*, 2012] and is given as,

$$\Delta V_{th}(t) = \Delta V_{th,m}\left[1 - \exp - \left(\frac{t}{t_o}\right)^{\beta}\right] \tag{2.6}$$

where $\Delta V_{th,m}$ is the difference between the gate-source voltage (V_{GS}) and initial value of the threshold voltage (V_{th0}) before applying the gate-source voltage bias. It is important to note that the maximum possible shift in the threshold voltage due to bias-stress is the applied value of gate-source voltage (V_{GS}). β is the ratio of the kT to the characteristic energy associated with the distribution of the weak bonds. t_0 is the characteristic time required for conversion of weak

bonds into dangling bond and is given as, $t_0 = v^{-1} \exp(E_A/kT)$ [Liu *et al*, 2012], where E_A is the thermal activation energy and v is the attempt-to-escape frequency.

The drain current in saturation region is essential to be stable because at this region, transistor is in "ON" state. But the instability in the threshold voltage causes a change in the drain current with time and using Eq.(2.3) and Eq.(2.6), it is given as,

$$I_{DS}(t) = \mu_n . C_d . \frac{W}{2L} . \{V_{GS} - [V_{tho} + \Delta V_{th}(t)]\}^2 \quad (2.7)$$

The normalized drain current is the ratio of the drain current at time (t) and the drain current at time (t = 0) and it is given as,

$$I_{DS,normal} = I_{DS}(t) \Big/ I_{DS}(t = 0) \quad (2.8)$$

also given as [Source : Liu *et al*, 2012],

$$I_{DS,normal} = \exp -2\left(\frac{t}{t_0}\right)^{\beta} \quad (2.9)$$

This equation can be used for fitting the experimental variation of normalized drain current with time as it is or with some modifications [Liu *et al*, 2012] depending upon the lifetime of the a-Si:H TFT. Since stability issues of a-Si:H TFTs have been understood and modeled properly, hence, a-Si:H TFTs are being used for commercialized use, such as displays. Their capability to be processed at 300°C, makes it compatible with glass substrates. However, this processing temperature is quite high for flexible substrates, thereby questioning the compatibility of a-Si:H with substrates such as plastics. Hence, organic TFTs which are compatible with low temperature processing and flexible substrates are gaining a lot of attention for the development of a new era of flexible displays.

2.4 ORGANIC TFTs

The active layer in an organic TFT is of organic semiconducting material. The charge-carrier mobility achieved in organic TFT has increased from 10^{-5} cm^2/Vs in 1985 to more than 1 cm^2/Vs in year 2014, also shown in Figure 1.3. The ability of organic semiconductors to be processed using techniques such as vacuum evaporation, spin coating, drop casting, and printing makes it a cost effective technique. The compatibility of processing these organic semiconductors at low temperature makes it suitable for fabrication of organic TFTs on flexible substrates such as plastics having larger area as compared to rigid substrates such as silicon. The advantage of producing these devices at large area and low temperature on flexible plastic substrates makes it a low-cost technology, which has gained the attention of researchers world-wide.

The current focus of this research work is towards demonstrating flexible, high performance, stable and reliable organic TFT devices with low voltage operation which can be implied in future commercial systems. The structure, operation, electrical characteristics, parameter extraction for evaluating the performance, and challenges of organic TFTs are discussed in following Section.

2.4.1 Architecture

An organic TFT device consists of mainly four layers namely: one metal layer as gate electrode, second metal layer to form source and drain electrodes, dielectric layer, and organic semiconductor layer. The gate metal electrode is separated from the source and drain electrodes by a dielectric layer. Depending on the sequence of deposition processes and placement of gate

and source/drain electrodes, organic TFTs can be classified into four types (see Figure 2.9), top-gate-top-contact, bottom-gate-top-contact, top-gate-bottom-contact, and bottom-gate-bottom-contact. Here these structures are named on the basis of the placement of gate and metal (source and drain) contacts. These structures can also be named on the basis of the deposition of the active material, and these are called as top-gate-coplanar, bottom-gate-staggered, top-gate-staggered, and bottom-gate-coplanar device structures respectively. Figure 2.9(b and c) show the staggered structure because gate and metal contacts are present on the opposite side of the active layer and Figure 2.9(a and d) show the coplanar structure because gate and metal contacts lie on the same side of the active layer.

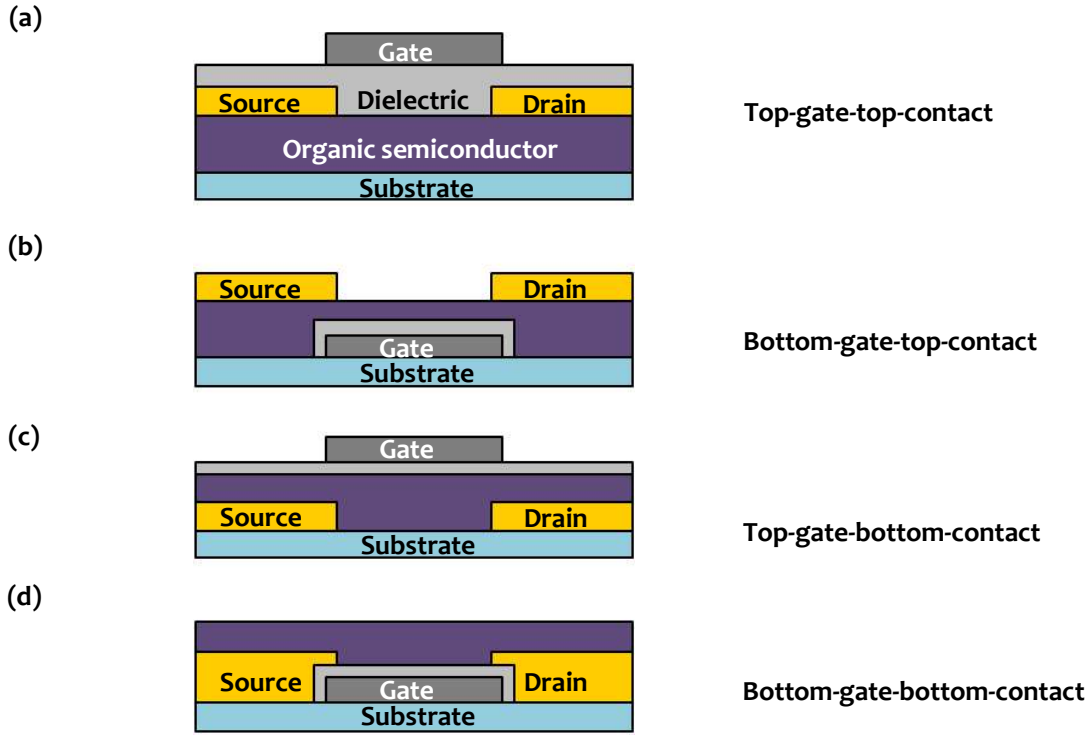

Figure 2.9 : Schematic diagram showing various Architecture of Organic TFTs: (a) Top-gate-top-contact (Coplanar), (b) Bottom-gate-top-contact (Staggered), (c) Top-gate-bottom-contact (Staggered), and (d) Bottom-gate-bottom-contact (Coplanar)

The devices are named as top or bottom contacts depending on whether the source and drain electrodes are deposited on the top of the semiconductor or below the semiconductor. Similarly, the devices are referred as top or bottom gate depending on whether the gate electrode is deposited on top of the dielectric or below the dielectric. Among all the four architectures, the easiest one to fabricate is bottom-gate-bottom-contact structure (see Figure 2.9(d)), where organic semiconductor layer is deposited in the last step in the pre-patterned substrate having gate, source and drain electrodes. One of the commonly used device structure of this category is the one where heavily doped Si substrate is used as the gate dielectric, SiO_2 as dielectric, and patterned metal contacts (Cr/Au; Ti/Au; Au) as source and drain electrodes. Finally on these substrates, any organic semiconductor can be deposited by spin coating or vacuum evaporation or any other processing technique to complete the organic TFT fabrication for that semiconductor. This bottom-gate-bottom-contact organic TFT structure has been mainly used for characterizing the properties of organic semiconductor.

To achieve better performance in terms of low contact resistance the bottom-gate-top-contact structures are preferred [Gupta *et al*, 2009]. The same structure has been used in this thesis to study the stability and reliability of organic TFT devices.

2.4.2 Operation

The organic TFTs operate in accumulation mode on the contrary to the conventional MOSFET devices where inversion mode is required for the device to be turned on. However, due to the high similarity of the output and transfer characteristics obtained from organic TFT devices, the current model of conventional MOSFETs is used to analyze organic TFT devices. The operating principle of both p-channel and n-channel organic TFTs with the help of energy level diagram with various applied voltage conditions is described in Figure 2.10 in left and right diagrams respectively.

When no voltage is applied at gate, source and drain terminals, the majority charge-carriers (holes in p-type and electrons in n-type) are uniformly distributed in the semiconductor and there is no channel formation between source and drain electrodes for conduction (see Figure 2.10(a)). To have better charge injection from source to semiconductor, it is preferable to use source and drain metals with Fermi level close to HOMO level for hole injection, and to LUMO level for electron injection for achieving low contact resistance and a better conduction between source and drain resulting the high performance organic TFT devices.

For a p-channel organic TFT, when a negative gate voltage is applied such that $V_{GS} < 0$ and $|V_{GS}| > |V_{th}|$, excess holes are accumulated at the semiconductor/dielectric interface leading to formation of a conducting channel of accumulated holes between source and drain terminals. The carrier concentration in the channel is controlled by applied gate-source voltage. However, there will be no flow of current until a drain-source voltage is applied. In this condition, the Fermi level of metal is almost matched with the HOMO level of semiconductor (see Figure 2.10(b)).

When negative voltage is also applied at drain-source terminal ($V_{DS} < 0$), the potential barrier between source and drain terminals is reduced that results in the conduction of drain current (I_{DS}) between source and drain terminals (see Figure 2.10(c)). This is called as the accumulation mode and organic TFTs are "switched on" in this mode. The p-channel organic TFTs are "switched off", when absolute value of applied voltages at gate-source is lower than the absolute value of threshold voltage $|V_{GS}| < |V_{th}|$.

The operation of n-channel organic TFTs is also similar to that of the p-channel organic TFTs (see right side of Figure 2.10), with a discrepancy that n-channel organic TFTs are "turned on", when excess electrons are accumulated at the semiconductor/dielectric interface leading to formation of a conducting channel of accumulated electrons between source and drain terminals. In this condition, the LUMO level of semiconductor is matched with the metal Fermi level upon applying positive voltages ($V_{GS} > 0$, and $V_{DS} > 0$).

Similar to MOSFETs, the organic TFTs have two operating regimes. The first is linear regime, where drain current increases almost linearly with applied drain-source voltages for a particular applied gate-source voltage. When this current saturates and does not increase significantly with applied drain-source voltages, it results in the second operating regime called as saturation. This linear and saturation regimes are further discussed in the electrical characteristics in Section 2.4.3.

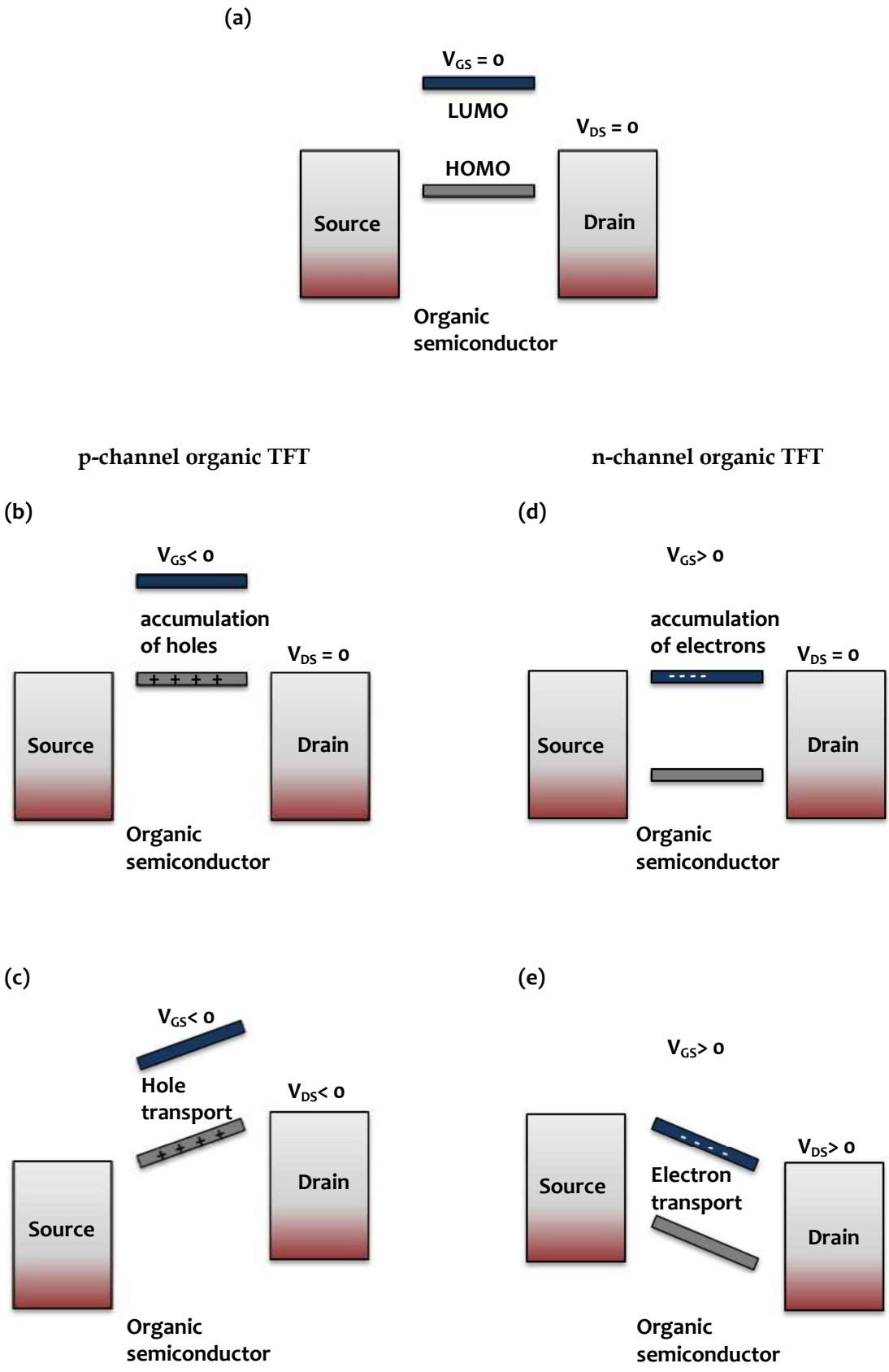

Figure 2.10 : Schematic diagram showing the Operating principle of p-channel and n-channel Organic TFT (Left and Right respectively)

2.4.3 Device Characterization

The TFT devices are characterized with the help of two types of plots, one where the change of drain current is plotted with continuous increase in drain-source voltages for a particular gate-source voltage, and it is named as output characteristics. In this plot, the gate voltage is varied in steps from 0 to V_{DD} (maximum applied voltage). The second plot is transfer characteristics, where drain current is plotted with continuous change in gate-source voltage for a particular drain-source voltage. Depending upon whether this drain-source voltage is small or close to V_{DD}, the transfer characteristics are obtained for either linear or saturation region.

The electrical characterization set-up used in this study for measuring the current-voltage characteristics is shown in Figure 2.11. It consists of a micromanipulator 6200 probe station and Agilent 4156C parameter analyzer. The probe station consists of a chuck which can move in X, Y, and Z direction, and it is connected to a vacuum pump which prevents the movement of the sample placed in the chuck; six manipulators which can also move in X, Y, and Z direction and are connected to vacuum pump to prevent their movement during measurements; and an optical microscope. However, utmost three manipulators are used for the measurements in this thesis work. The substrate is placed in the vacuum chuck. The manipulators are used to probe the source, drain, and gate contacts and are connected to the parameter analyzer. The parameter analyzer *i.e.* the three source-measurements unit (SMU) is used to give the input signals to the devices and results are obtained from it.

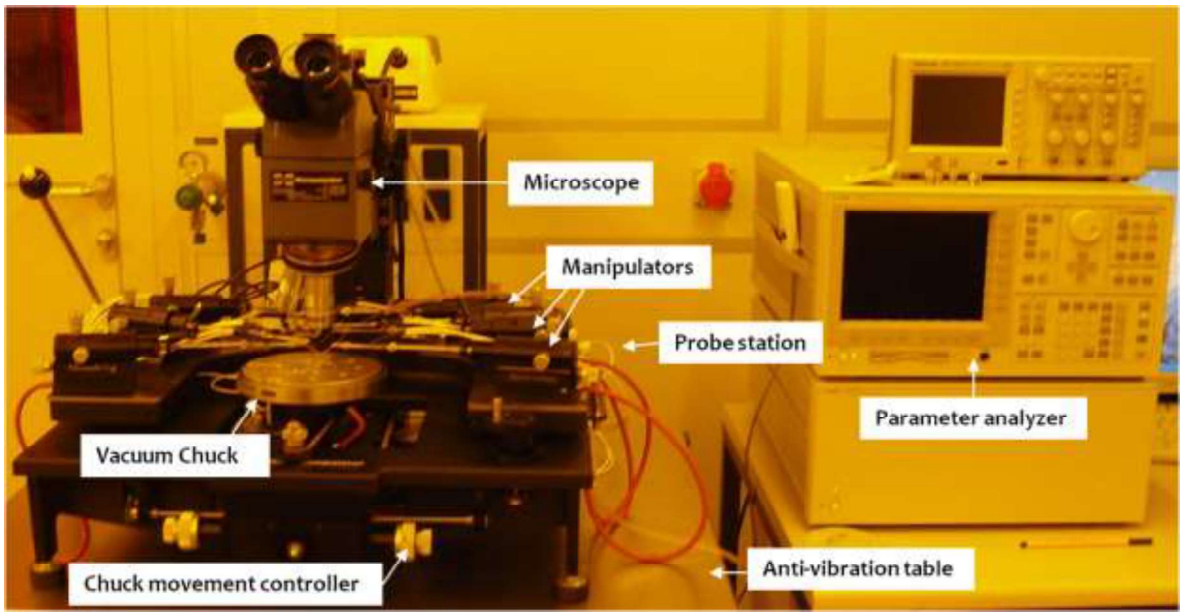

Figure 2.11 : Photograph of the Electrical Characterization Set-up Consisting of Keithley 6200 Probe Station and Agilent 4156C Parameter Analyzer

A bottom-gate-top-contact structure is used here to explain the electrical characteristics of fabricated organic TFTs whose schematic structure is given in Figure 2.12. The device consists of heavily doped p-type Si substrate which acts as the gate electrode; combination of thermally-grown 100 nm-thick SiO_2, 8 nm-thick aluminium oxide (AlO_x) deposited by atomic layer deposition technique (ALD), and 1.7 nm-thick n-tetradecylphosphonic acid (HC_{14}-PA) self-assembled monolayer (SAM) as the dielectric; 15 nm-thick 2,9-didecyl-DNTT (C_{10}-DNTT [Kang *et al*, 2011]) as organic semiconductor (discussed in Chapter 3 in detail); and 30 nm-thick gold as source and drain electrodes. The fabricated organic TFT has L of 100 µm and W of 200 µm. The

capacitance per unit area is 34 nF/cm² [Zschieschang *et al*, 2012; Hofmockel *et al*, 2013; Zschieschang *et al*, 2013]. The transfer and output characteristics of this C_{10}-DNTT organic TFT is shown in Figure 2.13.

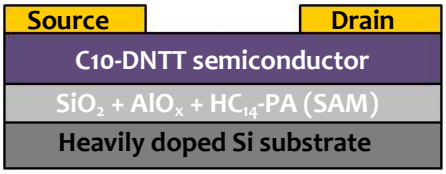

Figure 2.12 : Schematic structure of Fabricated Bottom-gate-top-contact Organic TFT

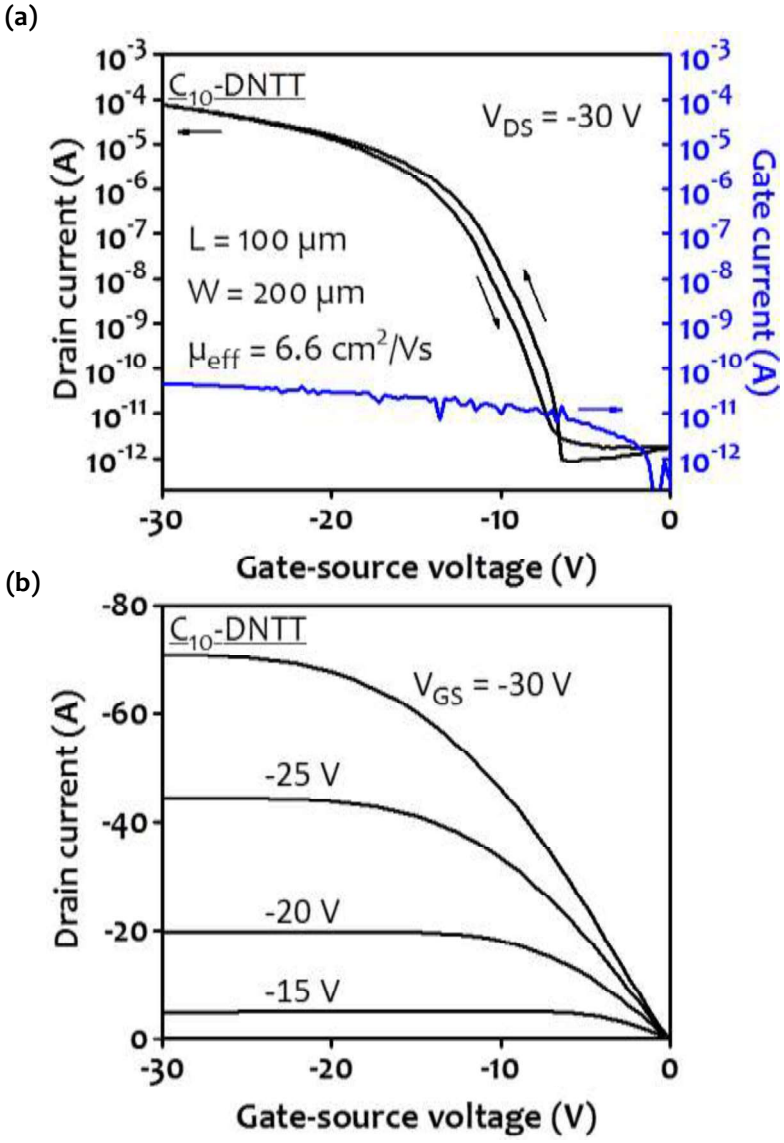

Figure 2.13 : Electrical Characteristics of an Organic TFT with W of 200 µm and L of 100 µm: (a) Transfer and (b) Output Characteristics, pointing the Linear and Saturation Regions

The transfer characteristics show the variation of the drain current (I_{DS}) as a function of gate-source voltage (V_{GS}) from 0 V to -30 V (varying with a step of -0.3 V) at a specified drain-source voltage (V_{DS}) of -30 V in this case (see Figure 2.13(a)). The output characteristics show the variation of the drain current (I_{DS}) as a function of drain-source voltage from 0 V to -30 V (varying with a step of -0.6 V) at specified gate-source voltages of -10 V, -15 V, -20 V, -25 V and -30 V (see Figure 2.13(b)). In the output characteristics, it can be seen that a nice saturation is achieved for drain current, similar to that observed in conventional MOSFETs. The same is true for the transfer characteristics observed for C_{10}-DNTT based organic TFT. Due to this similarity of transfer and output characteristics in between organic TFTs and conventional MOSFETs, the same drain current [Eq.(2.2) and Eq.(2.3)] is used for organic TFT devices.

2.4.4 Parameter Extraction

The measurement results of the fabricated C_{10}-DNTT based organic TFT explained above is used here for the extraction of the parameters which are important to evaluate the performance of the devices. The transfer characteristics (I_{DS} versus V_{GS}) and the variation of square root of drain current with gate-source voltage ($\sqrt{I_{DS}}$ versus V_{GS}) is shown in Figure 2.14, and it is used for the extraction of various essential parameters such as field-effect mobility, threshold voltage, current on/off ratio, and subthreshold slope.

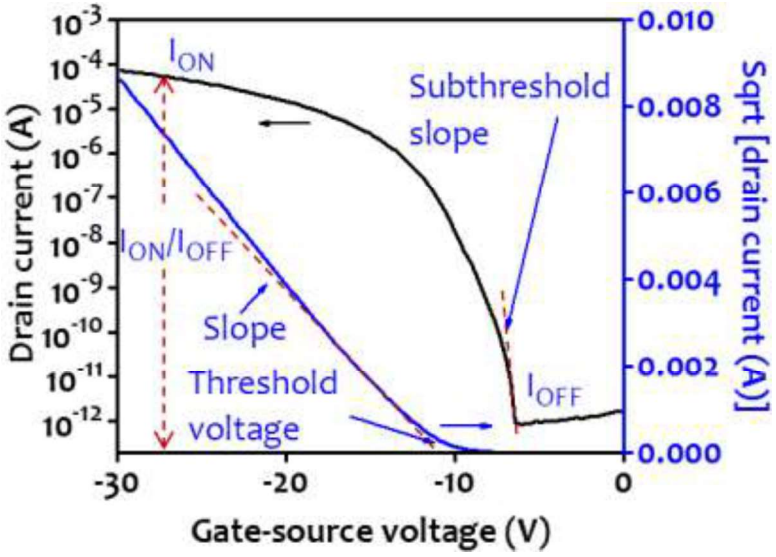

Figure 2.14 : Change in Drain Current (Black Line) and Square Root of Drain Current (Blue Line) with the Gate-Source Voltage for Applied Drain-source Voltage of -30 V

(a) Field-effect Mobility

The field-effect mobility is calculated using the slope (red dotted line in Figure 2.14) of the graph plotted between the square root of drain current and gate-source voltage. Depending on whether the TFT device is operated in linear region ($V_{GS} - V_{th} > V_{DS}$), or in saturation region ($V_{GS} - V_{th} < V_{DS}$); the field-effect mobility is named as linear or saturation field-effect mobility, respectively. The extracted field-effect mobility in saturation region is derived using the drain current Eq.(2.3) for the saturation region, and it is given as,

$$\mu_{eff} = \frac{2L}{W.C_d} \cdot \left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \qquad (2.10)$$

The effective saturated field-effect mobility extracted from the measured results for C_{10}-DNTT based organic TFT is 6.6 cm^2/Vs, and it is plotted as a function of applied gate-source voltage in Figure 2.15.

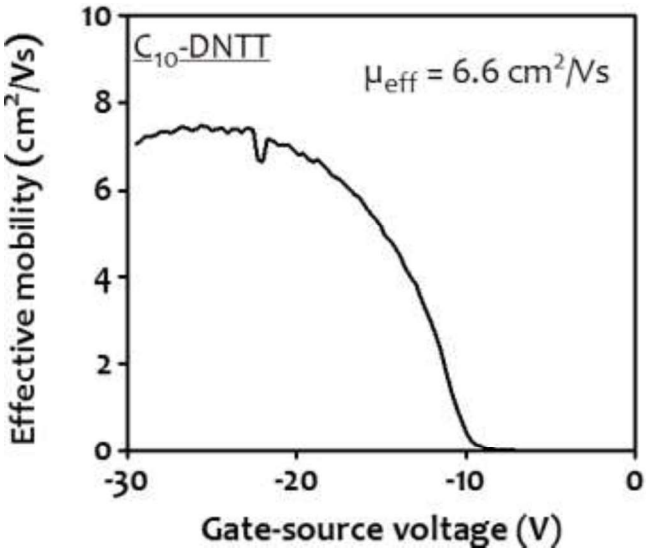

Figure 2.15 : Effective Charge-carrier Mobility as a function of Gate-source Voltage for Applied Drain-source Voltage of -30 V

The field-effect mobility (μ_{eff}) is different for linear and saturation region due to its dependence on applied gate-source and drain-source voltages. The drain current equation for linear region [Eq.(2.2)] is used to derive the linear field-effect mobility and it is given as,

$$\mu_{eff} = \frac{L}{W.C_d.V_{DS}}.\frac{\partial I_{DS}}{\partial V_{GS}} \tag{2.11}$$

The field-effect mobility in linear region is lower compared to field-effect mobility in saturation region due to the strong effect of contact resistance in linear region due to low applied voltages [Necliudov *et al*, 2003; Blanchet *et al*, 2004; Gundlach *et al*, 2006].

(b) Threshold Voltage

The threshold voltage of organic TFT is also calculated from the graph plotted in between square root of the drain current and gate-source voltage ($\sqrt{I_{DS}}$ versus V_{GS}) by using the straight line tangential to the maximum slope point. The value of threshold voltage is obtained from the intersection made by this line on the gate-source voltage axis (see Figure 2.14). It is important to note that the same point where maximum slope is obtained provides the value of maximum mobility of the device. The threshold voltage of fabricated C_{10}-DNTT organic TFT on Si substrate explained in Section 2.4.3 is -12 V.

(c) Current On/Off Ratio

The current on/off ratio is calculated from the ratio of the drain current when device is completely ON ($V_{GS} = V_{DS} = V_{DD}$) to the drain current during "OFF" condition ($V_{GS} = 0$). The current on/off ratio of fabricated p-channel organic TFT in Section 2.4.3 is estimated as ~10^8 (see Figure 2.14).

(d) Subthreshold Swing

The subthreshold swing (S) is the inverse of the maximum slope of the change in drain current in logarithmic scale as a function of gate-source voltage. It is shown using the red dotted line in Figure 2.14 and is given as,

$$S = \frac{dV_{GS}}{d\log I_{DS}} \tag{2.12}$$

The subthreshold swing of fabricated organic TFT given in previous Section is 0.9 V/decade. The subthreshold swing can also be used to calculate the maximum interfacial trapped density (N_{trap}) of states using following equation [McDowell *et al*, 2006],

$$S = \frac{kT}{q} . \log 10 \left[\frac{q.N_{trap}}{C_d} + 1\right] \tag{2.13}$$

Subthreshold swing is used to measure the amount of voltage required for changing the current by a decade, near the point of maximum slope. The low value of subthreshold swing *i.e.* steep slope in the logarithmic drain current as a function of gate-source voltage is desirable for faster switching. Since, it takes less voltage for switching on the devices with low subthreshold swing, and the operating voltage is also reduced resulting in low static power consumption.

2.4.5 Challenges

Though organic TFTs have shown a lot of promise to be used in large-area flexible electronics with field-effect mobility comparable to a-Si:H TFTs, there are various issues which need to be addressed before these devices can be used in the commercialized systems. Some of the challenges in achieving high-performance, reliable, and reproducible organic TFTs are low field-effect mobility, high operating voltage, and electrical and environmental stability.

(a) Field-effect Mobility

Achieving high field-effect mobility is very important for organic TFT devices to produce high currents sufficient for driving any circuitry. The field-effect mobility of a particular organic semiconductor based TFT depends on various parameters such as technique used for depositing organic semiconductor, device geometry, and materials used for substrate, and dielectric. For example, one of the most commonly studied organic semiconductors *i.e.* pentacene, has shown huge improvement in field-effect mobility from ~0.002 cm^2/Vs in year 1992 [Dimitrakopoulos and Malenfant, 2002] to more than 0.5 cm^2/Vs in 2014 [Sirringhaus, 2014].

It was reported that the performance of pentacene based TFTs differs depending upon the device structure *i.e.* coplanar or staggered, irrespective of the same materials used for the fabrication of both device structures [Necliudov *et al*, 2003]. The field-effect mobility of 3 cm^2/Vs for pentacene based TFT fabricated on Si substrate with polyvinylphenol (PVP) as dielectric material was also reported [Klauk *et al*, 2002]. The same group has also reported the field-effect mobility of 0.6 cm^2/Vs for the same organic semiconductor based TFT fabricated on glass substrate with AlO_x as gate dielectric [Zschieschang *et al*, 2009].

The field-effect mobility extracted from TFT devices for different organic semiconductors has increased from ~10^{-5} cm^2/Vs in year 1984 to more than 1 cm^2/Vs in year 2014. However, in most of the cases where demonstrated field-effect mobility is 10 or greater, the applied voltages are generally very high (20 V to 100 V). For example, the field-effect mobilities of ~10.2 cm^2/Vs, and current on/off ratio of ~10^7 were reported for solution processed dithieno[3,2-b:2′,3′-d]thiophene derivatives based organic TFTs, fabricated on Si substrate with dielectric combination of SiO_2 and poly(methylmethacrylate) *i.e.* PMMA operating at voltages of 40 V to 80 V [Yang *et al*, 2013]. Similarly, field effect-mobilities of up to ~8.2 cm^2/Vs for poly[2,5-bis(alkyl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione-alt-5,5′-di(thiophen-2-yl)-2,2′-(E)-2-

(2(thiophen-2-yl)vinyl)thiophene] (PDVT-10) based organic TFT fabricated on octadecyltrichlorosilane (OTS) modified surface treated Si/SiO_2 (300 nm) substrates operating at voltages up to 100 V were reported [Chen *et al*, 2012].

Since, field-effect mobility depends on the applied voltage; achieving high values of field-effect mobility is a challenge for low-operating voltage organic TFTs. U. Zschieschang *et al* reported field-effect mobility of 4.3 cm^2/Vs for 2,9-didecyldinaptho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (C_{10}-DNTT) based organic TFT fabricated on flexible plastic substrate with thin dielectric of AlO_x followed by the deposition of HC_{14}-PA operating at 3 V [Zschieschang *et al*, 2012]. On similar dielectric and operating at similar voltages, a field-effect mobility of ~17.2 cm^2/Vs for 2-tridecyl[1]benzothieno[3,2-b][1]-benzothiophene (C_{13}-BTBT) based organic TFT, but these TFTs are fabricated on Si/SiO_2 substrates was reported [Amin *et al*, 2012].

All this improvement in field-effect mobility is only possible due to the efforts of material scientists and chemists in designing and developing new materials, physicists in advancing and developing physics, and device engineers in optimizing interfaces and device structures, and engineering contacts and dielectric layers. However, a lot of research and development is still required for producing organic TFT devices which can be flexible as well as exhibit higher field-effect mobilities.

The conduction in these organic TFTs is greatly influenced due to the first few mono layers of the organic semiconductor. Hence improving the molecular ordering of organic semiconductor for first few mono layers improves the field-effect mobility. The molecular ordering of organic semiconductor can be improved using SAM prior to its deposition, and using various annealing treatments before and/or during the deposition of organic semiconductor [Dickey *et al*, 2006; Kalb *et al*, 2007; Tiwari *et al*, 2009; Zschieschang *et al*, 2010; Yokota *et al*, 2013].

(b) Operating Voltage

Low operating voltage is required in devices for reducing the power consumption of the systems driven by these devices. One of the commonly used techniques to reduce the operating voltage of a device is to scale down the dimensions of the device, such as channel length and gate dielectric thickness. The high on current produced from small size devices enhances the speed of the circuits because the driving circuits are also small having less gate area and low capacitance. Reducing the dimension of channel length increases the drain current, but it has a limit, beyond which the leakage of devices overtakes the performance of devices, which is not desirable. Similarly, reducing the thickness of gate dielectric increases the gate dielectric capacitance. Hence, results in low voltage requirement at gate to produce the same drain current as that produced by a TFT with thick dielectric, operating at high voltages.

However, reducing the dielectric thickness is not possible all the time because of the breakdown field limit and gate leakage currents; to take care of this problem, high-k gate dielectric materials are used as an alternative for the same. There are various reports in which high-k materials are used as dielectric layer, which reduce the voltage operation of devices. Organic TFTs based on high-k dielectric material *i.e.* barium zirconatetitanate, pentacene as organic semiconductor; on Si substrate exhibiting a field-effect mobility of ~0.6 cm^2/Vs operating at ~100 V, and on plastic substrate exhibiting a field-effect mobility of ~0.4 cm^2/Vs operating at ~4.0 V were reported [Dimitrakopoulos *et al*, 1999]. There is a wide range of voltages at which organic TFTs are reported to operate. The pentacene based organic TFT with charge-carrier mobility of 0.7 cm^2/Vs and current on/off ratio of 10^8 when transistors were operated at ~100 V were also reported [Gundlach *et al*, 1997]. The same organic semiconductor based TFT has also been reported to have a charge-carrier mobility of 0.6 cm^2/Vs and current on/off ratio of 10^7, when transistors were operated at ~3.0 V [Klauk *et al*, 2007].

A high-k gate dielectric material may not be suitable for flexible substrates. Hence, thin gate dielectric materials with the combination of SAM are demonstrated to be an excellent option for low-voltage operating TFTs. The pentacene based organic TFTs fabricated on 2.5 nm thick molecular SAM as gate dielectric operating at ~2.0 V was reported [Halik *et al*, 2004]. C_{10}-DNTT based organic TFTs operating at ~3.0 V fabricated on flexible plastic substrate, and a dielectric combination of thin layer of AlO_x and $HC_{14}PA$ was also reported [Zschieschang *et al*, 2012].

(c) Device Reliability and Stability

There are two main issues related to device reliability and stability of organic TFTs. The first is the degradation of electrical characteristics upon exposure to ambient air, and the second is the change in electrical properties of devices upon extreme operating conditions. The electrical performance of organic TFTs degrades on exposure to air due to the oxidation of the organic molecules.

Pentacene is one of the widely studied organic semiconductors and the degradation of organic semiconductor on exposure to air is well known [Zschieschang *et al*, 2010]. This can happen either due to the moisture present in the atmosphere or due to the oxygen in air. The other factors such as exposure to light or any radiation can also result in temporary/permanent degradation of device characteristics. It was reported that pentacene based organic TFT device with low operational voltage of 30 V and limiting channel shows good device stability due to repeated applied voltage scans and environmental exposure as compared to devices with high operational voltage of 100 V and shorter channel lengths; the devices measured in ambient nitrogen show good stability than that measured in ambient air [Kagan *et al*, 2005].

The main challenge for addressing the issue of degradation due to environmental conditions is to find an organic semiconductor which doesn't oxidize/change its properties in ambient air and/or to find an encapsulation technique/material which can ensure complete protection from the environmental degradation. Many of the proposed passivation techniques protect the device from oxygen and moisture. However, they may not provide protection from light and radiation. One of the primarily requirements for the encapsulation layer is, compatibility with flexible substrates.

An improved stability of pentacene based TFTs on flexible polyimide substrate and Si substrate when parylene is used as the passivation layer was reported; but, these devices show hysteresis due to diffusion of water into pentacene semiconductor through parylene film, and it has been improved by encapsulating the device with parylene/acryl/aluminum triple layer instead of single parylene layer as encapsulation [Simeone *et al*, 2009]. The protection of flexible pentacene based devices from ultraviolet light due to the use of tindioxide (SnO_2) as encapsulating layer was also reported [Kim *et al*, 2006].

For real applications, organic TFT have to be switched "ON" for long duration, such as, for many hours or overnight for large area display applications and other switching circuitry purposes the devices have to be switched "ON" for more than thousands of timed continuously; for example, in displays with continuously changing information. For the first case, instability in threshold voltage is observed with time, when continuous voltages are applied at the device, which is also referred as bias-stress, similar to that explained for a-Si:H TFTs [Klauk *et al*, 2007]. In second case, when devices are repeatedly operated, a shift in threshold voltage is observed. Both of the above issues are cause of concern for electrical stability of devices; due to these stability issues the organic TFT devices cannot be reliably used in commercialized systems. Hence producing stable and reliable devices is extremely essential for organic electronics to succeed.