4
Bias-stress Stability of Flexible Organic TFTs

The bias-stress stability of low-voltage flexible p-channel and n-channel organic TFTs based on six promising organic semiconductors is demonstrated in this Chapter. The influence of the choice of the organic semiconductor and the applied gate-source and drain-source voltages on the bias-stress-induced decay of the on-state drain currents is studied. The results are benchmarked with metal oxide and a-Si:H TFTs, and some of the fabricated organic TFTs perform as high as a-Si:H TFTs.

4.1 INTRODUCTION

Organic TFTs have high potential to be used in driving circuitry of flexible, large-area electronic applications [Zhou *et al*, 2006; Yagi *et al*, 2008; Nakajima *et al*, 2009; Noda *et al*, 2011; Fujisaki *et al*, 2012; Steudel *et al*, 2012]. For example, in an AMOLED display, each pixel contains several TFTs, one of which has the task of supplying the electric current that is required to drive the OLED of that pixel to the specified brightness. Since the brightness (luminance) of organic LEDs is typically a steep function of the electric current flowing through the LED [Meerheim *et al*, 2011], the long-term stability of the drain current of the drive TFTs in AMOLED displays during continuous on-state biasing is very important. For all the organic electrical circuit, the high electrical stability is essential to achieve reliable operation of the devices.

For analog applications, the accepted change in the TFT devices can be within few percentages, however, for digital circuits, a change of 10-20% may be accepted. In TFTs based on disordered materials, such as a-Si:H, amorphous or polycrystalline metal oxides, and conjugated organic semiconductors, the stability of the on-state drain current during continuous operation is typically limited by the bias-stress effect. Hence, for real-life applications it is very important to expose the organic TFTs to real-life bias conditions which they have to deal with to visualize their efficiency and reliability.

4.2 BIAS-STRESS

For bias-stress measurements, a constant continuous voltage signal [Street *et al*, 2006; Kalb *et al*, 2007; Colleaux *et al*, 2011; Bobbert *et al*, 2012] or an alternating voltage signal [Salleo and Street, 2003; Richards and Sirringhaus, 2008; Tiwari *et al*, 2009] is applied to the gate, source and drain terminals of organic TFTs for long-duration of time-intervals, and the device on current as well as other important factors such as effective mobility and threshold voltage are monitored as a function of time. Figure 4.1 shows the schematic diagram showing the set-up used for bias-stress measurements. A continuous constant voltage-bias at source, drain and gate terminal were applied and changes in device parameters are monitored with time.

Ideally for an electrically stable device, on-current should not change with time upon applying constant continuous voltages in device. However, in practical scenario, the device on-current decreases with time due to non-idealities in the transistor. The non-idealities such as localized states or defects trap the free mobile charge-carriers, leading to the formation of immobile trapped charge-carriers. These immobile trapped charge-carriers continue to

contribute in the charge neutrality. However, they no longer contribute to the flow of current from source to drain, which leads to shift in the threshold voltage and drop in the drain current during bias-stress. The drop in device current is also seen in case for a-Si:H TFTs, which is currently used as a driver circuit in AMOLED displays.

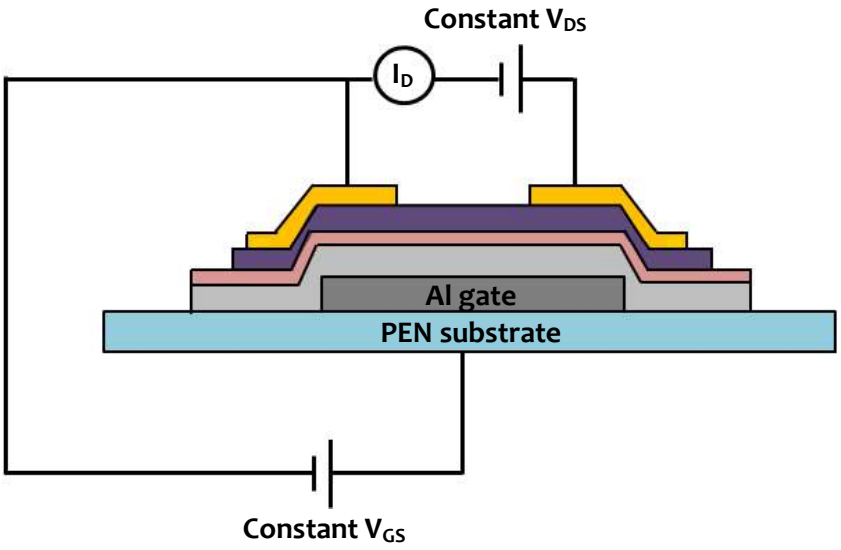

Figure 4.1 : Schematic diagram showing the Set-up Used for Bias-stress Measurements; where Negative (Positive) Voltages are Applied for p-channel (n-channel) TFTs to Operate the Device in On State

A useful basis for meaningful comparisons of the stability against this bias-stress-induced current decay among TFTs based on different materials and/or different technologies is the 10%-current-decay lifetime, which is defined as the time until the drain current drops to 90% of its initial value [Hekmatshoar *et al*, 2009]. The large extent to which the 10%-current-decay lifetime depends on the applied gate-source voltage was also demonstrated, making it necessary to measure it for a range of applied voltages for organic TFTs in order to facilitate useful benchmarking was also demonstrated [Hekmatshoar *et al*, 2009].

Figure 4.2 shows a graph plotted between the normalized drain current and stress duration where 10%-current-decay lifetime is determined to range from less than a minute (lowest process temperature, largest gate bias) to more than a decade (highest process temperature, smallest gate bias) for a-Si:H n-channel TFTs fabricated at substrate temperatures (temperature during semiconductor deposition) ranging from 200 ^{o}C to 350 ^{o}C and stressed with gate-source voltages ranging from 7.5 V to 120 V [Hekmatshoar *et al*, 2008; Hekmatshoar *et al*, 2009]. The reason behind this drop in device current for a-Si:H TFTs has been properly understood, and is considered to be due to the dangling bond formation in the bulk of a-Si:H, which is due to the weak Si-Si bond breaking and also due to the defects in the dielectric [Powell *et al*, 1989; Liu *et al*, 2012].

In organic TFTs the physical mechanisms and the analytical description of the bias-stress effect have been the subject of a large number of previous publications and reviews. Some of the studies in literature report that,
(i) bias-stress instability is due to the long-term charge trapping inside the semiconductor close to the dielectric interface and not to a structural change in the polymer, or due to the charge in the dielectric in organic TFTs [Salleo and Street, 2003; Häusermann and Batlogg, 2011]; (ii) charge trapping in stressed devices does not occur in the semiconductor but in the gate

dielectric, irrespective of p- or n-type operation using organic TFTs [Mathijssen *et al*, 2010]; (iii) presence of trace amounts of water in the organic layer of the transistor is the main reason behind the bias-stress instability [Gomes *et al*, 2006]; and (iv) presence of water and possible electrochemical process at the interfaces is the main reason behind the operational and bias-stress instability of p-channel organic TFTs [Kalb *et al*, 2007; K. Suemori *et al*, 2009; Zhang *et al*, 2009; Colleaux *et al*, 2011; Bobbert *et al*, 2012].

In addition, there are many reports discussing about how the bias-stress stability of organic TFTs is affected by various other parameters, such as,
(i) TFT architecture; which shows that bias-stress stability of the staggered devices is better than the coplanar devices [Richards and Sirringhaus, 2008], (ii) the presence of grain boundaries in the organic semiconductor [Häusermann and Batlogg, 2011], (iii) the material chosen for the source and drain contacts; where n-channel organic TFTs show better performance and stability for calcium electrodes than gold [Tiwari *et al*, 2009], (iv) the application of encapsulation and post-process anneal, which suppresses the DC bias stress-induced degradation [Sekitani *et al*, 2005], and (v) the magnitude of the applied gate-source and drain-source voltages [Street *et al*, 2006; Hsiao-Wen and Shin-Chin, 2008; Tiwari *et al*, 2009; Zschieschang *et al*, 2009].

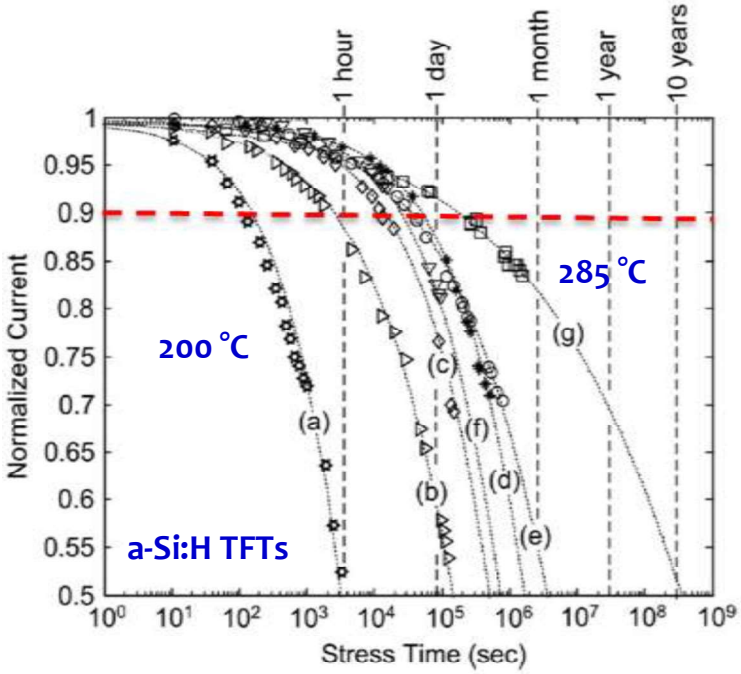

Figure 4.2 : Development of Normalized Drain Current of a-Si:H TFTs in Saturation Region at a Constant Gate Field of ~2.5 × 10^5 V/cm [Hekmatshoar *et al*, 2008]

Hence, there is a huge lack of understanding regarding the location of trapped carriers, which is still deceptive. So, there are various measures to obtain high performance bias-stable organic TFTs. Some of them are: to develop and use the materials (for semiconductor and dielectric) with no or very few defects; making the surface of dielectric as hydrophobic and improving the interfaces within organic TFTs; and using the staggered device architecture instead of coplanar architecture. It was reported that combining the organic semiconductor with a hydrophobic SAM results in excellent electrical characteristics, which are hardly affected by long-term gate bias stress [Kalb *et al*, 2007]. With a few exceptions [Sekitani *et al*, 2005; Hwang *et al*, 2011; Fujisaki *et al*, 2012; Zschieschang *et al*, 2012], the organic transistors examined in all the

above mentioned reports were all fabricated on rigid Si or glass substrates. Since conclusions drawn from bias-stress experiments conducted on TFTs fabricated on Si or glass substrates are not necessarily applicable to TFTs fabricated on plastic substrates (for example, due, to the impact of surface roughness [K. Suemori *et al*, 2009] and thermal budget [Hekmatshoar *et al*, 2008]). Hence, it is very important to investigate and benchmark the bias-stress stability of organic TFTs specifically fabricated on plastic substrates.

Here bias-stress stability of all the flexible p-channel and n-channel organic TFTs, which is already demonstrated and discussed in Chapter 3 are compared. The device structure of these TFTs is already shown in Figure 3.1. The six organic semiconductors employed in this study are pentacene, DNTT, C_{10}-DNTT, and DPh-DNTT for the p-channel TFTs, as well as F_{16}CuPc and NTCDI for the n-channel TFTs whose chemical structure is given in Figure 3.3 and 3.4. The p-channel organic TFTs exhibit field-effect mobilities in range of 0.5 to 4 cm^2/Vs, while the other two electron-transport semiconductors have shown great potential for the realization of organic n-channel TFTs with good air stability. All fabricated TFTs in this study have L of 30 μm and a W of 100 μm. All measurements were performed in ambient air at room temperature.

4.3 BIAS-STRESS MECHANISM

The operation of TFTs based on disordered materials, such as a-Si:H, amorphous or polycrystalline metal oxides, and conjugated organic semiconductors is typically limited by the bias-stress effect *i.e.*, by the time-dependent trapping of charges from the gate-induced carrier channel into localized defect states in the semiconductor, in the gate dielectric, and/or at the semiconductor/dielectric interface. As discussed in Section 4.2, the location of the trapped charge-carriers is very illusive and it is hugely dependent on the materials used for the formation of dielectric and organic semiconductor during the fabrication of organic TFTs.

While the trapped charges no longer contribute to the drain current, they continue to contribute to the charge balance of the transistor, so that the time-dependent decay in the on-state drain current during bias stress is accompanied by a time-dependent shift of the threshold voltage of the transistor which limits the stability of the on-state drain current and is termed as bias-stress effect. This threshold voltage shift is in the direction of the applied gate-source voltage (*i.e.* in negative direction for p-channel TFTs and in positive direction for n-channel TFTs), and is considered to be the main reason of the bias-stress induced decay of the drain current.

4.4 RESULTS AND DISCUSSIONS

For studying the bias-stress effect, the decay in drain current with time were measured and compared for various conditions by plotting the graphs between change in normalized drain current and time. The 10%-current-decay lifetime is calculated for these graphs to study the effect of applying different gate-source and drain-source voltages on bias-stress induced decay of drain current. In addition, the effect on drain current during bias-stress, due to the use of different organic semiconductors is also studied. The device characteristics before and after bias-stress; and after relaxation of devices from bias-stress are also discussed here. Finally, the bias-stress measurement results of fabricated organic TFTs in this study are compared between with different technologies.

4.4.1 Influence of Applied Voltages

The influence of applied gate-source and drain-source voltages ranging from ±2.0 V to ±3.0 V (corresponding to gate fields ranging from 3.8 to 5.5 MV/cm) on the drain current for all fabricated organic TFTs are discussed here. This is a useful range of gate-source voltages for the TFTs employed in this study, since gate-source voltages below ±2.0 V will be too close to the threshold voltage for some of the semiconductors, while gate-source voltages above ±3.0 V

might damage the gate dielectric when applied over extended periods of time. The drain-source voltage was either set to be equal to the applied gate-source voltage (V_{GS} = V_{DS}) or was set to ±3.0 V; this corresponds to a range of biasing conditions that is representative for those under which the drive TFTs in AMOLED display pixels operate most of the time. Identical measurements were carried out on all six p-channel and n-channel organic TFTs demonstrated in Chapter 3. It is important to note that each bias-stress measurement was conducted on a fresh (*i.e.*, not previously stressed) transistor.

Figure 4.3 shows how the drain current of flexible organic p-channel TFTs (a) pentacene, (b) DNTT, (c) C_{10}-DNTT, and (d) DPh-DNTT; and n-channel TFTs (e) F_{16}CuPc and (f) NTCDI changes over time during continuously applied voltage in a range of ± 3.0 V and ± 2.0 V with the condition of equal voltages at gate-source and drain-source terminals *i.e.* V_{GS} = V_{DS}. These graphs are plotted between normalized drain current and duration for which continuous voltages were applied on the device. The straight dotted line (blue color) corresponding to 0.9 value of the normalized drain current indicates the value at which the drain current drops by 10% of initial value of the drain current, referred as 10%-current-decay lifetimes. The black, red, and blue curves corresponds to the normalized drain current when applied voltages at gate-source and drain source are -3.0 V, -2.5 V, and -2.0 V, for p-channel organic TFTs and +3.0 V, +2.5 V, and +2.0 V, for n-channel TFTs. The extracted 10%-current-decay lifetime increases from 3,500 sec to 69,000 sec on lowering the applied voltages from V_{GS} = V_{DS} = -3.0 V to V_{GS} = V_{DS} = -2.0 V for pentacene TFTs. Similarly, for other p-channel organic TFTs *i.e.* DNTT, C_{10}-DNTT, and DPh-DNTT; 10%-current-decay lifetime increases from 27,000 sec to 364,000 sec; 20,000 sec to 40,000 sec; and 115,000 sec to 502,000 sec, respectively on lowering the applied voltages from V_{GS} = V_{DS} = -3.0 V to V_{GS} = V_{DS} = -2.0 V. For n-channel organic TFTs, the extracted 10%-current-decay lifetime increases from 15 sec to 290 sec on lowering the applied voltages from V_{GS} = V_{DS} = +3.0 V to V_{GS} = V_{DS} = +2.0 V for F_{16}CuPc TFTs, and on applying the same set of voltages to NTCDI TFTs, 10%-current-decay lifetime increases from 550 sec to 7,300 sec.

For the other set of measurements, the constant drain-source voltage and three different gate-source voltages were applied. Figure 4.4 shows the variation of normalized drain current with time during bias-stress. The black, purple, and orange curves indicate the change of the drain current when applied voltages at drain-source is -3.0 V; for p-channel TFTs and +3.0 V for n-channel TFTs, and applied voltage at gate-source is -3.0 V, -2.5 V, and -2.0 V, for p-channel organic TFTs and 3.0 V, 2.5 V, and 2.0 V, for n-channel TFTs. The extracted 10%-current-decay lifetime of pentacene TFTs increases from 3,500 sec to 22,000 sec on lowering the applied voltages at gate-source from V_{GS} = -3.0 V to V_{GS} = -2.0 V, during V_{DS} = -3.0 V. Similarly, for other p-channel TFTs *i.e.* DNTT, C_{10}-DNTT, and DPh-DNTT; 10%-current-decay lifetime increases from 27,000 sec to 417,000 sec; 20,000 sec to 32,000 sec; and 115,000 sec to 145,000 sec, respectively on lowering the applied voltages at gate-source from V_{GS} = -3.0 V to V_{GS} = -2.0 V, during constant drain-source voltage of -3.0 V. For n-channel TFTs, the extracted 10%-current-decay lifetime increases from 15 sec to 480 sec for F_{16}CuPc TFTs and from 550 sec to 251,000 sec for NTCDI TFTs, on lowering the applied voltages at gate-source from V_{GS} = +3.0 V to V_{GS} = +2.0 V, during constant drain-source voltage of +3.0 V.

A closer examination of Figure 4.3 and 4.4 shows that the drain current does not decay monotonically over time during bias stress, especially for small applied gate-source voltages, *i.e.*, when the bias-stress effect is relatively small, the drain current actually *increases* during the first few hours of bias stress. This is believed to be due to an initial time-dependent decrease of the contact resistance, which is reported to remarkably decrease in pentacene TFTs on exposure to air [Kalb *et al*, 2007; Lu *et al*, 2011] and that has been confirmed to also occur in TFTs based on at least some of the organic semiconductors employed in the present study [U. Kraft *et al*, 2014]. However, the exact physical or chemical mechanism(s) responsible for this time-dependent decrease of the contact resistance are not yet clear.

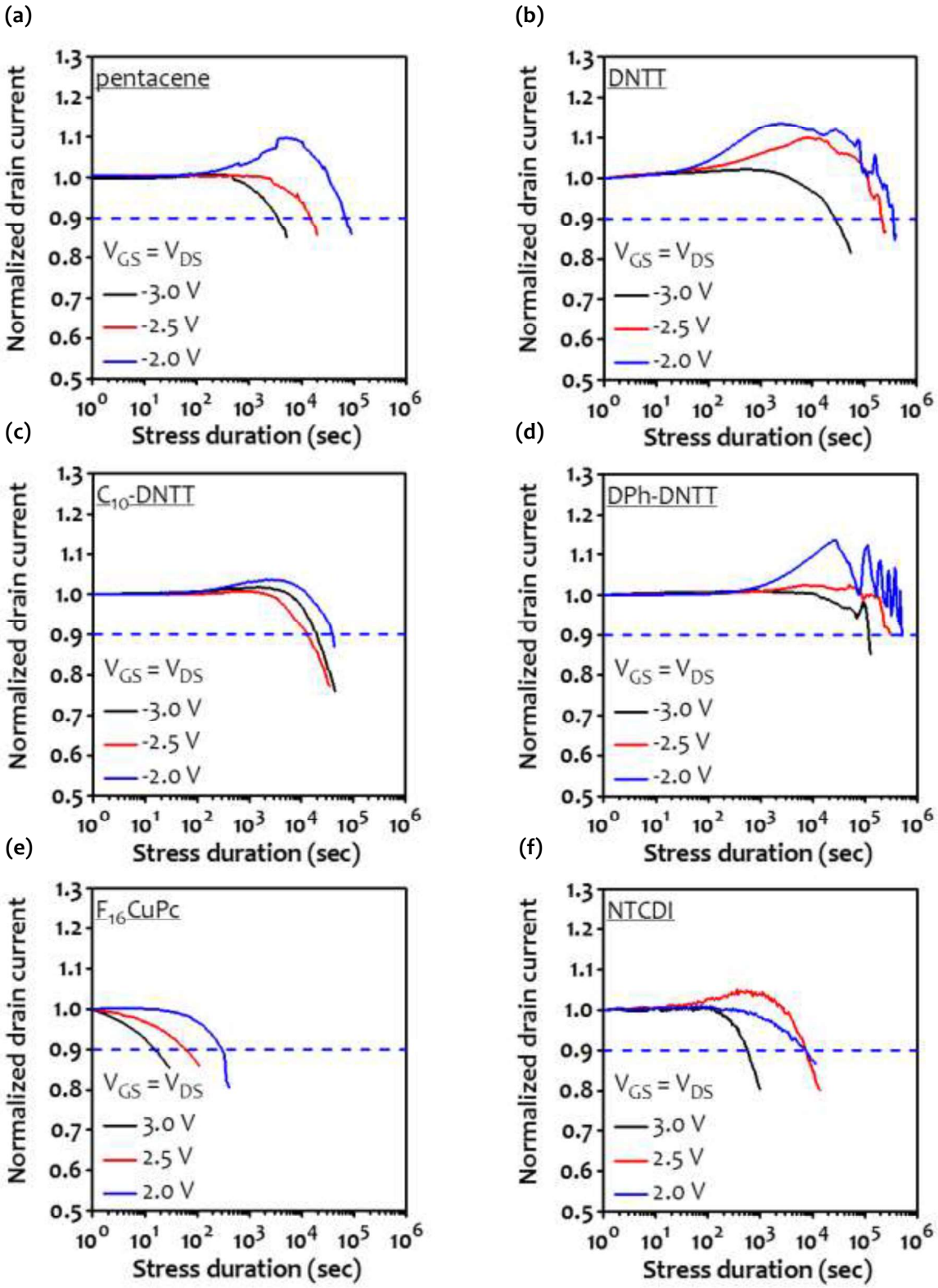

Figure 4.3 : Influence of Bias-stress on Normalized Drain Current over Time for (a) Pentacene, (b) DNTT, (c) C_{10}-DNTT, (d) DPh-DNTT, (e) F_{16}CuPc, and (f) NTCDI TFTs on Equal Applied Voltages at Gate-source and Drain-source *i.e.* $V_{GS} = V_{DS}$

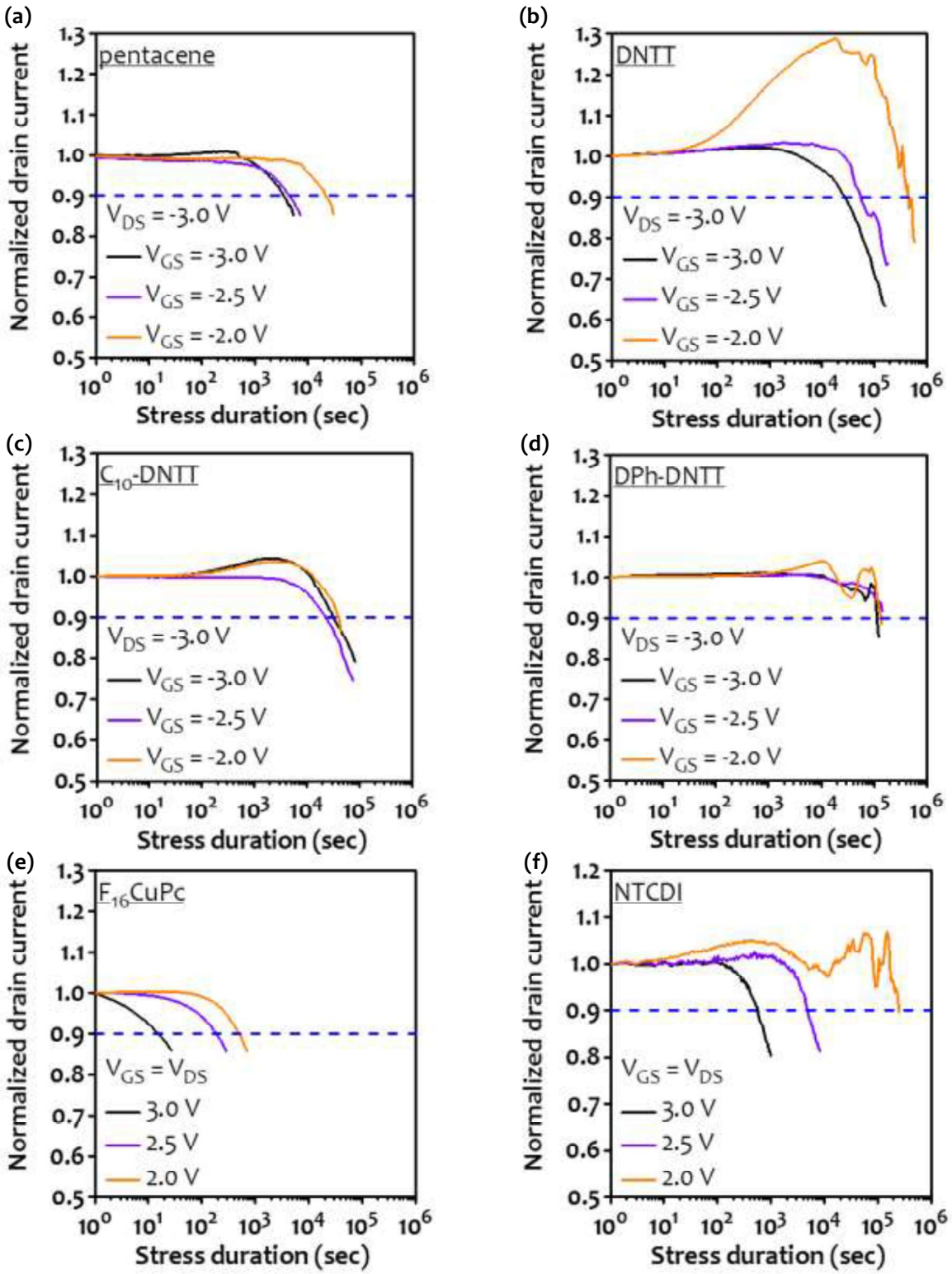

Figure 4.4 : Variation of Normalized Drain Current over Time for (a) Pentacene, (b) DNTT, (c) C_{10}-DNTT, (d) DPh-DNTT, (e) F_{16}CuPc, and (f) NTCDI TFTs when Constant Drain-source Voltage of ±3.0 V and Gate-source Voltage of ±3.0 V, ±2.5 V, and ±2.0 V are Applied

4.4.2 Dependence of Lifetime on Voltages and Semiconductors

The bias-stress stability of all the six organic semiconductors based TFTs, on various applied voltages are compared here in terms of 10%-current-decay lifetime. The variation of the drain current with the duration for which continuous voltages were applied at gate-source and drain-source terminals is shown in Figure 4.5.

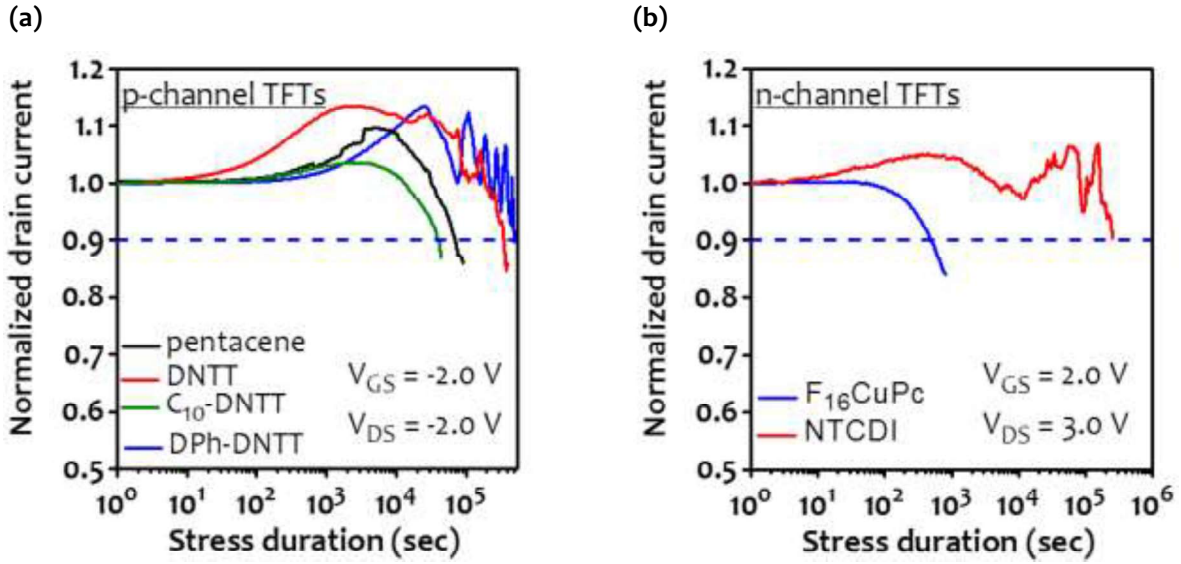

Figure 4.5 : Change of the Normalized Drain Current with Time for (a) p-channel (Pentacene, DNTT, C_{10}-DNTT, and DPh-DNTT) TFTs on Applied Voltage of -2.0 V at Gate-source and Drain-source Terminals and (b) n-channel (F_{16}CuPc and NTCDI) TFTs during Applied Voltage of +3.0 V and +2.0 V at Drain-source and Gate-source Terminals, respectively

The graph in Figure 4.5(a) shows the comparison of bias-stress stability between various p-channel (pentacene, DNTT, C_{10}-DNTT, and DPh-DNTT) TFTs on the basis of decay of the drain current during applied voltage of -2.0 V at gate-source and drain-source terminals (V_{GS} = V_{DS} = -2.0 V). The black, red, green, and blue curves indicate the change of the drain current for pentacene, DNTT, C_{10}-DNTT, and DPh-DNTT based TFTs, respectively. The extracted 10%-current-decay lifetimes from this graph is 69,000 s for pentacene, 364, 000 s for DNTT, 40,000 s for C_{10}-DNTT, and 502, 000 s for DPh-DNTT TFTs.

Similarly, the graph given in Figure 4.5(b) is plotted between normalized drain current with time, showing the comparison of stability of various n-channel (F_{16}CuPc and NTCDI) TFTs, during continuous applied voltage of +2.0 V at gate-source and +3.0 V at drain-source terminals (V_{GS} = +2.0 V, V_{DS} = +3.0 V). The blue and red curves correspond to the change in normalized drain current for F_{16}CuPc and NTCDI based organic TFTs. The extracted 10%-current-decay lifetimes from this curve is 480 s for F_{16}CuPc and 251, 000 s for NTCDI TFTs.

From all the bias-stress measurements, the 10%-current-decay lifetime for p-channel and n-channel organic TFTs were extracted. The 10%-current-decay lifetime of all these TFTs are plotted as a function of the applied gate-source voltages in Figure 4.6. The graph given in Figure 4.6(a) is plotted for p-channel organic TFTs, showing the measurement results when applied drain-source voltage is identical to gate-source voltage; whereas Figure 4.6(b) shows the results of p-channel TFTs, for drain-source voltage of -3.0 V, and gate-source voltage of -3.0 V, -2.5 V, and -2.0 V. Similarly, the measurement results of n-channel organic TFTs is shown in Figure 4.6(c), where applied drain-source voltage is identical to applied gate-source voltage; and

Figure 4.6(d), shows the result for drain-source voltage of +3.0 V, and gate-source voltage of +3.0 V, +2.5 V, and +2.0 V.

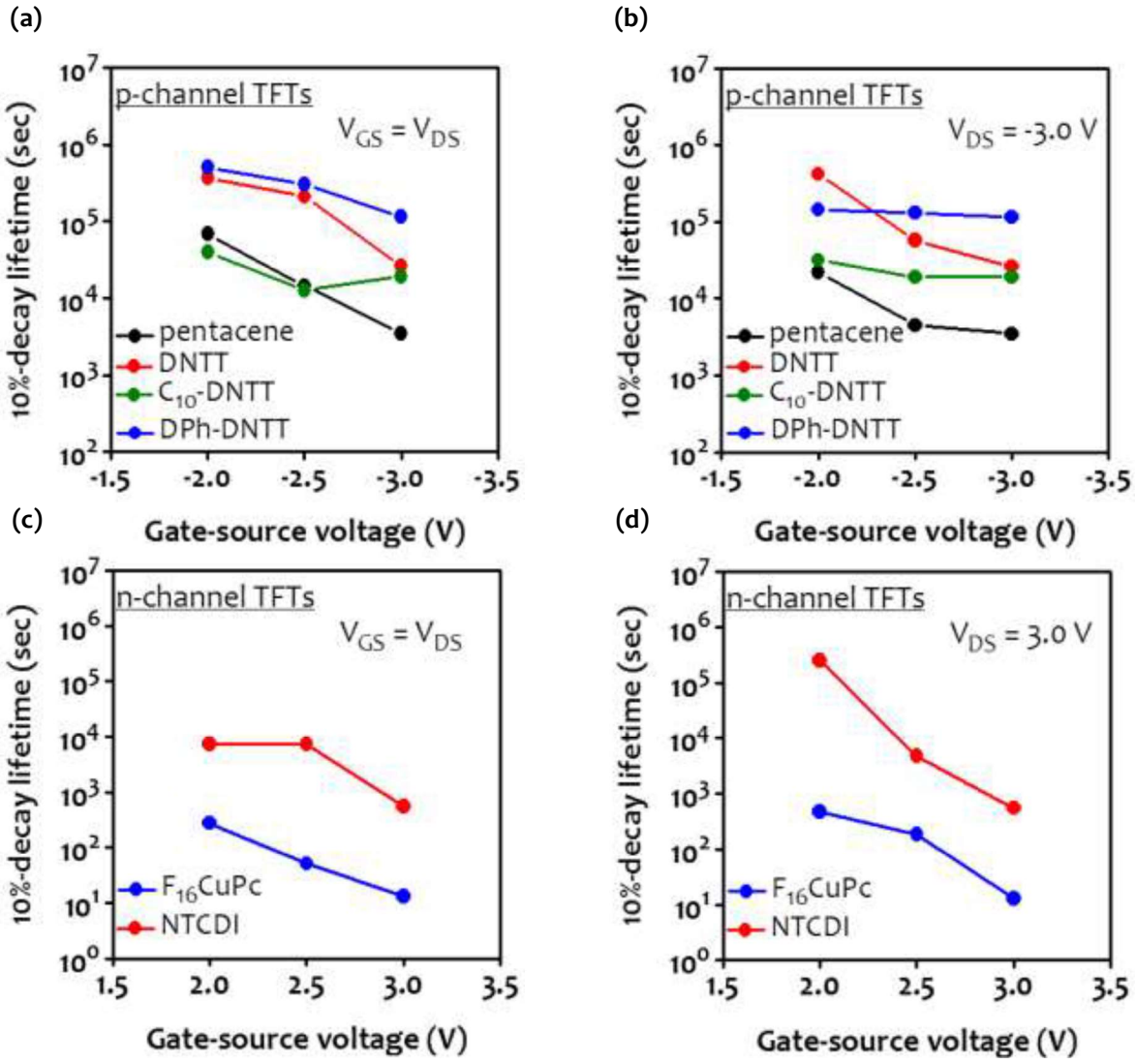

Figure 4.6 : 10%-current-decay Lifetimes Plotted as a function of the Applied Gate-source Voltage for (a) p-channel TFTs (Pentacene, DNTT, C_{10}-DNTT, and DPh-DNTT) when $V_{GS}=V_{DS}$, (b) p-channel TFTs when V_{DS} = -3.0 V, (c) n-channel TFTs (F_{16}CuPc and NTCDI), when $V_{GS}=V_{DS}$, and (d) n-channel TFTs whenV_{DS} = +3.0 V

The 10%-current decay lifetime for p-channel and n-channel TFTs is summarized in Table 4.1 and 4.2, respectively. These results indicate that, depending on the choice of the semiconductor and on the voltages applied during bias stress, the 10%-lifetime of the flexible pentacene, DNTT, C_{10}-DNTT, DPh-DNTT, F_{16}CuPc and NTCDI TFTs range from 15 seconds to about 1 week. The results confirm that a larger applied gate-source voltage generally leads to a shorter 10%-lifetime and *vice versa*, as was previously reported by Hekmatshoar *et al* [Hekmatshoar *et al*, 2009] and others [Street *et al*, 2006; Hsiao-Wen and Shin-Chin, 2008; Zschieschang *et al*, 2009]. In principle, these results also allow conclusions regarding the bias-stress stability of organic TFTs depending on the choice of the semiconductor. However, it should be noted that since the TFTs with different semiconductors can have different threshold voltages (see Table 3.1), the same applied gate-source voltage will induce a different density of

charge-carriers in the channel of TFTs, which in turn may result in a different trap rate during bias stress. To account for this, it is important to plot the 10%-current-decay lifetime as a function of gate overdrive voltage *i.e.* the difference between the applied gate-source voltage and the threshold voltage (see Figure 4.7).

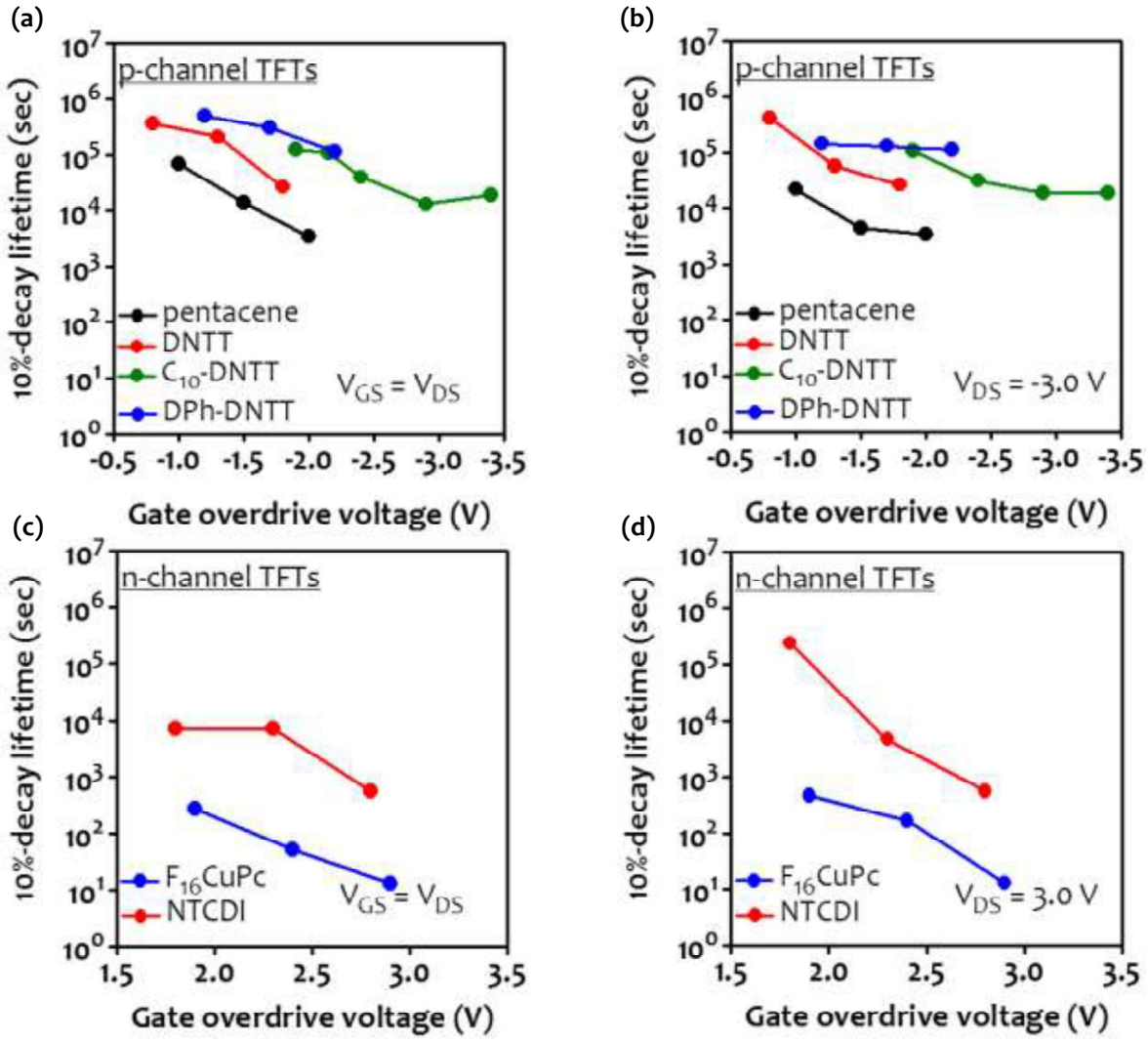

Figure 4.7 : 10%-current-decay Lifetimes Plotted as a function of the Gate Overdrive Voltage (Difference between the Applied Gate-source Voltage and the Threshold Voltage of the TFT) for (a) p-channel TFTs (Pentacene, DNTT, C_{10}-DNTT, and DPh-DNTT) when $V_{GS}=V_{DS}$, (b) p-channel TFTs when V_{DS} = -3.0 V, (c) n-channel TFTs (F_{16}CuPc and NTCDI), when $V_{GS}=V_{DS}$, and (d) n-channel TFTs when V_{DS} = +3.0 V

Figure 4.7 shows the 10%-current decay lifetimes plotted as a function of gate overdrive voltage (V_{GS}-V_{th}). As can be seen, for the p-channel TFTs, DPh-DNTT and C_{10}-DNTT provide somewhat better stability than DNTT, which shows better stability than pentacene. For the n-channel TFTs, the results show that in addition to substantially larger electron mobility, NTCDI also provides significantly better bias-stress stability over the entire range of gate-source and drain-source voltages compared to F_{16}CuPc. In general, the p-channel TFTs examined in this study all provide larger carrier mobilities and better bias-stress stability compared to the n-channel TFTs.

Table 4.1 :10%-current Decay Lifetimes Measured during Bias Stress under Five Different Bias Conditions for Flexible p-channel TFTs

V_{GS}	V_{DS}	pentacene	DNTT	C_{10}-DNTT	DPh-DNTT
-2.0 V	-2.0 V	69,000 s	364,000 s	40,000 s	502,000 s
-2.5 V	-2.5 V	14,000 s	209,000 s	13,000 s	302,000 s
-3.0 V	-3.0 V	3,500 s	27,000 s	20,000 s	115,000 s
-2.5 V	-3.0 V	4,500 s	58,000 s	20,000 s	132,000 s
-2.0 V	-3.0 V	22,000 s	417,000 s	32,000 s	145,000 s

Table 4.2 :10%-current Decay Lifetimes Measured during Bias Stress under Five Different Bias Conditions for Flexible n-channel TFTs

V_{GS}	V_{DS}	F_{16}CuPc	NTCDI
2.0 V	2.0 V	290 s	7,300 s
2.5 V	2.5 V	55 s	7,300 s
3.0 V	3.0 V	15 s	550 s
2.5 V	3.0 V	185 s	4,800 s
2.0 V	3.0 V	480 s	251,000 s

4.4.3 Effect of Bias-stress on Electrical Characteristics

During continuous application of constant gate-source and drain-source voltages the on-state drain current can be expected to decay over time, due to the trapping of charges from the gate-induced carrier channel into localized states. Concurrent with the observed bias-stress-induced decay of the on-state drain current, the threshold voltage of the TFTs will shift in the direction of the gate-source voltage applied during bias stress, *i.e.*, towards more negative threshold voltages in the case of p-channel TFTs and towards more positive threshold voltages in the case of n-channel TFTs.

Figure 4.8 shows the change in the electrical characteristics for p-channel TFTs, after applying continuous constant voltages at gate-source and drain-source terminals, until drain current drops to at least 10% of its initial value. For these experiments, the transfer characteristics were measured once before the bias stress experiment and again immediately after completion of the experiment.

The shift in the transfer and output characteristics of DPh-DNTT TFTs produced after applying -2.0 V at gate-source and drain-source terminals for a duration of 500,000 sec is shown in Figure 4.8(a & b). The black and red curves indicate measurement results obtained before and after stress, respectively. The extracted threshold voltage and field-effect mobility for DPh-DNTT TFTs, before and after bias-stress are -0.5 V and 1.8 cm^2/Vs; and -0.7 V and 1.8 cm^2/Vs, respectively. Similarly, Figure 4.8(c & d) shows the shift in the transfer and output characteristics of DNTT TFTs produced after applying -2.0 V at gate-source and drain-source terminals for the duration of 540,000 sec. The extracted threshold voltage and field-effect mobility before and after bias-stress for these TFTs are -1.2 V and 1.8 cm^2/Vs; and -1.7 V and 1.0 cm^2/Vs, respectively. The extent of this bias-stress-induced threshold voltage shift produced by one particular bias-stress condition ($V_{GS} = V_{DS} = -2.0$ V) for DPh-DNTT and DNTT based TFTs show that the smallest threshold-voltage shifts are seen for the DPh-DNTT TFTs. The threshold-voltage shift of -0.2 V ($\Delta V_{th} = -0.2$ V) is seen for DPh-DNTT TFTs after 138 hours of bias stress and for DNTT TFTs, the threshold-voltage shift of -0.5 V is seen after 150 hours of bias-stress.

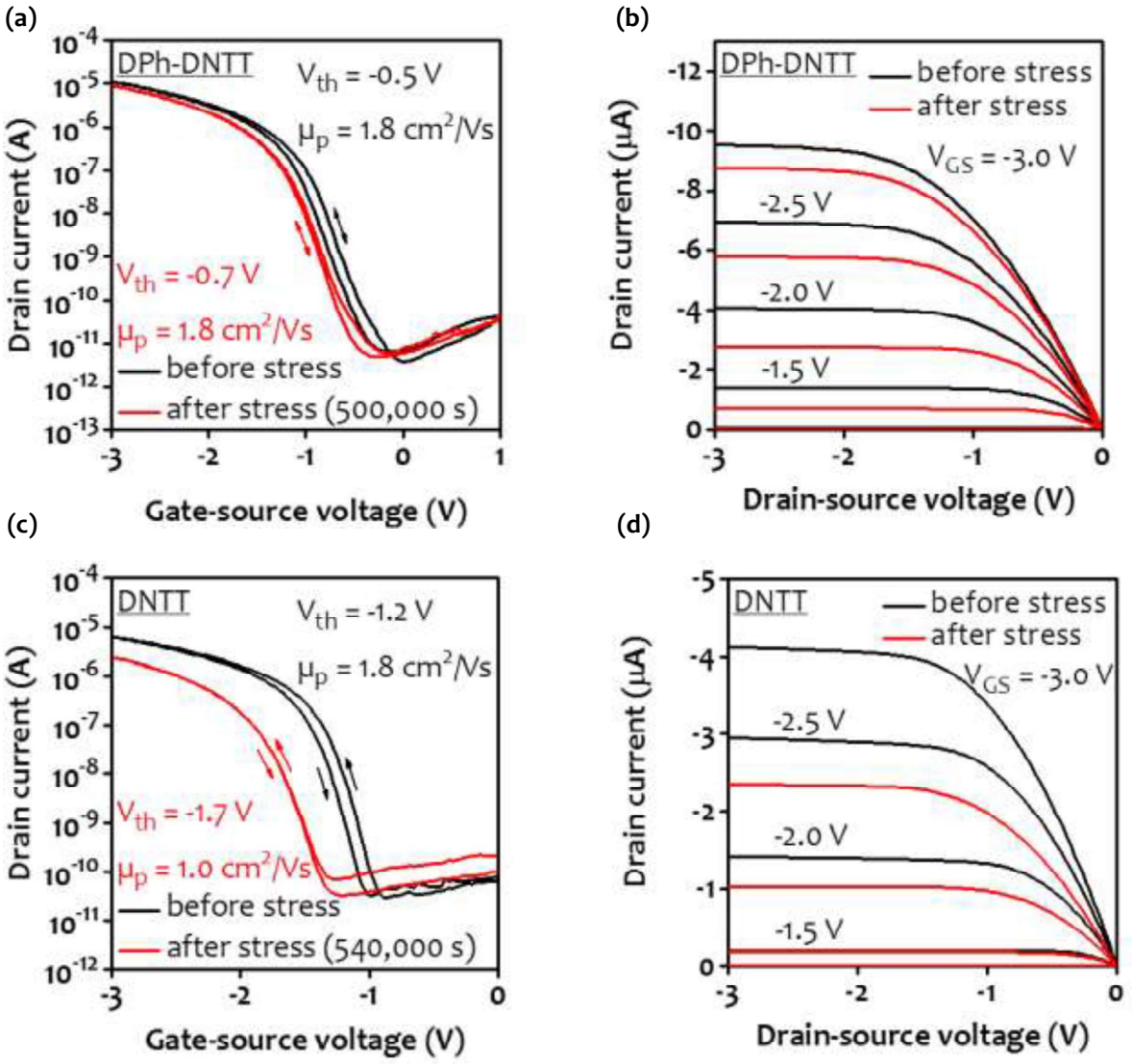

Figure 4.8 : Measured Electrical Characteristics for p-channel TFTs: (a) Transfer and (b) Output Characteristics; of DPh-DNTT TFTs Before and After Stress Produced on Applying -2.0 V at Gate-source and Drain-source Terminals for 500,000 sec, (c) Transfer and (d) Output Characteristics; of DNTT TFTs Before and After Stress Produced on Applying -2.0 V at Gate-source and Drain-source Terminals for 540,000 sec, where Black and Red Curves Indicate Measurement Results Before and After Stress

The graphs given in Figure 4.9 show the change in the electrical characteristics due to bias-stress for n-channel TFTs, until which the drain current drop to at least 10% of its initial value. The variation of transfer and output characteristics for NTCDI TFTs produced after applying 2.0 V at gate-source and drain-source terminals for a duration of 230,000 sec is shown in Figure 4.9(a & b). The extracted threshold voltage and field-effect mobility for these TFTs, before and after bias-stress are 0.1 V and 0.16 cm^2/Vs; and 0.1 V and 0.12 cm^2/Vs, respectively. The graphs plotted in Figure 4.9(c & d) show the shift in the transfer and output characteristics for $F_{16}CuPC$ TFTs produced after applying 2.0 V at gate-source and drain-source terminals for the duration of 8,000 sec.

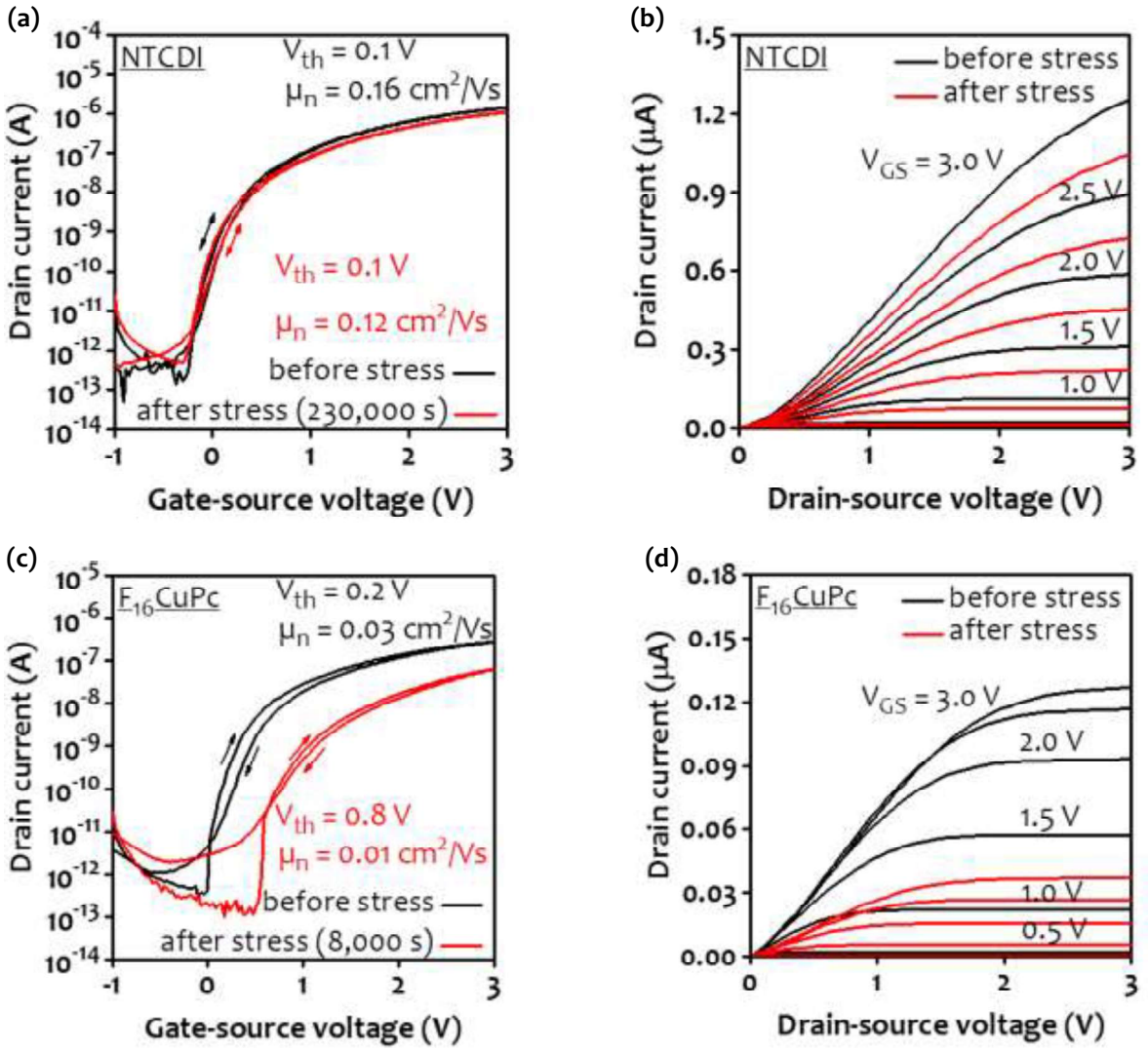

Figure 4.9 : Measured Electrical Characteristics for n-channel TFTs: (a) Transfer and (b) Output Characteristics; of NTCDI TFTs Before and After Stress Produced on Applying 2.0 V at Gate-source and Drain-source Terminals for 230,000 sec, (c) Transfer and (d) Output Characteristics; of F_{16}CuPc TFTs Before and After Stress Produced on Applying 2.0 V at Gate-source and Drain-source Terminals for 8,000 sec, where Black and Red Curves Indicate Measurement Results Before and After Stress

The extracted threshold voltage and field-effect mobility before and after bias-stress for these TFTs are 0.2 V and 0.03 cm²/Vs; and 0.8 V and 0.01 cm²/Vs, respectively. For n-channel organic TFTs, the smaller threshold-voltage shift is seen for the NTCDI TFTs (ΔV_{th} ~0 V) after 64 hours of bias stress as compared to F_{16}CuPc TFTs (ΔV_{th} ~0.6 V) after ~3 hours of bias stress. Higher shift in threshold voltage should result in higher decay of the drain current, leading to lesser values of 10%-current decay lifetime. The same results are reflected for all the fabricated TFTs for this study, whose 10% current decay lifetime was summarized in Table 4.1 and 4.2, and shift in threshold voltage can be seen from Figure 4.8 and 4.9. The reason behind DPh-DNTT and NTCDI TFTs, exhibiting high 10%-current decay lifetimes can be understood due to the minimum shift in threshold voltage of these TFTs as compared to other p-channel and n-channel TFTs, respectively.

A comparison of the transfer characteristics recorded before and after long-term bias stress further reveals that for some of the semiconductors investigated in this study, the carrier mobility decreases during bias stress. For example, the carrier mobility of the DNTT TFTs drops from 1.8 cm^2/Vs before bias stress to 1.0 cm^2/Vs after 110 hours of bias stress. It is important to note that this is not the intrinsic mobility of the semiconductor channel, but an effective (apparent) mobility that is extracted from the transfer characteristics and is smaller than the intrinsic channel mobility due to the influence of extrinsic factors, most importantly due to the contact resistance [Ante *et al*, 2012]. The changes in the performance parameters *i.e.* shift in threshold voltage (ΔV_{th}) and change in field-effect mobility ($\Delta\mu$) extracted from the transfer characteristics before and after stress for DPh-DNTT, DNTT, NTCDI and $F_{16}CuPc$ is summarized in Table 4.3. The probable reason for the degradation of observed field-effect mobility is due to the degradation of the organic semiconductor due to exposure to air (seen in Chapter 3), which would result in the decrease of the intrinsic channel mobility, or due to changes in extrinsic factors during bias-stress such as increase of the contact resistance; which would cause the effective mobility to decrease, even if the intrinsic mobility was not affected by the bias stress, and the same has been reported by Wang *et al* for pentacene TFTs [Wang *et al*, 2008; Yan *et al*, 2011].

Table 4.3 : Calculated Threshold Voltage Shift and Change in Effective Field-effect Mobility After Bias-stress for p-channel (DPh-DNTT and DNTT) and n-channel (NTCDI and $F_{16}CuPc$) TFTs, with Stress Duration

Semiconductor	Stress duration (sec)	$\lvert \Delta V_{th} \rvert$	$\Delta\mu$ (cm^2/Vs)
DPh-DNTT	500,000	~0.2 V	~0
DNTT	540,000	~0.5 V	~0.6
NTCDI	230,000	~0 V	~0.04
$F_{16}CuPc$	8,000	~0.6 V	~0.02

4.4.5 Effect of Relaxation on Electrical Characteristics

To test whether the degradation in the performance parameters of device is permanent or temporary, it is useful to monitor the relaxation of the transistors after bias stress. The reason is that in organic TFTs, the bias-stress-induced changes are usually not permanent, *i.e.*, after the applied voltages are reduced or removed, at least some of the trapped charge-carriers are released, the threshold voltage shifts back towards its initial value, and the original current-voltage characteristics are at least partially recovered. The same is observed for the DPh-DNTT and NTCDI TFTs. The electrical characteristics after relaxation of one p-channel and one n-channel organic TFTs is given in Figure 4.10.

The transfer and output characteristics showing the measurement results of before and after bias-stress of 132,000 sec, and after relaxation of devices; for DPh-DNTT TFTs is given in Figure 4.10 (a & b). The electrical characteristics for relaxation of these devices were calculated after 48 hours of relaxation of stressed devices. The black, red, and blue curves indicate the measurement results for before bias-stress, after bias-stress, and after relaxation of devices, respectively. Figure 4.10 (c & d) show the transfer and output characteristics of before and after bias-stress of 10,000 sec, and after relaxation of 24 hours for NTCDI TFTs. For both DPh-DNTT and NTCDI TFTs, an almost complete recovery of the original current-voltage characteristics is observed after a period of 1 or 2 days of relaxation with the transistor terminals floating. In those TFTs in which the bias stress had produced a notable drop in the effective mobility

(especially in the DNTT TFTs), a partial recovery of the effective mobility was observed (see Table 4.4). The extracted performance parameters such as threshold voltage and field-effect mobility obtained from the measurement results of before bias-stress, after bias-stress, after relaxation of devices for p-channel (DPh-DNTT and DNTT) and n-channel (NTCDI and $F_{16}CuPc$) TFTs are summarized in Table 4.4.

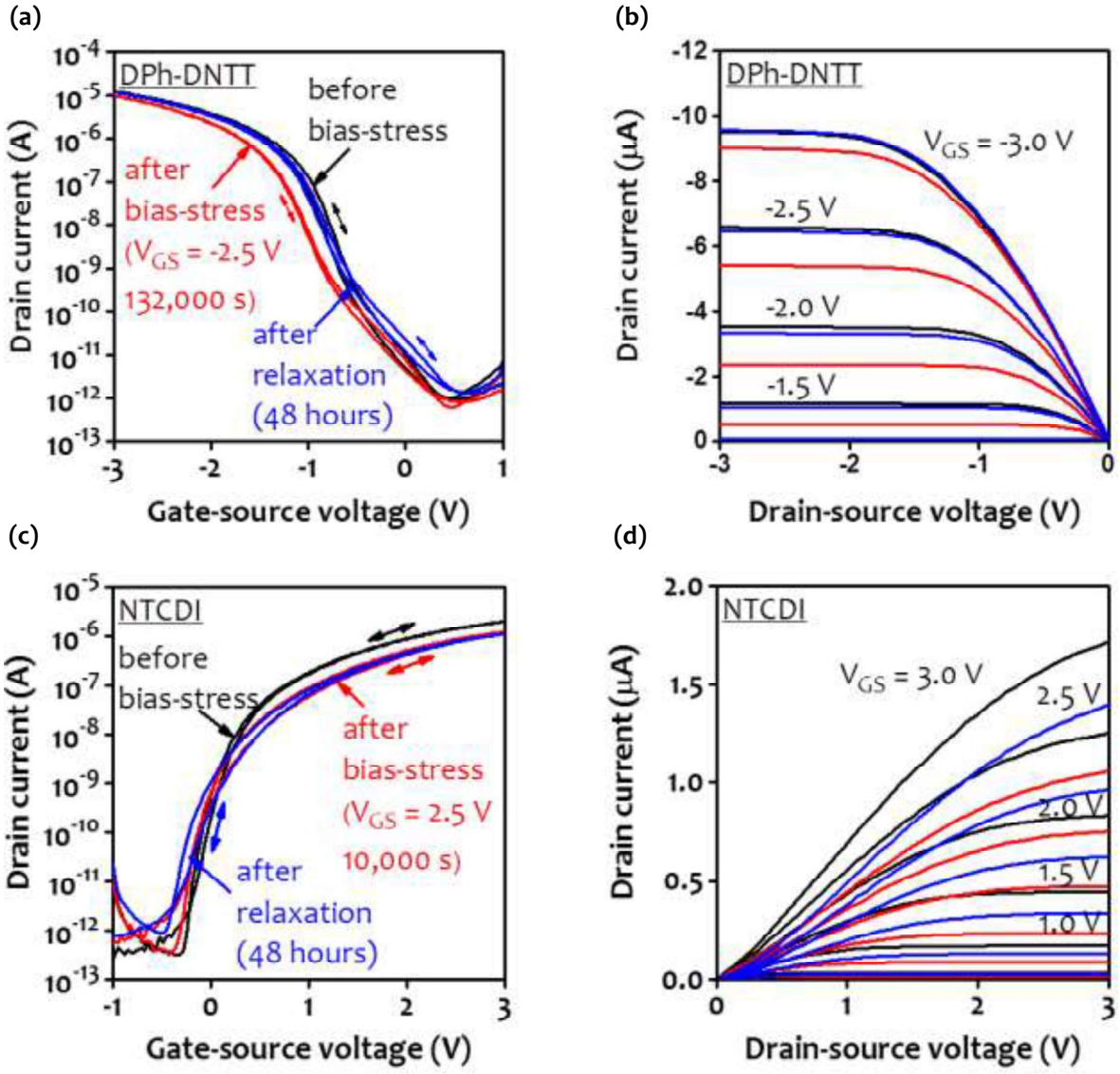

Figure 4.10 : (a) Transfer and (b) Output Characteristics; of DPh-DNTT (p-channel) TFTs, Measured Before Bias-stress on a Fresh Transistor, After Bias-stress for Duration of 132,000 sec, and After Relaxing these Devices for 48 hours, (c) Transfer and (d) Output Characteristics; of NTCDI (n-channel) TFTs, Measured Before Bias-stress, After Bias-stress for Duration of 10,000 sec, and After Relaxing these Devices for 24 hours, where Black, Red, and Blue Curves Indicate Measurement Results Before Stress, After Stress, and After Relaxation of Devices

The results indicate that the change in performance of device caused due to shift in threshold voltage and drop in effective field-effect mobility (due to trapping of charge-carriers and change in other factors during bias-stress) is completely or partially recoverable, and change in performance of device mainly caused due to degradation in intrinsic field-effect

mobility (due to degradation of material in ambient conditions) is not recoverable. Hence, air-stable and defect-free organic semiconductors are essential to obtain good bias-stress stability. The DPh-DNTT and NTCDI show very good bias-stress stability as compared to other p-channel and n-channel TFTs fabricated during this study.

Table 4.4 : Extracted Field-effect Mobility and the Threshold Voltage of DPh-DNTT, DNTT, NTCDI, and F_{16}-CuPc based TFTs, Calculated from the Electrical Characteristics Obtained Before Bias-stress, After Bias-stress, and After Relaxation of Devices

Semiconductor	DNTT	DPh-DNTT	F_{16}CuPc	NTCDI
Carrier type	p-channel TFT	p-channel TFT	n-channel TFT	n-channel TFT
V_{GS} during bias stress	-2.0 V	-2.0 V	2.0 V	2.0 V
V_{DS} during bias stress	-2.0 V	-2.0 V	3.0 V	3.0 V
Duration of bias stress	398,000 s	661,000 s	16,000 s	252,000 s
Effective mobility before bias stress	1.8 cm^2/Vs	1.8 cm^2/Vs	0.03 cm^2/Vs	0.16 cm^2/Vs
Effective mobility after bias stress	1.0 cm^2/Vs	1.8 cm^2/Vs	0.01 cm^2/Vs	0.13 cm^2/Vs
effective mobility after recovery	1.6 cm^2/Vs	1.8 cm^2/Vs	0.02 cm^2/Vs	0.12 cm^2/Vs
threshold voltage before bias stress	-1.2 V	-0.8 V	0.1 V	0.2 V
threshold voltage after bias stress	-1.7 V	-1.1 V	0.9 V	0.3 V
threshold voltage after recovery	-1.2 V	-0.8 V	0.8 V	0.2 V

4.4.6 Comparison between Various Technologies

To benchmark the 10%-current-decay lifetimes of TFTs fabricated using different materials or different technologies, it is useful to plot the graph between the 10%-current-decay lifetimes against the transistor's channel sheet resistance, which is inversely proportional to the field-effect mobility, the gate-dielectric capacitance per unit area and the applied gate-source voltage. Figure 4.11 summarizes some of the previously reported data for a-Si:H and metal-oxide TFTs

fabricated at various process temperatures ranging from 150 to 350 °C [Hekmatshoar *et al*, 2009; Riedl *et al*, 2007; Levy *et al*, 2008; Shinhyuk *et al*, 2011], and, for comparison the data obtained in this study for DPh-DNTT p-channel and NTCDI n-channel TFTs fabricated at process temperatures below 85 °C.

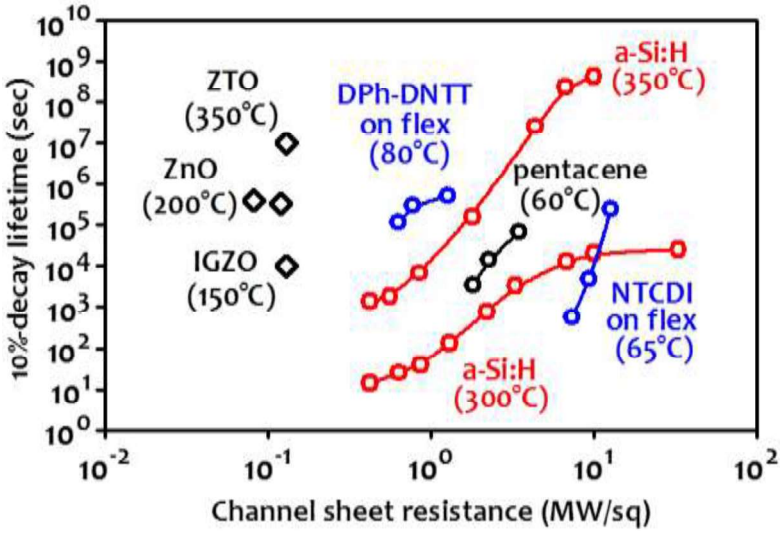

Figure 4.11 : Comparison of the Bias-stress Stability of TFTs Fabricated in various Technologies (a-Si:H, metal oxides, organic TFTs) on the basis of the 10%-current-decay Lifetime Plotted *versus* the Channel Sheet Resistance. The a-Si:H data were Taken from Reference [Source : Hekmatshoar *et al*, 2009], the Metal-oxide TFT Data were Taken from References [Source : Riedl *et al*, 2007; Levy *et al*, 2008; Shinhyuk *et al*, 2011] and the Organic-TFT Data were Taken from Table 4.1 and 4.2

For each data point, the channel sheet resistance was extracted from the output characteristics (drain current *vs.* drain-source voltage) measured before bias stress at the same gate-source voltage applied during the bias-stress experiment. From the data reported for a-Si:H and metal-oxide TFTs, two trends emerge. One is that for the same TFT, the 10%-lifetime is shorter when the channel sheet resistance is smaller, *i.e.*, when the gate-source voltage applied during bias stress is larger. This trend has been well documented [Street *et al*, 2006; Hekmatshoar *et al*, 2008; Hsiao-Wen and Shin-Chin, 2008; Hekmatshoar *et al*, 2009; Tiwari *et al*, 2009; Zschieschang *et al*, 2009] and is likely related to the fact that the gate-induced carrier density and hence the trapping rate increases on increasing the gate-source voltage. The second trend is that, the inorganic TFTs fabricated at higher process temperatures have longer 10%-lifetimes than inorganic TFTs fabricated at lower process temperatures [Hekmatshoar *et al*, 2009], which is likely related to the fact that in the fabrication of inorganic TFTs, higher process temperatures generally produce films and interfaces with smaller defect densities. However, process temperatures above ~200 °C make it difficult to fabricate the TFTs on flexible plastic substrates, which often have glass transition temperatures below ~200 °C. (Plastics with higher glass transition temperatures exist, but they tend to be more expensive than PEN and PET, which have glass transition temperatures below 150 °C.)

Figure 4.11 shows that the bias-stress stability of at least some of the organic p-channel TFTs investigated in this study is actually better than that of many inorganic TFTs, despite the fact that the organic TFTs were fabricated at much lower process temperatures on PEN substrates. But Figure 4.11 also shows that more work is needed to further improve the bias-stress stability of flexible organic n-channel TFTs.

4.5 CONCLUSIONS

The limitations of the performance and stability of low-voltage organic p-channel and n-channel flexible TFTs based on six promising organic semiconductors due to bias-stress has been studied in this Chapter. In these measurements, a continuous constant voltage is applied at gate-source and drain-source terminals of TFTs and drain current is measured with time. On the basis of the measurement results, normalized drain current is plotted as a function of time and 10%-current-decay lifetime is extracted.

On the basis of 10%-current decay lifetime, the dependence of applied continuous constant voltages at gate-source and drain-source terminals, on the bias-stress-induced decay of the on-state drain current for all the fabricated TFTs is studied. The results show that the 10%-current-decay lifetimes of the flexible pentacene, DNTT, C_{10}-DNTT, DPh-DNTT, F_{16}CuPc and NTCDI TFTs range from 15 seconds to about 1 week. This 10%-current-decay lifetime is larger for lower applied gate-source voltage and *vice versa*; because at lower applied gate-source voltage the amount of accumulated charges is less due to which the probability of these charge-carriers to trap is low. For the p-channel TFTs, DPh-DNTT and C_{10}-DNTT provide somewhat better stability than DNTT, which shows better stability than pentacene. For the n-channel TFTs, the results show that in addition to substantially larger electron mobility, NTCDI also provides significantly better bias-stress stability over the entire range of gate-source and drain-source voltages compared with F_{16}CuPc. In general, the p-channel TFTs examined in this study, provide larger carrier mobilities and better bias-stress stability compared to the n-channel TFTs.

The time-dependent decay in the on-state drain current during bias-stress is observed due to time-dependent shift of the threshold voltage of the transistor in negative (positive) direction for negative (positive) applied voltages for p-channel (n-channel) organic TFTs. This shift in the threshold voltage during bias-stress is due to trapping of charge-carriers in the localized states, and the same is observed in the device characteristics before and after long-term bias stress. A comparison of the transfer characteristics recorded before and after long-term bias stress further reveals that for some of the semiconductors investigated in this study, the field-effect mobility decreases during bias stress. The probable reason for the degradation in observed field-effect mobility is due to the degradation of the organic semiconductor due to exposure to ambient air, or due to changes in extrinsic factors during bias-stress such as increase of the contact resistance. The relaxation studies conducted in stressed organic TFTs reveal that the change in performance of device caused due to shift in threshold voltage and drop in effective field-effect mobility is completely or partially recoverable, and change in performance of device mainly caused due to degradation in intrinsic field-effect mobility is not recoverable. Hence, to minimize the bias-stress induced instabilities, it is required to use air-stable and defect-free materials for fabrication of organic TFTs. For TFTs based on at least some of the semiconductors investigated in this study, especially DPh-DNTT, the bias-stress stability is already comparable to that of a-Si:H and metal oxide TFTs, despite the fact that the organic TFTs were fabricated at significantly lower process temperatures, which is important in view of the fabrication of these devices on plastic substrates.