4

Mitigation of Destabilizing Effects of CPL in a Buck-Boost Converter Feeding a Composite Load

In the Chapter 3, mitigation of negative impedance instabilities in a dc/dc buck converter has been addressed using SMC approach. A dc microgrid can consists of a buck-boost converter to meet the specific voltage requirement of different loads and at times may be required to feed a CPL dominated load profile. Furthermore, in the event of unavailability renewable sources or grid connection, bidirectional buck-boost converters(BDCs), used to interface storage units in a dc microgrid or to interface two dc microgrids, may also need to supply a CPL dominated load profile. Under these situations, the controllers of the converters must have sufficient robustness to ensure the stability and the performance in face of CPL. In this chapter, mitigation of negative impedance instabilities in an inverted topology dc/dc buck-boost converter and a bidirectional dc/dc converter in the presence of CPL, is addressed using SMC approach. Both converters are assumed to operate in CCM.

The control of a dc/dc buck-boost converter is relatively more challenging as compared to dc/dc buck converter due to its non-minimum phase structure, making it unstable even with a resistive load [Kazimierczuk, 2008]. The presence of CPL further increases the nonlinearity of the buck-boost converter system, thereby increasing the challenge for the control. In such a situation, control designed through linear approaches proves to be insufficient, and presents a need to use nonlinear techniques to design robust controllers and to ensure system stability in a large-signal sense. Some researchers have used SMC approach to design control for buck-boost converter feeding a resistive load [Tan et al., 2006; Salazar et al., 2013; El Fadil and Giri, 2008]. However, considering recent developments in RESs based dc distribution systems comprising of tightly regulated POLCs, storage units with sophisticated charge controllers, the presence of, conventional constant resistance, constant current, and constant power loads, is inevitable. In the modern dc distribution systems, the dc/dc converters has to supply aforementioned load profile and ensure high quality of power supply to the sophisticated loads. Considering aforementioned developments, in the first section of this chapter, mitigation of negative impedance instabilities in an inverted topology dc/dc buck-boost converter feeding a composite load using SMC approach is addressed. The condition for the stability of the system is established and the performance of the proposed controller is validated through real-time simulation studies.

The second section of this chapter deals with mitigation of negative impedance instabilities in a BDC within an isolated dc microgrid (DCMG) environment in the presence of CPL. In dc microgrids, a BDC is used either to interface battery energy storage to dc bus, or to interconnect two neighboring dc microgrids [Kumar et al., 2015; Narasimharaju et al., 2010]. When interfacing battery energy storage, BDC facilitates bidirectional power exchange between dc bus and battery energy storage to regulates the dc bus voltage and to absorb short-time transients. Basically, the presence of BDC increases the system inertia and prevents instabilities [Inthamoussou et al., 2013; Zeng et al., 2015]. In the isloated DCMG under consideration, RESs operating in MPPT mode (behaving as CPSs) and CPL connected to the dc bus are aggregated in terms of net CPL power, which may be positive or negative. Therefore, BDC supplying this net CPL, selects its mode of operation based on the sign of net CPL power. A

robust SMC is proposed to ensure the tight regulation of dc bus voltage and system stability in different operating modes. The proof of existence of sliding mode and the stability of switching surface are also presented. The performance of the proposed SMC is validated though real-time simulation studies.

4.1 MITIGATION OF THE DESTABILIZING EFFECTS OF CPL IN BUCK-BOOST CONVERTER

In this section, mitigation of CPL induced negative impedance instabilities in a conventional dc/dc buck-boost converter feeding a composite load is addressed. The considered buck-boost converter is of non-isolated topology and assumed to operate in CCM. In the following section, mathematical modeling of the buck-boost converter feeding a composite load is presented.

4.1.1 Mathematical Modeling of Converter Supplying Composite Load

A circuit diagram of a dc/dc buck-boost converter supplying power to a composite load is shown in Figure 4.1. The converter is expected to regulate its output voltage at a desired level, which may be lower or higher than its input voltage depending on the mode of converter operation (buck or boost). The output voltage of this converter topology is of negative polarity. The input source to the converter may be the output of a rectifier unit or the output of an RES such as solar PV, fuel cells etc. The load profile is composite having constant resistance, constant current and constant power components. This is the most realistic load profile and includes all kinds of loads. For example, the storage batteries in an ac/dc microgrid behave as constant current load under constant current charging mode and tightly regulated POLCs in the multiconverter power distribution system behave as CPL. Conventional constant resistance dc loads such as heating and lighting loads, are very common to dc power systems from centuries, and are quite relevant even today.

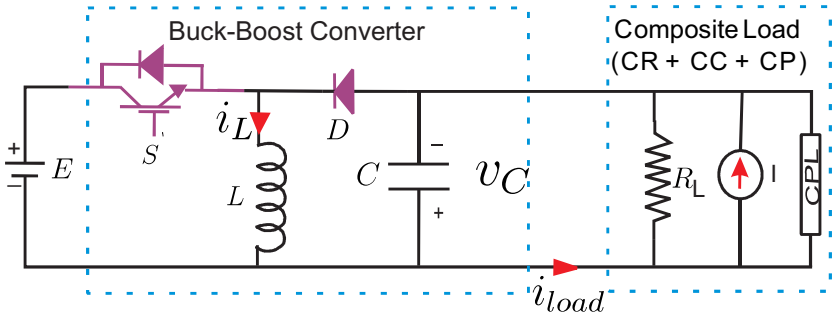

Figure 4.1 : Circuit diagram of dc/dc buck-boost converter feeding a composite load

The state-space averaged model of the system shown in Figure 4.1 can be represented by the following mathematical model

$$L\frac{di_L}{dt} = uE + (1-u)v_C \tag{4.1a}$$

$$C\frac{dv_C}{dt} = -(1-u)i_L - i_{Load} \tag{4.1b}$$

where inductor current i_L and capacitor voltage v_C are the state variables of the system. E is the input voltage. L and C are the converter's inductance and capacitance parameters respectively. $u \in \{0,1\}$, is the control input. The modeling of CPL also constrains the values of i_L and v_C. For a practical converter i_L and v_C have upper limits, therefore it is necessary to constrain the values of i_L and v_C. Furthermore, i_L and $v_C \in \Omega$ where set Ω is a subset of $\mathbb{R}^2$ i.e.,

$$i_L, v_C \in \Omega \subseteq \mathbb{R}^2 \setminus \{0\},\ i_L > 0\ v_C > 0 \tag{4.2}$$

Furthermore, the load current i_{load} drawn by the composite load is given by

$$i_{load} = \frac{v_C}{R_L} + i_{const} + \frac{P}{v_C};\ v_C > 0 \tag{4.3}$$

where P is the rated power of the CPL, and v_C is the capacitor voltage which is equal to output voltage of the converter. The load current i_{load} has three components: current drawn by resistive component R_L, constant current component i_{const}, and current drawn by the CPL. The motivation behind considering the model of the buck-boost converter of (4.1) is to make the destabilizing effect of CPL most pronounced. In practical converters, the presence of dissipative elements such as switch resistance, diode resistance, inductor and capacitor ESR; increase the natural damping of the system, thereby reducing the severity of CPL induced instability effects [Huddy and Skufca, 2013].

4.1.2 Sliding Mode Control Design

In this section, the design of a robust controller using SMC approach to mitigate the negative impedance instabilities in the buck-boost converter system of (4.1) is proposed. A new switching function is proposed to achieve control and performance objectives.

(a) Switching function

The first step in the design of a sliding-mode controller for a given system is to design a stable switching function. The proposed switching function is defined as

$$s := \beta_1(i_L - i_{Lref}) + \beta_2(v_C - v_{Cref}) + \beta_3 \int (v_C - v_{Cref})dt \tag{4.4}$$

where i_{Lref} and v_{Cref} are the reference values of i_L and v_C respectively. β_1, β_2, and β_3 are the parameters of the switching function. The second term of (4.4) requires reference of the inductor current, which depends on the input voltage and the load. Therefore, it is difficult to get the inductor current reference as the system input voltage and the load are dynamic variables. In order to overcome the problem in the estimation of inductor current reference, the inductor current is passed through a high pass filter to compute the inductor current error (i_L-i_{Lref}) [Santi et al., 2003; Mattavelli et al., 1993]. In steady-state the inductor current error is necessarily zero, therefore, in the absence of last term any nonzero value of switching function would indicate steady-state error in the voltage. The last term of switching function ensures zero steady state error in the output voltage [Mattavelli et al., 1993].

(b) PWM based SMC

To ensure fixed frequency switching and to reduce switching losses due to high frequency switching a PWM based SMC is proposed in this section. To compute the instantaneous duty cycle $u(t)$ of the PWM based SMC, the following reaching dynamics is used

$$\dot{s} = -\lambda s - Qsgn(s) \tag{4.5}$$

Where λ,Q>0 are the parameters of the reaching dynamics to control its convergence speed. Using (4.1), (4.4), and (4.5) and solving for $u(t)$ results in the instantaneous duty cycle of the converter

$$u(t) = \frac{\frac{\beta_2}{C} i_L + \frac{\beta_2}{C} i_{load} - \frac{\beta_1}{L} v_C - \beta_3(v_C - v_{Cref}) - \lambda s - Qsgn(s)}{\frac{\beta_1}{L} E - \frac{\beta_1}{L} v_C + \frac{\beta_2}{C} i_L} \tag{4.6}$$

The instantaneous duty cycle of converter $u(t)$ can be decomposed into two components namely; equivalent control u_{eq} (control that acts on the system under sliding mode), and discontinuous control u_N which ensures robustness against parameter uncertainties and the external disturbances during reaching phase. It decomposes the control law (4.6) as,

$$u(t) = u_{eq} + u_N \tag{4.7}$$

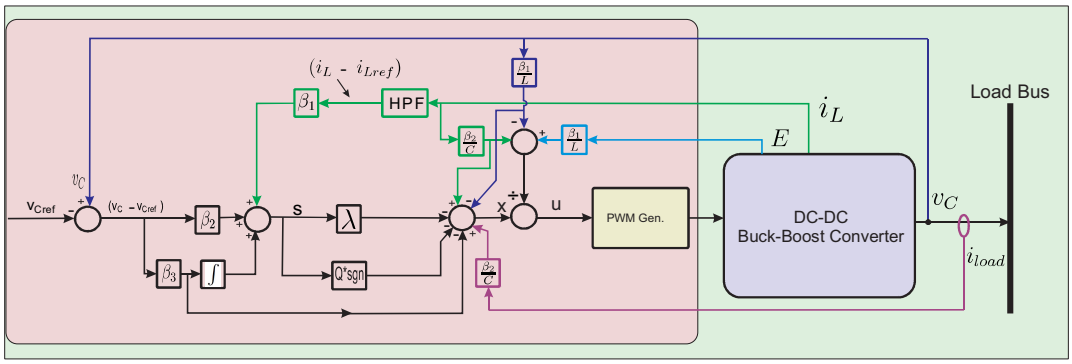

Figure 4.2 : The proposed sliding mode control scheme for buck-boost converter system

(c) Existence of sliding mode

It is straightforward to prove the reachability condition $s^T\dot{s} < -\eta|s|;\ \eta$ for the reaching dynamics of (4.5). This proof has been given in Chapter 2.

(d) Stability of the system at the switching surface

The reaching dynamics of (4.5) ensures that sliding mode $s = 0$ is reached in finite time. To ensure the system stability, trajectory from an arbitrary initial condition after reaching the switching surface $s = 0$, should be constrained to it with the control law (4.6) and converge towards the desired operating point along the switching surface. Sliding mode $s = 0$ implies

$$s := \beta_1(i_L - i_{Lref}) + \beta_2(v_C - v_{Cref}) + \beta_3 \int (v_C - v_{Cref})dt = 0 \tag{4.8}$$

Therefore, the reduced order system dynamics during sliding mode can be given by

$$i_{Lj} = -\frac{\beta_2}{\beta_1}(v_C - v_{Cref}) - \frac{\beta_3}{\beta_1}\int (v_C - v_{Cref})dt + i_{Lref} \tag{4.9a}$$

$$C\frac{dv_C}{dt} = -(1-u)i_L - i_{Load} \tag{4.9b}$$

Eliminating i_L, the reduced order dynamics of (4.9) becomes

$$C\frac{dv_C}{dt} - \frac{\beta_2}{\beta_1}(1-u)(v_C - v_{Cref}) - \frac{\beta_3}{\beta_1}(1-u)\int (v_C - v_{Cref})dt + \ldots \\ \ldots(1-u)i_{Lref} + i_{load} = 0 \tag{4.10}$$

Differentiating (4.10) with respect to time.

$$C\frac{d^2v_C}{dt^2} - \frac{\beta_2}{\beta_1}(1-u)\frac{dv_C}{dt} - \frac{\beta_3}{\beta_1}(1-u)(v_C - v_{Cref}) + \frac{di_{load}}{dt} = 0 \tag{4.11}$$

Considering linear approximation of the load current $i_{load}(v_C)$, $\frac{di_{load}}{dt}$ can be written as

$$\frac{di_{load}}{dt} \approx \frac{\partial i_{load}}{\partial v_C}\frac{dv_C}{dt} \approx \left(\frac{1}{R_L} - \frac{P}{v_{Cref}^2}\right)\frac{dv_C}{dt} \tag{4.12}$$

Substitution of (4.12) into (4.11) results in

$$C\frac{d^2v_C}{dt^2} + \left[\frac{1}{R_L} - \frac{P}{v_{Cref}^2} - \frac{\beta_2}{\beta_1}(1-u)\right]\frac{dv_C}{dt} - \frac{\beta_3}{\beta_1}(1-u)v_C + \frac{\beta_3}{\beta_1}(1-u)v_{Cref} = 0 \tag{4.13}$$

(4.13) can be written as

$$
\begin{aligned}
& C\frac{d^2v_C}{dt^2} + F_1\frac{dv_C}{dt} + F_2v_C + F_{3=0} \\
& where, \\
F_1 &= [\frac{1}{R_L} - \frac{P}{v_{Cref}^2} - \frac{\beta_2}{\beta_1}(1-u)] \\
F_2 &= -\frac{\beta_3}{\beta_1}(1-u) \\
F_3 &= \frac{\beta_3}{\beta_1}(1-u)v_{Cref}
\end{aligned}
\tag{4.14}
$$

(4.14) describes the behaviour of the closed loop system on the switching surface $s = 0$. To ensure the stability of the system on the switching surface $s = 0$, the following conditions must be satisfied.

$$F_1 > 0;\ and\ F_2 > 0 \tag{4.15}$$

Considering $\beta_1 = 1$ and nominal value of control input $u = d$ (*duty cycle of the converter*), the above conditions imply

$$\frac{1}{R_L} - \frac{P}{v_{Cref}^2} - \beta_2(1-d) > 0;\ and\ \ -\beta_3(1-d) > 0 \tag{4.16}$$

Therefore, to ensure the stability of the system with given operating conditions and loading profile, the values of the parameters β_2 and β_3 can be chosen to satisfy the following conditions.

$$\beta_2 < \frac{1}{(1-d)}[\frac{1}{R_L} - \frac{P}{v_{Cref}}]\ and\ \beta_3 < 0 \tag{4.17}$$

It is interesting to note that constant current component of the load does not play any role in the stability conditions obtained using linearized approximation of the load current. In the next section, the performance of the proposed SMC is validated through real-time simulation studies.

4.1.3 Real-time Simulation Studies

This section presents the validation of the performance of the proposed SMC to mitigate the CPL induced instabilities in the buck-boost converter system of Figure 4.1. The system under consideration was modeled in $MATLAB/SIMULINK^{TM}$ and simulated in real-time environment using ORDS. The steady-state and dynamic performance of the controller is validated in both operating modes (boost and buck), under different operating conditions. The nominal values of system parameters and different variables used in the real-time simulation studies are provided in Table 4.1. In this study the values of β_2 calculated using (4.17), are 2.488 and 1.458 for buck and boost mode respectively. This implies that the chosen controller parameters for the simulation studies satisfy the stability conditions given in (4.17). An image of the ORDS used to perform real-time simulation studies is shown in Figure 4.3. Next, real-time simulation studies to validate the performance of the proposed SMC are presented under boost operating mode, followed by real-time simulation studies under buck operating mode.

(a) Real-time simulation studies in boost mode

In boost mode, the converter is controlled to provide a regulated output voltage of $-380\ V$. The results of the real-time simulation studies in boost mode are shown in Figures 4.4-4.7. It can be seen in Figure 4.4 that the converter output voltage and the inductor current reach their references in less than 4 *ms* and stay there then on. The steady-state error in the

Table 4.1 : Parameters of buck-boost converter and the proposed SMC

Parameter	Value
Converter rating	1 kW
Inductance, L	2 mH
Capacitance, C	47 μF
Constants, $\beta_1,\ \beta_2,\ \beta_3$	$1,\ -50\ , -10000$
Constant, λ	2000
Constant, Q	0.5
Input voltage, E	220 V
Load resistance R	100 Ω
CPL, P	200 W
Constant current load, i_{const}	0.5 A
HPF time constant, τ	0.00015
Switching frequency, f_s	25 kHz

Figure 4.3 : An image of OPAL-RT digital simulator used for real-time simulation studies

voltage is zero, which is further confirmed in zoomed plot, shown in Figure 4.5. The transient response with respect to 30% reduction in the input voltage is shown in Figure 4.5. The output voltage is reduced by about 20 V and recovers to its steady-state value in < 0.020 s. The inductor current tracks its new reference instantly and the load current remains constant as there is no load change. Figures 4.6 and 4.7, show transient response with respect to the 100% increase in the constant current and constant power components of the load at $t = 0.8$ s and $t = 1.2$ s respectively, keeping resistive load fixed. The output voltage is momentarily reduced by 5 V and $6V$ in response to the step changes in the constant current and constant load respectively, which recovers to its steady-state value in less than 0.02 s. The inductor and the load currents change instantly to reflect the corresponding load changes.

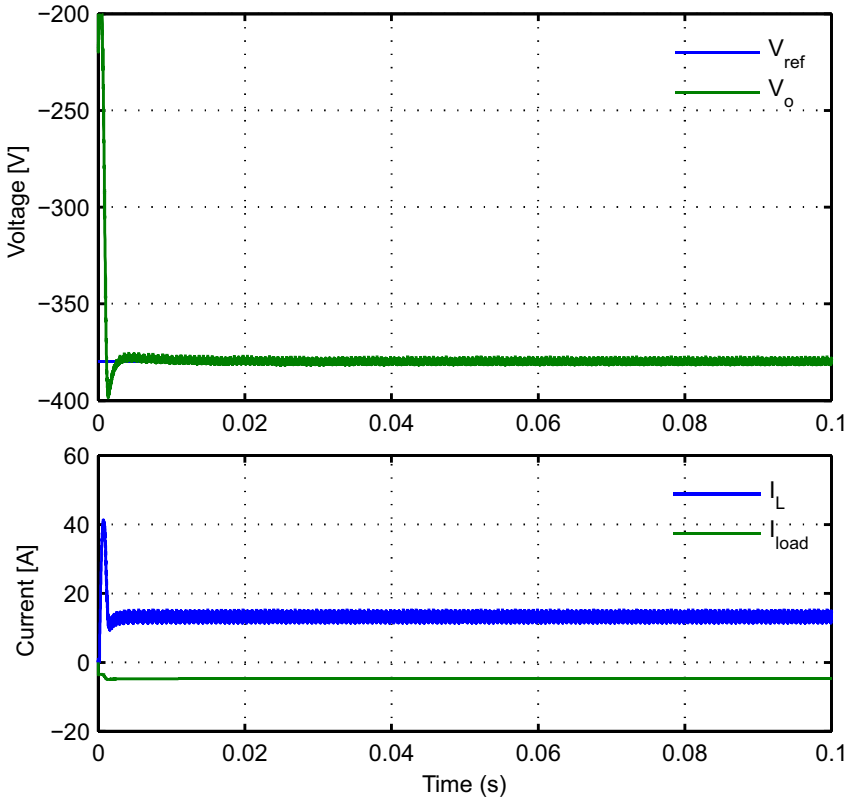

Figure 4.4 : Boost Mode: Start-up and steady state responses

(b) Real-time simulation studies in buck mode

The performance of the proposed controller has also been validated in buck mode, wherein the buck-boost converter system was controlled to produce a regulated output voltage of -120 V. The voltage and the current waveform in steady-state are shown in Figure 4.8, while Figures 4.9-4.11 show dynamic performance with respect to the step changes in the input voltage, constant current load, and constant power load; keeping resistive load fixed.

It can be seen in Figure 4.8 that, the output voltage reaches steady-state in less than 20 ms with zero steady-state error. The inductor current and load current also settle to their respective values. As shown in Figure 4.9, in response to the reduction of 30% in the input voltage at $t = 0.4$ s, the output voltage reduces by 8 V and recovers its steady-state value in less than 0.025 s. Furthermore, the inductor current tracks its changed reference quickly while load current remains unchanged as there was no change in the load. It can be observed from Figure 4.10 that the output voltage undergoes transient disturbance of very short duration confined in the range of (± 4 V), when constant current load is increased by 100%. The output

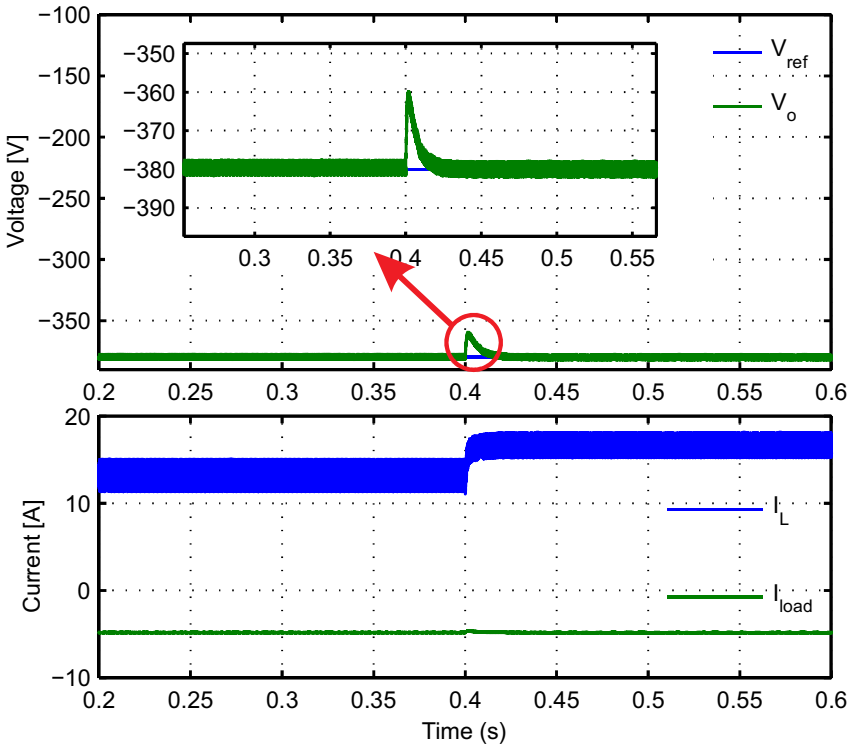

Figure 4.5 : Boost Mode: Transient s corresponding to 30% decrease in E at $t = 0.4\ s$

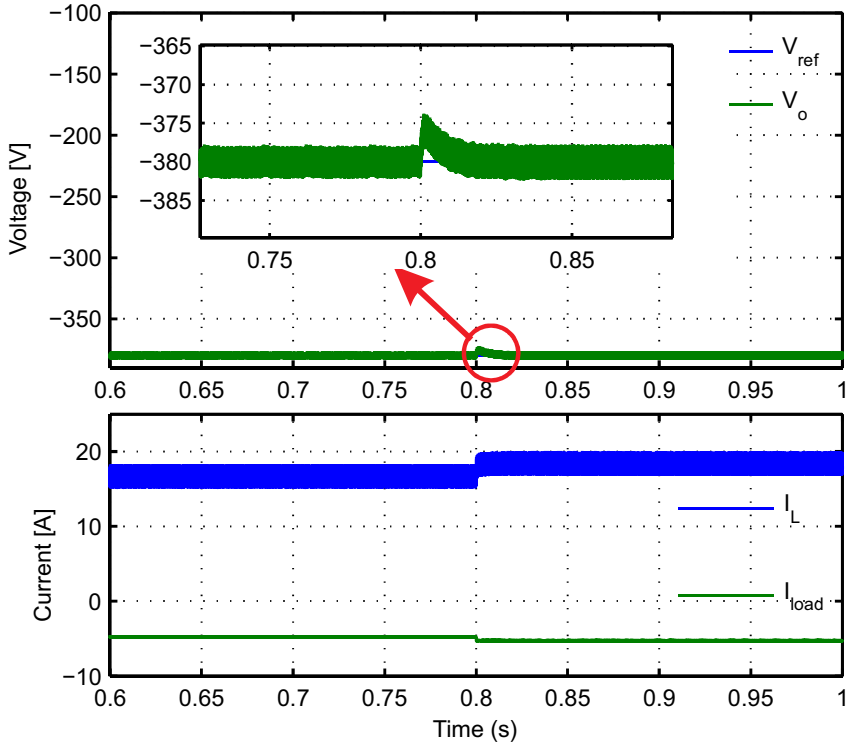

Figure 4.6 : Boost Mode: Transient responses corresponding to 100% increase in the constant current component of the load at $t = 0.8\ s$

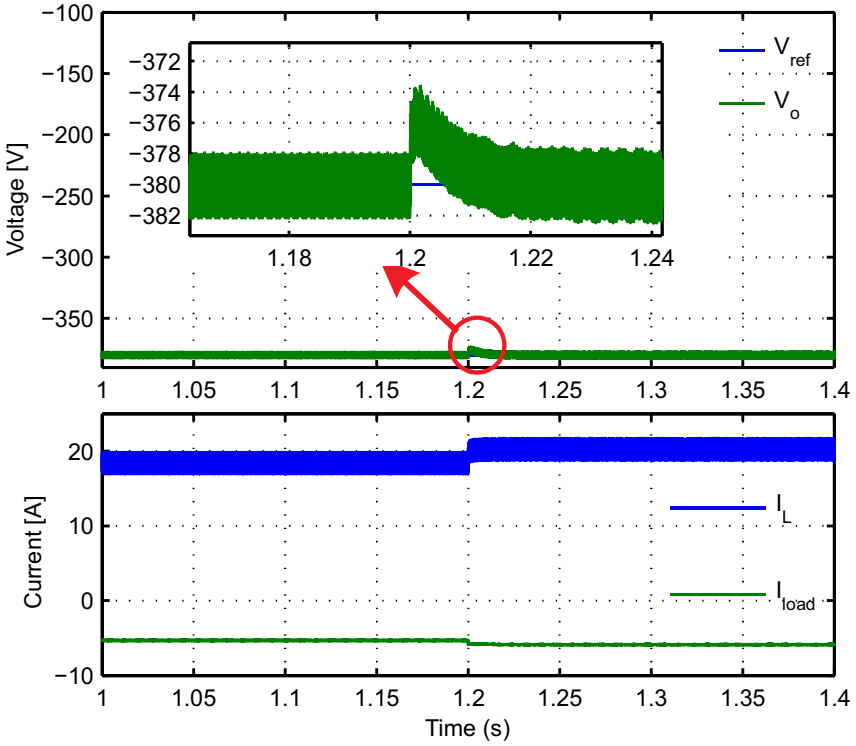

Figure 4.7 : Boost Mode: Transient responses corresponding to 100% increase in CPL at $t = 1.2\ s$

voltage recovers to its steady-state value in less than $0.010\ s$, and the inductor current and the load currents instantly change to reflect the increase in the load. The voltage and current waveforms corresponding to the 100% step increase in the constant power load are shown in the Figure 4.11. An impulse transient of ($< \pm 10\ V$) can be seen in the output voltage, which controller handles sufficiently well and forces the output voltage to its steady-state value. The inductor current in this case shows an overshoot at the instance of step change, but tracks its changed reference instantly. The load current also reflects the corresponding load change.

The performance of the proposed controller is validated through real-time simulation studies in boost and buck mode, under various operating conditions. The controller is able to mitigate instabilities due to the presence of the dominant CPL component, and tightly regulates the output voltage with zero steady state error. The controller is robust with respect to the changes in the input voltage, constant current load, and constant power load. The effectiveness of the proposed controller has been validated with realistic composite load profile.

4.2 MITIGATION OF CPL INDUCED INSTABILITY EFFECTS IN BIDIRECTIONAL DC/DC CONVERTER

In this section, mitigation of negative impedance instabilities in a BDC feeding a CPL dominated load is addressed. The BDC is considered to interface a storage unit, in an isolated DCMG. In addition to the storage unit, the DCMG has RESs interfaced to its dc bus, and supplies a mixed load (CPL and CVL). To design a SMC, the isolated DCMG is replaced by an equivalent system, with RESs operating under MPPT control and CPL combined to form a net CPL. In the following section, the detailed description of the test system and its modeling are presented.

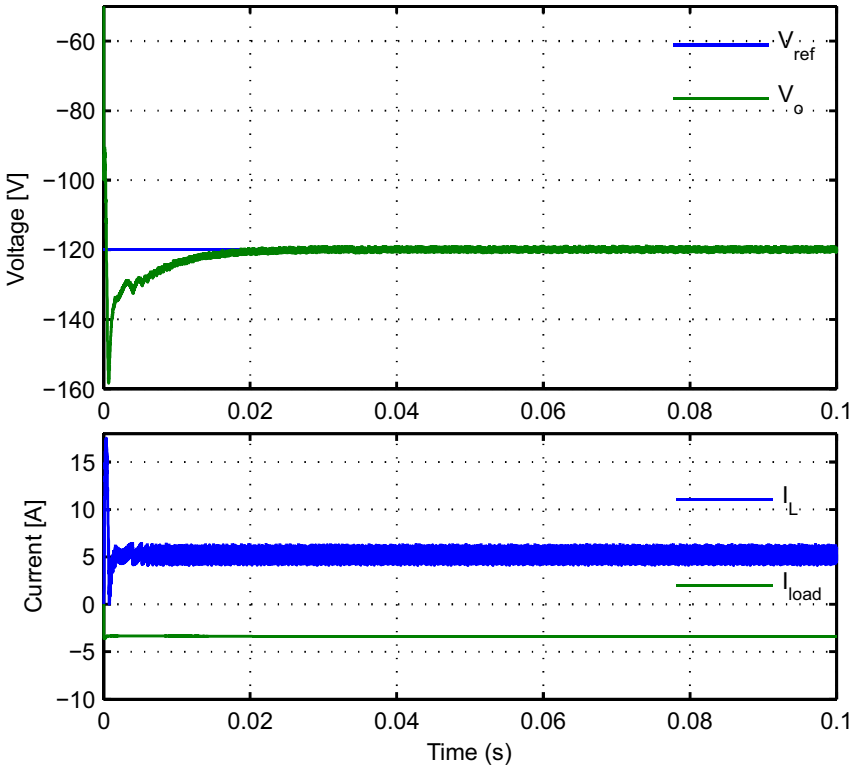

Figure 4.8 : Buck Mode: Start-up and steady state responses

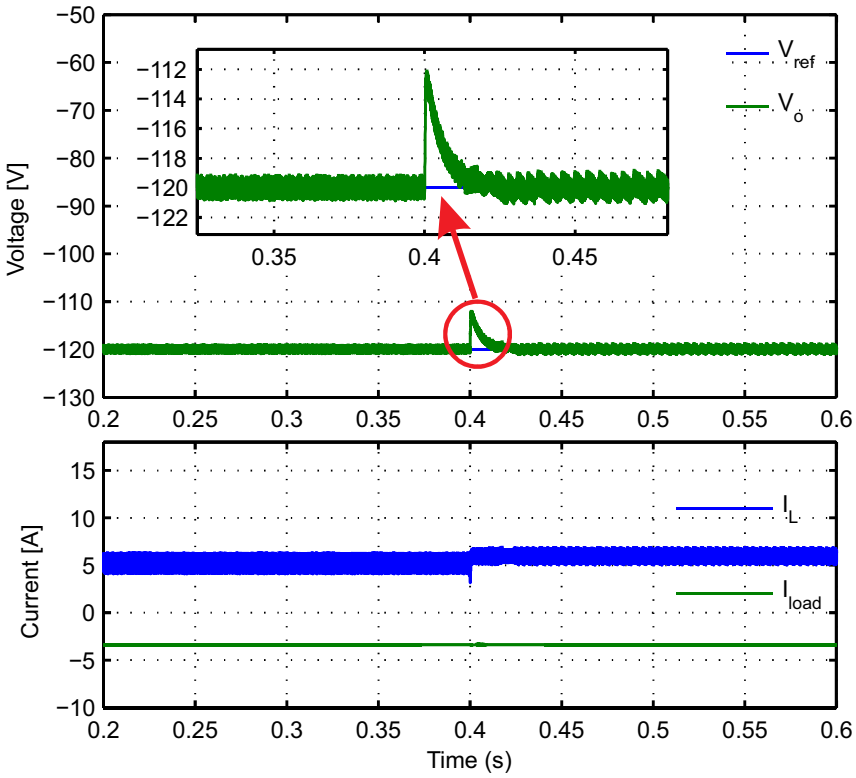

Figure 4.9 : Buck Mode: Transient responses corresponding to 30% decrease in E at $t = 0.4\ s$

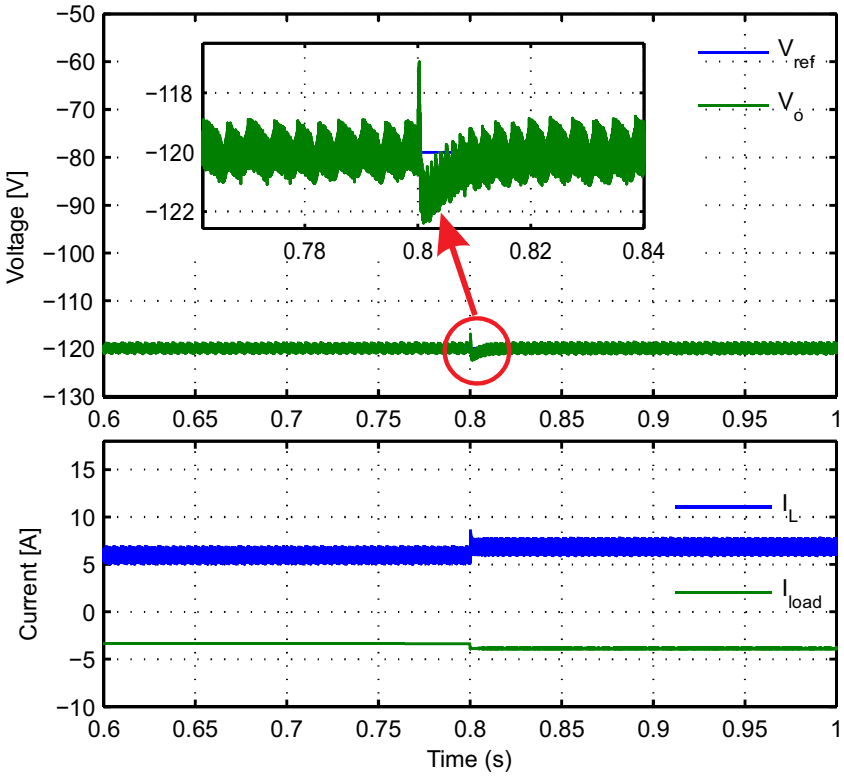

Figure 4.10 : Buck Mode: Transient responses corresponding to 100% increase in the constant current component of the load at $t = 0.8\ s$

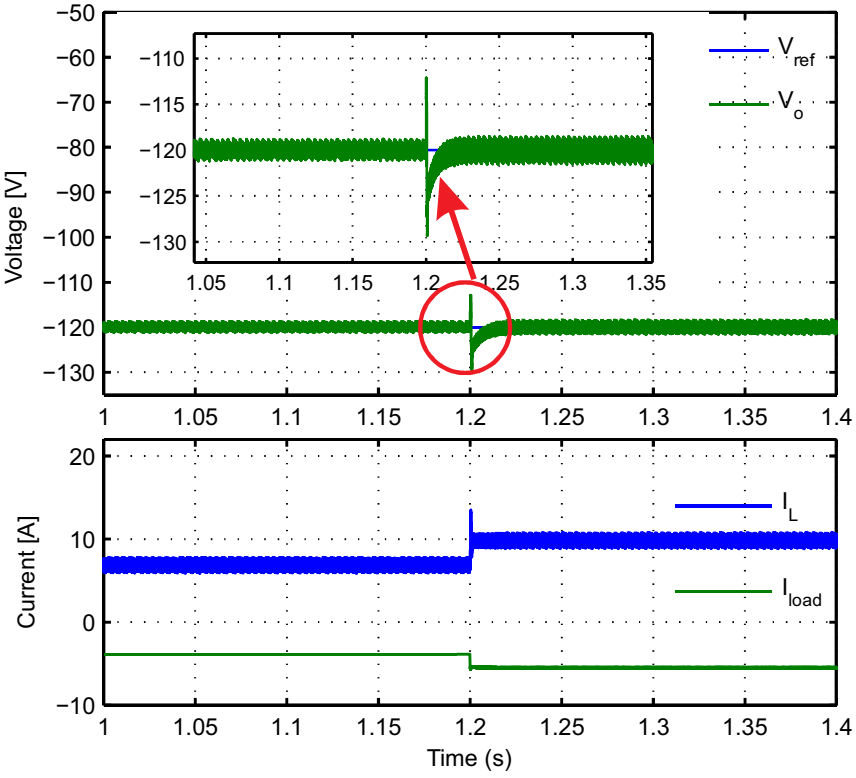

Figure 4.11 : Buck Mode: Transient responses corresponding to 100% increase in CPL at $t = 1.2\ s$

4.2.1 Modeling of Bidirectional DC/DC Converter

The schematic diagram of a typical RESs based isolated DCMG is shown in Figure 4.12. The load on the system is considered to be predominantly of CPL in nature. The sources (solar PV, wind generator, fuel cell) contribute a total power supply P_S (referred by a negative value) while load power P (referred by a positive value) includes the power consumed by CPL only. BDC standing at the interface of dc bus and battery storage, facilitates bidirectional flow of power (charging and discharging battery) to ensure dc bus voltage regulation depending upon the net balance between power available from the sources and load demand. For the control design and analysis, the sources and CPL are aggregated to represent the net power demand $P_n = P_S + P$. When sources provide more power than required by the constant power load i.e. $|P_S| \geq |P| \Longrightarrow P_n \leq 0$, sources supply power to the load and residual power is used to charge the batteries (BDC operates under charging mode). When sources cannot provide enough power demanded by the constant power load i.e. $|P_S| \leq |P| \Longrightarrow P_n \geq 0$, the battery discharges and supplies required power to the load (BDC works under discharging mode). In discharging mode, as demand is greater than the available power, bus voltage is reduced and due to the presence of CPL ($VI = K$), the load current is further increased. Therefore, situation becomes critical in the presence of CPL.

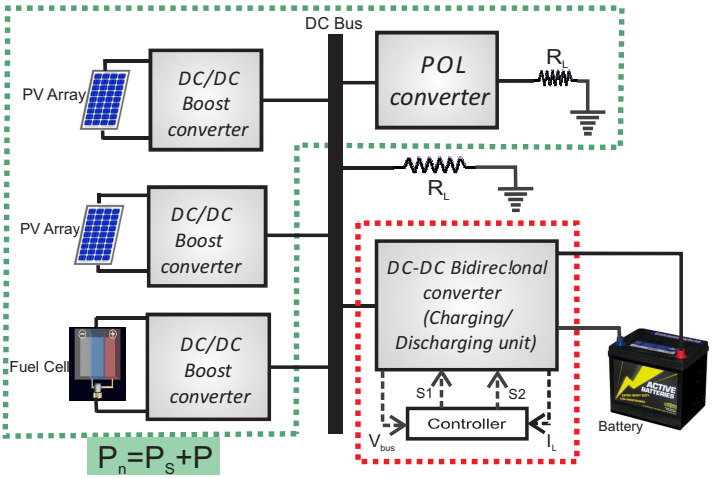

Figure 4.12 : Schematic diagram of a typical isolated dc microgrid

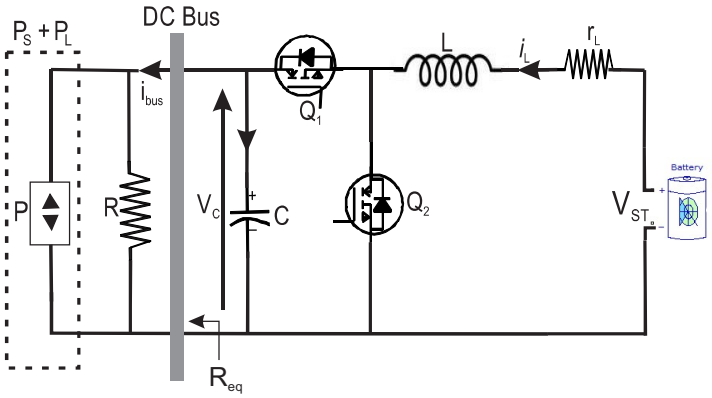

Figure 4.13 : Equivalent circuit of dc microgrid with bidirectional dc/dc converter

The circuit diagram of the equivalent dc microgrid where the rest of the system is seen as a load by BDC, is shown in Figure 4.13. Switches Q_1 and Q_2 are assumed to be complimentary i.e. when Q_1 is on, Q_2 is off and vice versa. Therefore, switching control input u is uniquely

designed as $u \in \{0,1\}$ with reference to switch Q_1, i.e., when $u = 0$ Q_1 is off and Q_2 is on, and vice versa. The operation of BDC in charging and discharging mode is shown through a block diagram in Figure 4.14.

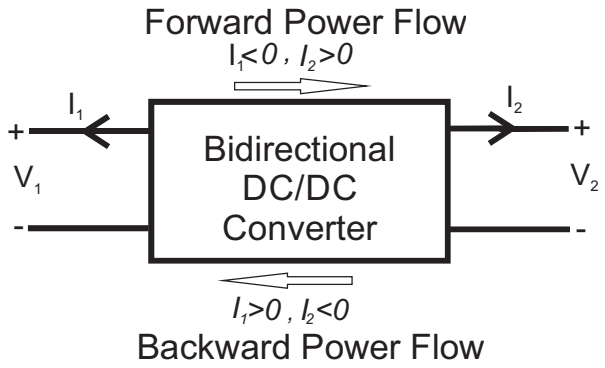

Figure 4.14 : Operation of a BDC during charging and discharging mode

Now considering the equivalent circuit of Figure 4.13, the total instantaneous current drawn from the dc bus by the combination of CVL and net DCMG demand P_n is given by

$$i_{bus} = \frac{v_C}{R_L} + \frac{P_n}{v_C}; \tag{4.18}$$

that is,

$$i_{bus} = i_{CPL} + i_{CVL} \quad and \quad R_{eq} = \frac{v_C}{i_{bus}} \tag{4.19}$$

where $P_n = P_S + P$ is the total demand which could be positive or negative, R_L is the resistive of (CVL), i_{CPL} is the current drawn by the CPL, and i_{CVL} is the current drawn by the resistive load. R_{eq} is the equivalent load resistance and v_C is the capacitor voltage which is equal to the dc bus voltage. The non-linear state-space averaged model of the system shown in Figure 4.14, is given by

$$L\frac{di_L}{dt} = V_{bat} - r_L i_L - u v_C \tag{4.20a}$$

$$C\frac{dv_C}{dt} = u i_L - \frac{v_C}{R_L} - \frac{P_n}{v_c} \tag{4.20b}$$

where L is the inductance of the converter and its value is decided based on a permissible ripple in inductor current. C is the capacitance of the converter and its value is chosen based on permissible ripple in dc bus voltage. V_{bat} is nominal battery voltage. r_L is the equivalent series resistor of the BDC inductor. i_L and v_C are the instantaneous values of inductor current and capacitor voltage respectively. The dynamic model of (4.22) can be represented in normalized coordinates using the following transformation

$$\begin{bmatrix} i_L \\ v_c \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{C}{L}} V_{bat} & 0 \\ 0 & V_{bat} \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} and \ \tau = \frac{t}{\sqrt{LC}} \tag{4.21}$$

As given by

$$\frac{dx}{d\tau} = 1 - Qx - uy \tag{4.22a}$$

$$\frac{dy}{d\tau} = ux - My - \frac{N}{y} \tag{4.22b}$$

where $J = \sqrt{\frac{C}{L}} r_L \in \mathbb{R}^+$, $M = \frac{1}{R_L}\sqrt{\frac{L}{C}} \in \mathbb{R}^+$, and $N = \sqrt{\frac{L}{C}} \frac{P_n}{V_{bat}^2} \in \mathbb{R}$, are the normalized parameters of the system, while the control input $u \in \{0,1\}$ remains the same. In the normalized state

vector $z=[x,y]$, $x\in\mathbb{R}^+$ and $y\in\mathbb{R}^+$ are related to the inductor current and the capacitor voltage respectively. In the next section, design of a robust SMC for the system described by the dynamic model given in (4.21) is proposed.

4.2.2 Sliding mode control design

In this section, a robust SMC is designed to ensure dc bus voltage regulation in the presence of fluctuating power supply from RESs and in the presence of the CPL. In the following subsections, definition of switching function, control law, the proof of existence of sliding mode and system stability are presented.

(a) Switching function

The switching function s in terms of the normalized state variables is defined as

$$s=y-y_{ref}+\mu(x-x_{ref}) \tag{4.23}$$

where x_{ref} and y_{ref} are the reference values of state variables x and y respectively and $x_{ref}=My_{ref}^2+N$. The constant $\mu>0$ is a parameter of the switching function which controls the convergence speed. The control objective is to drive the normalized voltage y and current x to a desired equilibrium point y_{ref} and x_{ref} respectively. The following discontinuous control law is chosen

$$u:=\frac{1}{2}(1+sgn(s))=\begin{cases}1 & \text{if } s>0\\ 0 & \text{if } s<0\end{cases} \tag{4.24}$$

The control law of (4.24) with switching function (4.24) should force the system trajectories from an arbitrary initial point on to the switching surface $s=0$ and constrain to the switching surface then on. The existence of sliding mode and stability of the system on switching surface $s=0$ are proved in the following subsections.

(b) Existence of sliding mode

The existence or accessibility of sliding mode is proved through the reachability condition $s^T\dot{s}<0$ i.e., when $s>0$, $\dot{s}$ should be negative and vice-versa, which ensures the existence of sliding mode.

Case I: $s>0$

Since $s>0$, from equation (4.24), the switching control law $u=1$. Therefore, to ensure the reachability condition from (4.23) it follows

$$\dot{s}=\dot{y}+\mu\dot{x}<0 \tag{4.25}$$

Substituting the values of $\dot{x}$ and $\dot{y}$ from (4.22)

$$x-My-\frac{N}{y}+\mu(1-y)<0 \tag{4.26}$$

Assuming that the value of inductive resistance is very small, i.e. $J=0$. Solving (4.24) for the reference values of x and y i.e., x_{ref} and y_{ref} respectively, and considering $y_{ref}>1$ i.e., taking bus voltage greater than the nominal battery voltage, implies

$$\mu>\frac{x_{ref}-My_{ref}-\frac{N}{y_{ref}}}{y_{ref}-1} \tag{4.27}$$

since $x_{ref}=My_{ref}^2+N$, equation (4.27) simplifies to

$$\mu>\frac{x_{ref}}{y_{ref}} \tag{4.28}$$

Case II: $s < 0$

Since $s < 0$, from equation (4.24), the switching control law $u = 0$. Therefore, to ensure the reachability condition from (4.23) it follows

$$\dot{s} = \dot{y} + \mu\dot{x} > 0 \tag{4.29}$$

Substituting the values of $\dot{x}$ and $\dot{y}$ from (4.22)

$$-My - \frac{N}{y} + \mu > 0 \tag{4.30}$$

Solving (4.30) for the reference values of x and y i.e. x_{ref} and y_{ref} respectively

$$\mu > \frac{x_{ref}}{y_{ref}} \tag{4.31}$$

Therefore, to ensure the existence of sliding mode condition of (4.31) should be satisfied.

(c) Stability of switching surface

For the stability of the system x should approach x_{ref} and y should approach y_{ref} asymptotically, when sliding mode $s = 0$ is established. Since sliding mode $s = 0$ establishes a linear relation between state variables x and y, therefore system order is reduced by 1. Hence, stability of variable x necessarily implies stability of y i.e., $s = 0 \Rightarrow y = -\mu x$. Therefore, stability of y implies stability of x and vice versa.

To prove the stability of switching surface, equivalent control concept is used here. Equivalent control u_{eq} is defined as the smooth feedback control law which ideally restricts the state trajectory to the switching surface s. The value of u_{eq} is calculated according to the following equation

$$\dot{s} = 0 \tag{4.32}$$

From equation (4.32)

$$\dot{s} = \dot{y} + \mu\dot{x} = 0 \tag{4.33}$$

Substituting the values of $\dot{x}$ and $\dot{y}$ from (4.22) and solving (4.33) for equivalent control law u_{eq} is given by,

$$u_{eq} = \frac{My + \frac{N}{y} - \mu}{x - \mu y} \tag{4.34}$$

The ideal sliding dynamics occurs when u_{eq} acts on the system as a feedback control with $s = 0$ i.e., $y = y_{ref} - \mu(x - x_{ref})$, is given by,

$$\dot{x} = \frac{x - My^2 - N}{x - \mu y} \tag{4.35}$$

The fact that the dynamics (4.35) exhibits stable point of equilibrium i.e. $x = x_{ref}$, can be established via several approaches like phase plane approach, approximate linearization approach or Lyapunov stability theory. Here, the stability of ideal sliding dynamics of (4.35) is proved through the approximate linearization approach.

Approximate Linearization Approach: Let $e_1 = x - x_{ref}$ and $e_2 = y - y_{ref}$. Then, from (4.31),

$$\dot{e_1} = \frac{e_1 - Me_2(e_2 + 2y_{ref})}{e_1 - \mu e_2 + x_{ref} - \mu y_{ref}} \tag{4.36}$$

and

$$s = e_2 + \mu e_1 = 0 \tag{4.37}$$

Linearizing equation (4.36) after some algebraic manipulation and neglecting higher power terms of error gives

$$\dot{e_1} = \frac{e_1(1 + 2M\mu y_{ref})}{x_{ref} - \mu y_{ref}} \tag{4.38}$$

For the system (4.38) to be asymptotically stable i.e. $e_1 \to 0$ as $t \to \infty$, the following condition must satisfy

$$\frac{1 + 2M\mu y_{ref}}{x_{ref} - \mu y_{ref}} < 0 \tag{4.39}$$

Since $\mu > 0$ and $M, y_{ref} \in \mathbb{R}^+$, hence the necessary condition for stability of e_1 is given by

$$\mu > \frac{x_{ref}}{y_{ref}} \tag{4.40}$$

Which is same as the existence condition. From (4.37), stability of e_1 implies stability of e_2. Hence, (4.40) gives the necessary and sufficient condition for the existence and stability of the system during sliding mode with switching function of (4.23) and control law (4.24).

(d) Switching frequency

To prevent high frequency chattering and losses due to ideally infinite high switching frequency of conventional SMC, it is desired that switching frequency be limited to practical limits imposed by the switches. The solution using a hysteresis band between the de-normalized switching surface s_d and the switching control law u, is employed to avoid very high switching and to confine switching losses

$$u := \begin{cases} 1 & \text{if } S_d > h \\ 0 & \text{if } S_d < -h \\ u_p & \text{if } -h \le S_d \le h \end{cases} \tag{4.41}$$

where u_p is the previous value of u and h is a constant which represents the width of the hysteresis band and is obtained by the following equation [Tahim et al., 2012],

$$h = \frac{V_{bat}(v_C - V_{bat})}{2Lf_s v_C} \tag{4.42}$$

where f_s is steady state switching frequency.

(e) Implementation aspects and tuning

It is necessary to convert the parameters in de-normalized form to design and implement the controller. The parameters which are to be de-normalized are, (i) the switching surface parameter (μ), and (ii) the width of the hysteresis band (h). The de-normalized switching surface is represented as

$$s_d = (v_C - v_{Cref}) + \gamma(i_L - i_{Lref}) \tag{4.43}$$

where $\gamma = \sqrt{\frac{L}{C}}\mu$ is de-normalized switching surface parameter and v_{Cref} and i_{Lref} are reference values of capacitor (bus) voltage and inductor current respectively. The value of h is calculated by replacing v_C by v_{Cref} in equation (4.42). The circuit diagram showing complete implementation scheme of the proposed SMC is given in Figure 4.15.

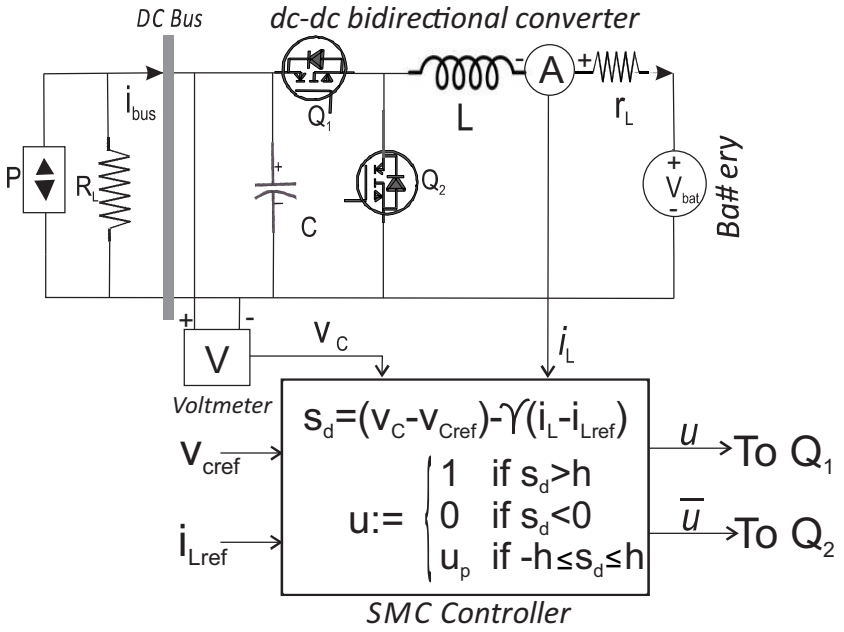

Figure 4.15 : Implementation scheme of the proposed SMC for bidirectional dc/dc converter

4.2.3 Real-time Simulation Studies

The effectiveness of the proposed SMC under source power and load variations is validated through real-time simulation studies conducted using ORDS (shown in Figure 4.3). The parameters of the converter and the controller used in simulation studies are provided n Table 4.2. The value of reference inductor current is calculated from equation (4.18) as: $i_{Lref} = \frac{i_{bus}}{d}$, where $d = \frac{V_{bat}}{v_{Cref}}$ is the duty cycle of switch Q_1. Simulation studies have been conducted under the following operating conditions. Four step changes were applied in the power P_n. The BDC initially starts in charging mode.

Table 4.2 : Parameters of bidirectional dc/dc converter and the proposed SMC

Parameter	Symbol	Value
Reference Bus Voltage	v_{cref}	120 V
Nominal Battery Voltage	V_{bat}	60 V
Inductance of BDC	L	5 mH
Capacitance of BDC	C	1000 μF
Inductive Resistance	r_L	0.22 Ω
Switching Surface parameter	γ	5
Switching Frequency	f_s	40 kHz
Resistive Load	R_L	200 Ω

- At $t = 0.1\ s$, $P_n = -400\ W \rightarrow 200\ W$ (discharging)
- At $t = 0.2\ s$, $P_n = 200\ W \rightarrow 50\ W$ (discharging)
- At $t = 0.3\ s$, $P_n = 50\ W \rightarrow -200\ W$ (charging)
- At $t = 0.4\ s$, $P_n = -200\ W \rightarrow 100\ W$ (discharging)

The real-time simulated response of the system corresponding to the above mentioned operating conditions is given in Figure 4.16, showing plots of the output voltage, the inductor

current, State-of-charge (SoC) of the battery and power ($P_n = P_S + P$). The red curves show the reference values and blue curves show the actual values. It can be seen from Figure 4.16(b), that the output voltage reaches its reference value in less than 20 *ms* with negligible steady-state error. The inductor current (Figure 4.16(c)) tracks its reference value perfectly, but has high start up value which is quite natural keeping in view I-V characteristics of the CPL (voltage is small at the start up which results in the high value of the inductor current). The controller ensures dc bus voltage regulation within permissible limits in spite of various step changes in the power P_n.

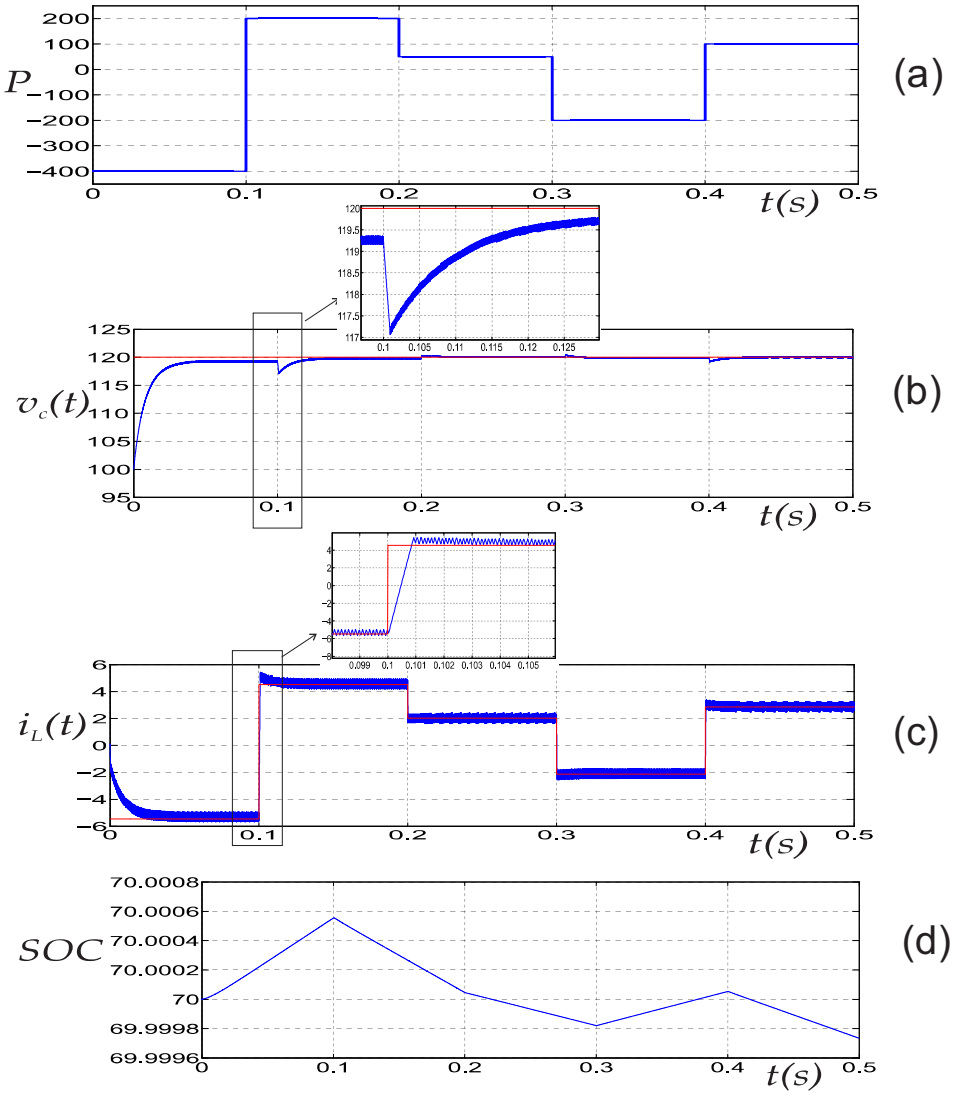

Figure 4.16 : Real-time simulation response of the proposed SMC with BDC

Thus, real-time simulation responses of the bidirectional dc/dc buck-boost converter system validate the effectiveness of the proposed controller to absorb dc bus transients which occur due to load and source variations, mitigate the destabilizing effects of the CPLs, and to maintain the bus voltage within tight limits. The robustness of the controller with respect to the large changes in the CPL power is evident from the simulated response.

4.3 SUMMARY

In this chapter mitigation of negative impedance instabilities in an inverted topology dc/dc buck-boost converter feeding a composite load has been addressed. The proposed robust sliding mode controller ensures tight regulation of the converter output voltage and stability under CPL dominated load. A condition for system stability has been obtained. Both buck and boost operating modes of the converter have been considered, wherein the converter is responsible to maintain its output voltage at the desired level. The steady-state and dynamic performance of the controller has been validated through real-time simulation studies using ORDS. The controller is found to be robust with respect to the sufficiently large variations in the supply voltage and the load.

In the second part of the chapter, mitigation of negative impedance instabilities in a bidirectional dc/dc converter, interfacing a storage unit in a typical isolated dc microgrid is addressed. The net CPL power (aggregate of power produced from RESs operating in MPPT mode and exhibiting constant power source characteristics, and CPL) is used to select the operating mode of the BDC. A robust sliding mode controller for BDC has been proposed to ensure tight regulation of dc bus voltage and system stability in different operating modes. Furthermore, the existence of sliding mode and system stability have been proved. The effectiveness of the controller has been validated through real-time simulation studies using ORDS. The controller demonstrates the dc bus regulation remains within tight limits ($\pm 0.83\%$ of its nominal value) and robustness with respect to the sufficiently large variations (150%) in the net power demand. In the next chapter, mitigation of the destabilizing effects of CPL will be addressed in a complete dc microgrid scenario with many converters, storage unit, and a diverse load profile, using robust sliding mode approach.

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